1S-10

Rapid Prototyping of Multi-Mode QC-LDPC Decoder for 802.11n/ac Standard

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LDPC Codes & Decoders

LDPC codes are widely applied:
GMR-1, DVB-S2, DVB-S2X, IEEE 802.11n/ac (WiFi), 802.16, 802.11ad, 802.3, DVB-T2, DVB-NGH, ATSC, DTMB, CMMB, G.hn, IEEE 802.15.3c…

LDPC decoders are well studied:
Limit-approaching error rate, moderate complexity, economical power consumption, Gbps throughput…

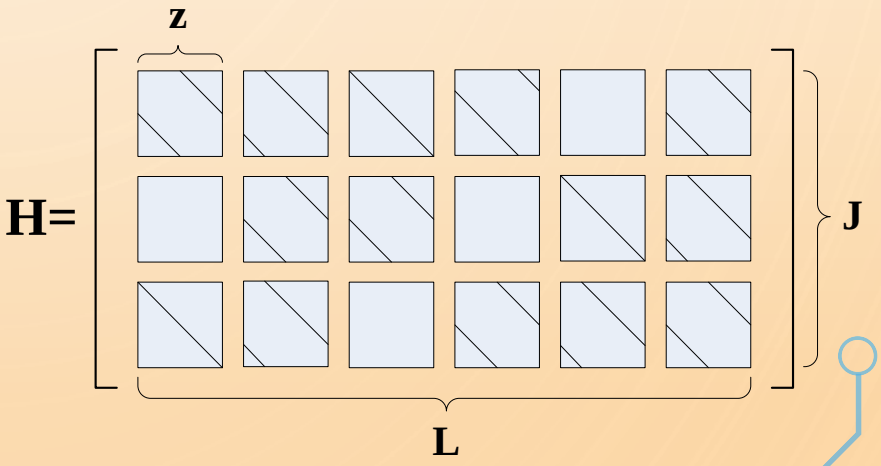
A practical issue: dynamic code

	High length/low rate	Low length/High rate
Error rate	low	high
Complexity	high	low
Power	high	low
Throughput	low	high
SNR	low	high

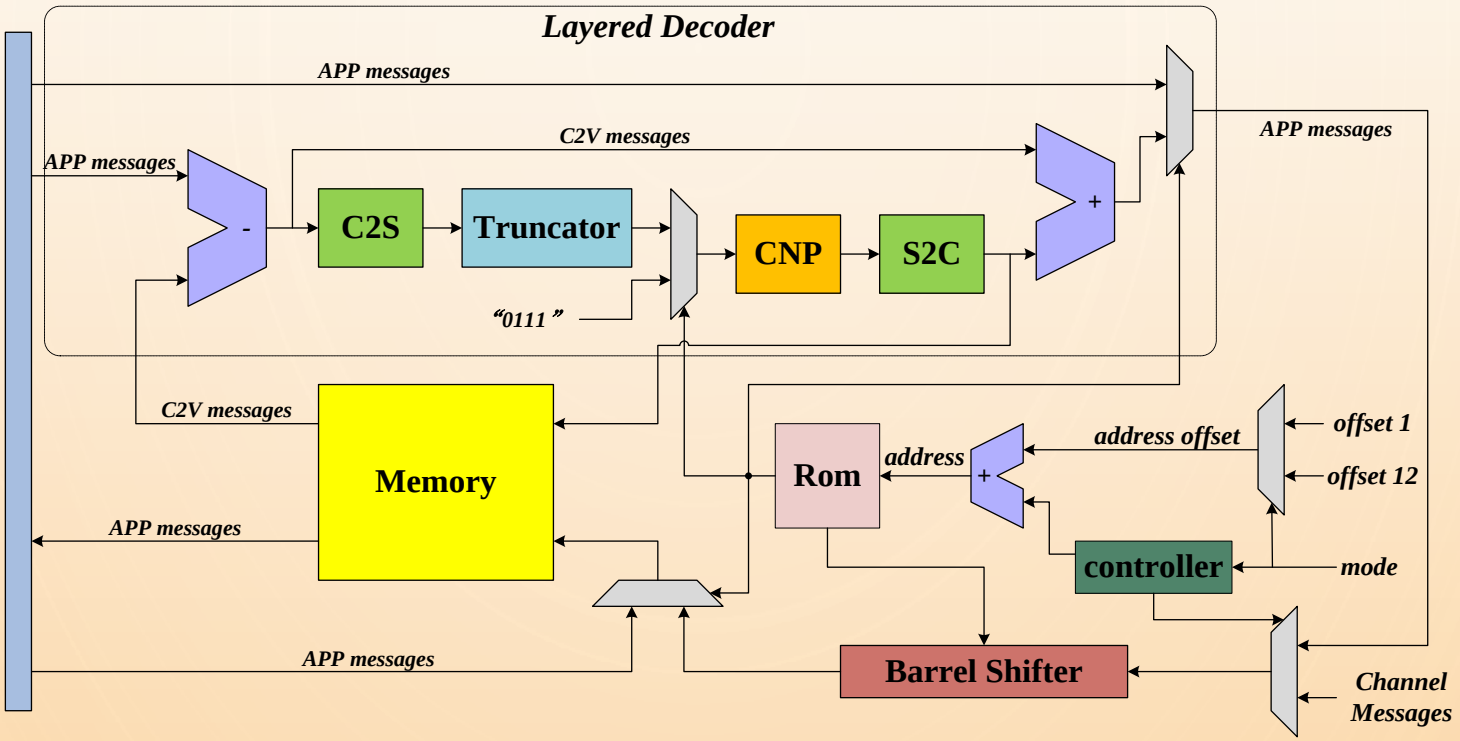
Multi-Mode Decoder

IEEE 802.11n/ac (WiFi) Standard:

- 12 codes of different sizes and patterns
- 24 block columns (L=24)
- code length: 648, 1296, 1944 (z=27, 54, 81)
- code rate: 1/2, 2/3, 3/4, 5/6 (J=12, 8, 6, 4)

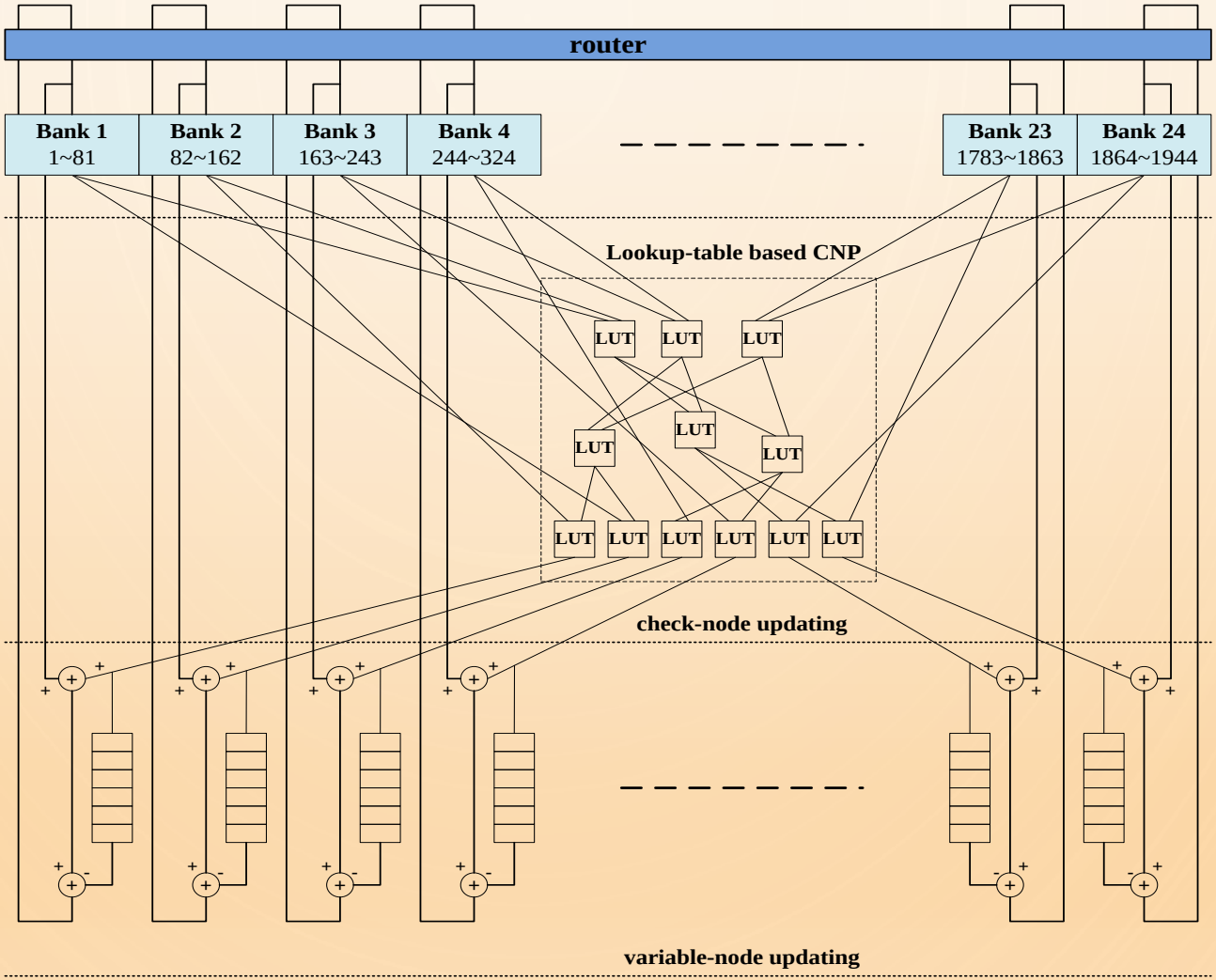


Proposed Architecture (RTL)

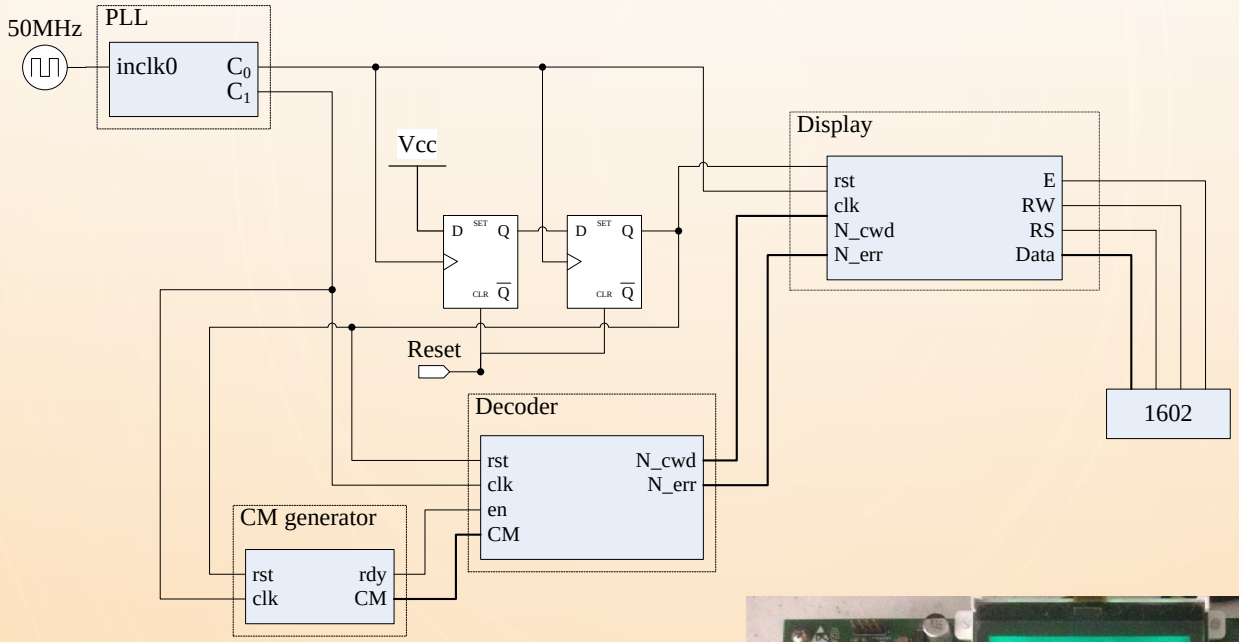


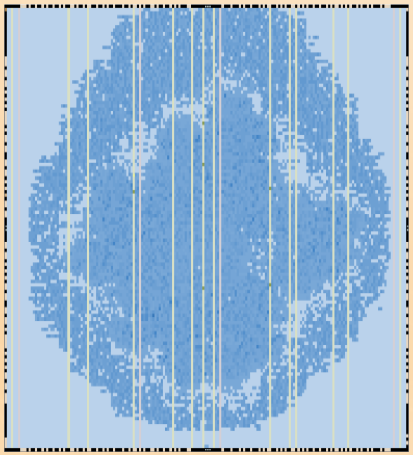
- Objectives: on-the-fly configurability and others things under this premise
- Configurations: layered decoding & sum-product algorithm, 5 iterations, 4-bit quantization, 27 parallelism
- Features: addressable patterns stored in ROM, patent-dependent routing, dynamic memory allocation, spatial-temporal rotation for message alignment

Layered Decoding

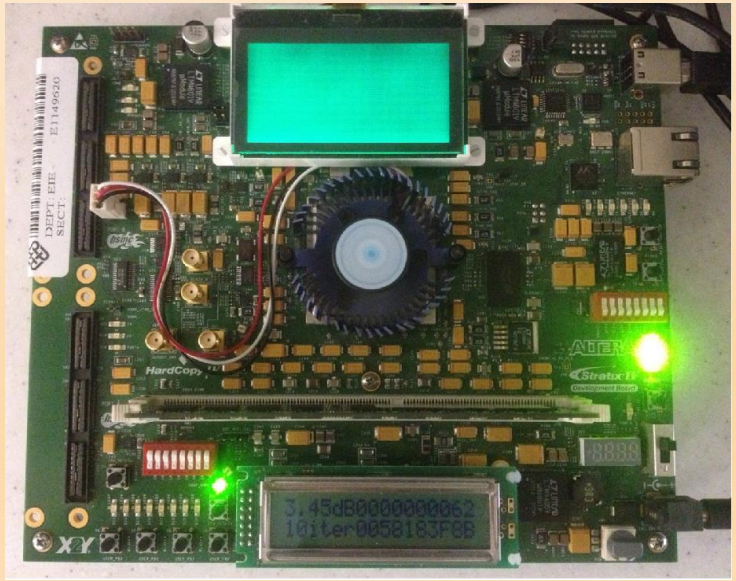


Implementation (FPGA)

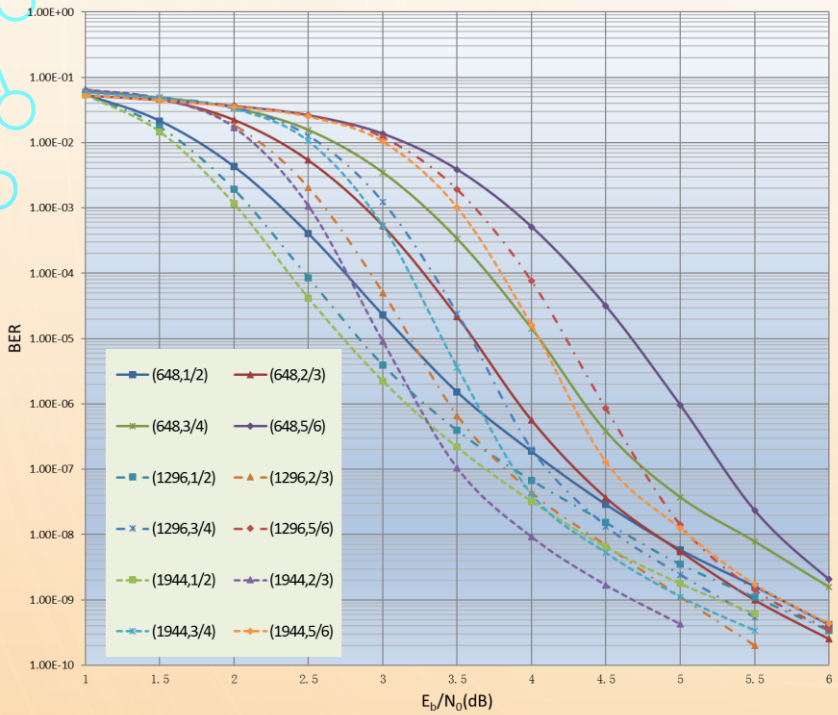




(45%)



Implementation (cont'd)



	Our design	[1]
FPGA device	Stratix IV	Virtex-4
LUTs	64475	52565
Registers	108879	#
Memory type	Shift registers	2-port RAM
ROM bits	21888	#
Quantization	4 bits	5 bits
No. of Iterations	5	10
Pipelining stages	1	3
Clock frequency (MHz)	60	121
Throughput (Mbps)	382-1852	308.6-1507

Mode	1/2	2/3	3/4	5/6
648 bits	637 Mbps	948 Mbps	1.25 Gbps	1.85 Gbps
1296 bits	425 Mbps	632 Mbps	8.26 Gbps	1.23 Gbps
1944 bits	382 Mbps	569 Mbps	7.52 Gbps	1.11 Gbps

[1] Kumawat, S.; Shrestha, R.; Daga, N.; Paily, R., "High-Throughput LDPC-Decoder Architecture Using Efficient Comparison Techniques & Dynamic Multi-Frame Processing Schedule," in *Circuits and Systems I: Regular Papers, IEEE Transactions on* , vol.62, no.5, pp.1421-1430, May 2015

Summary

1. A multi-mode QC-LDPC decoder has been proposed and implemented for the 802.11 n/ac WLAN protocol .
2. Only 24% overhead has been introduced to the largest single-mode decoder.
3. The storage scheme has facilitated a simple-structured memory requirement using shift registers of size 109 Kb.
4. Due to a parallelism degree of 27, the decoder has achieved a maximized throughput and meanwhile eliminated idleness for all modes.
5. An LUT-based method and parallel-routing network have been applied to design the check-node processor, therefore the accuracy and latency are both improved.
6. The throughput varies from mode to mode, ranging from 382 Mbps up to 1.85 Gbps with 60 MHz operational clock rate.
7. With 5-iteration layered decoding, the achievable BER is as low as 10^{-9} at E_b/N_0=4.7 dB.

Thank You

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