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A Noise Reduction Technique for Divider-Less Fractional-*N* Frequency Synthesizer using Phase-Interpolation Technique

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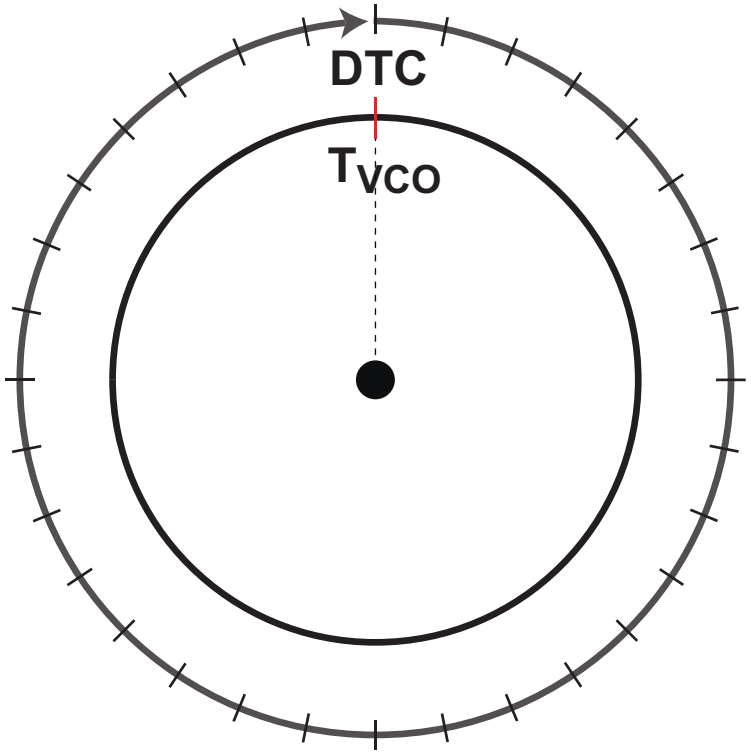
Motivation

- **Divider-less integer-*N* PLL:**
  - **Exhibits extremely low-jitter.**
  - **Suitable for wireless frequency synthesis.**
- **Divider-less PLL as frequency synthesizer:**
  - **Worsens jitter performance.**
  - **Large fractional spurs.**

} **Bottleneck**
Multi-phase generator used for frac.-*N* operation

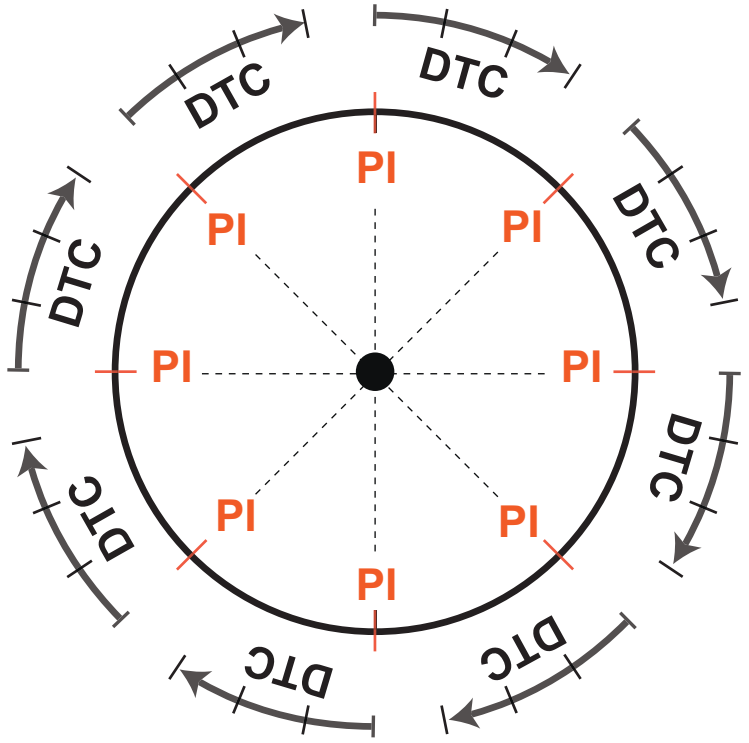
Aim: Divider-less FNPLL with low-jitter and low-spur

Jitter Considerations



Conventional DTC only topology

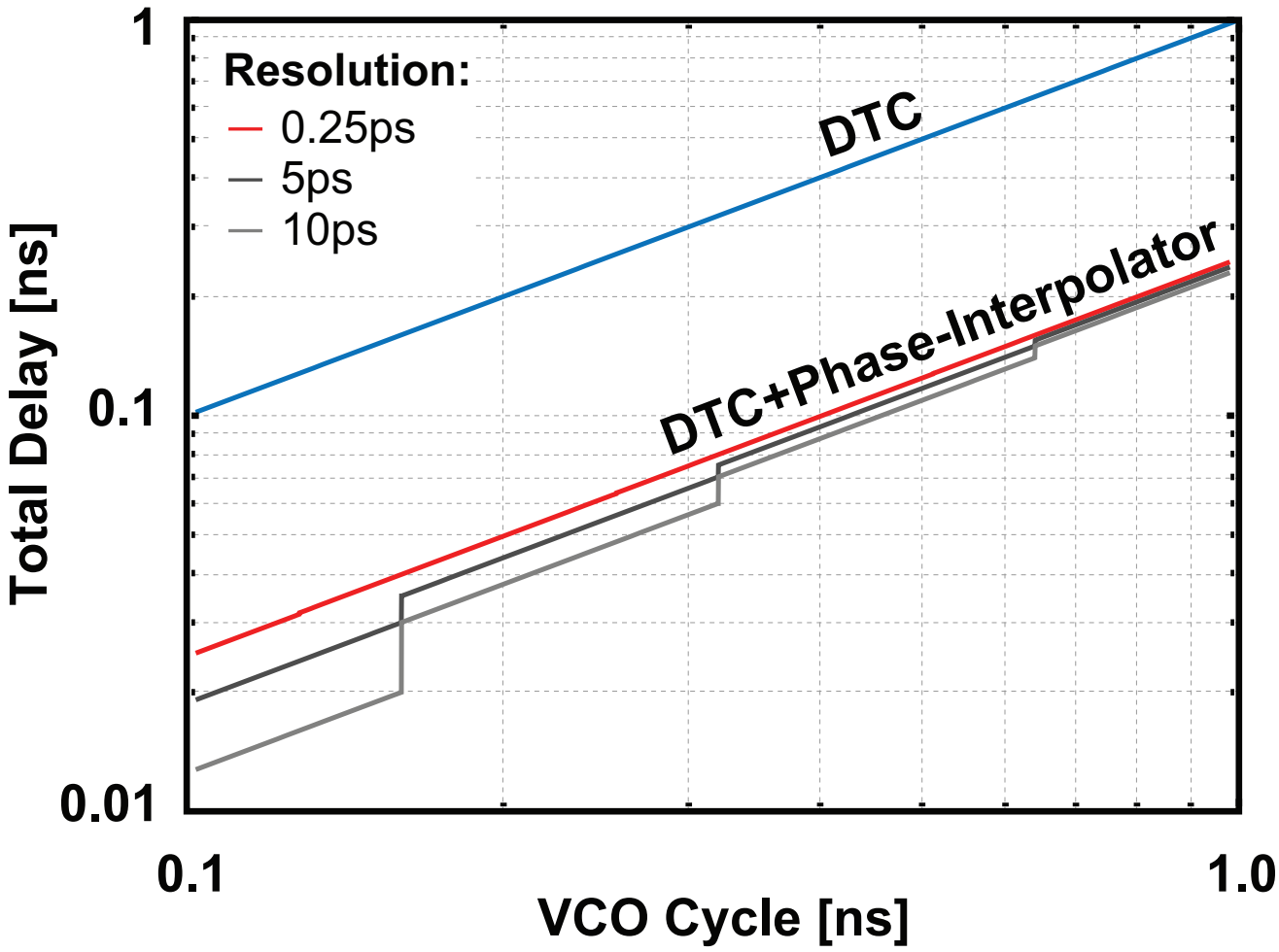
$$T_{DR,DTC} \geq T_{VCO}$$



Proposed PI + DTC topology

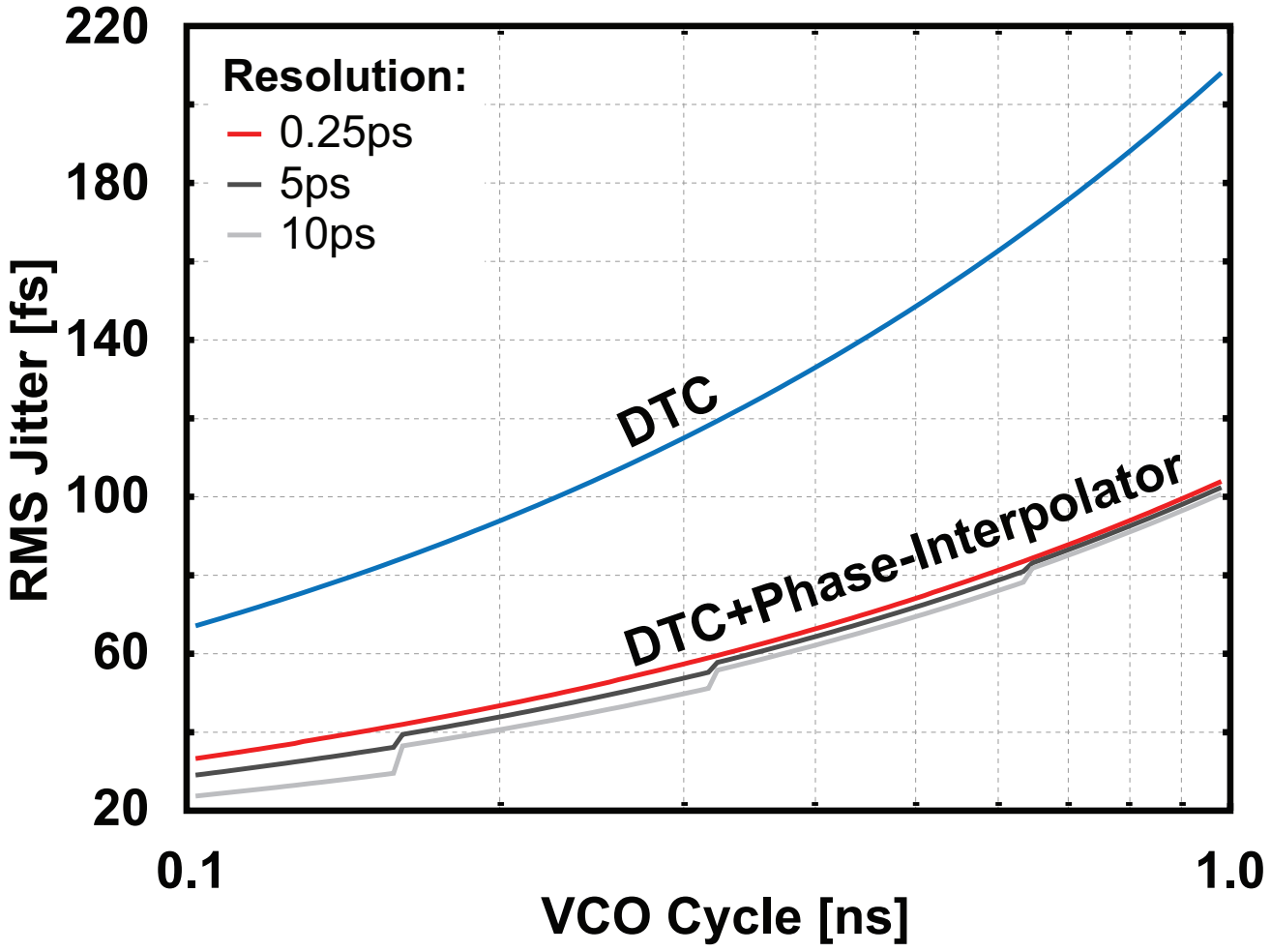
$$T_{DR,DTC} = {}^{T_{VCO}}/_{2^M}$$

Jitter Considerations



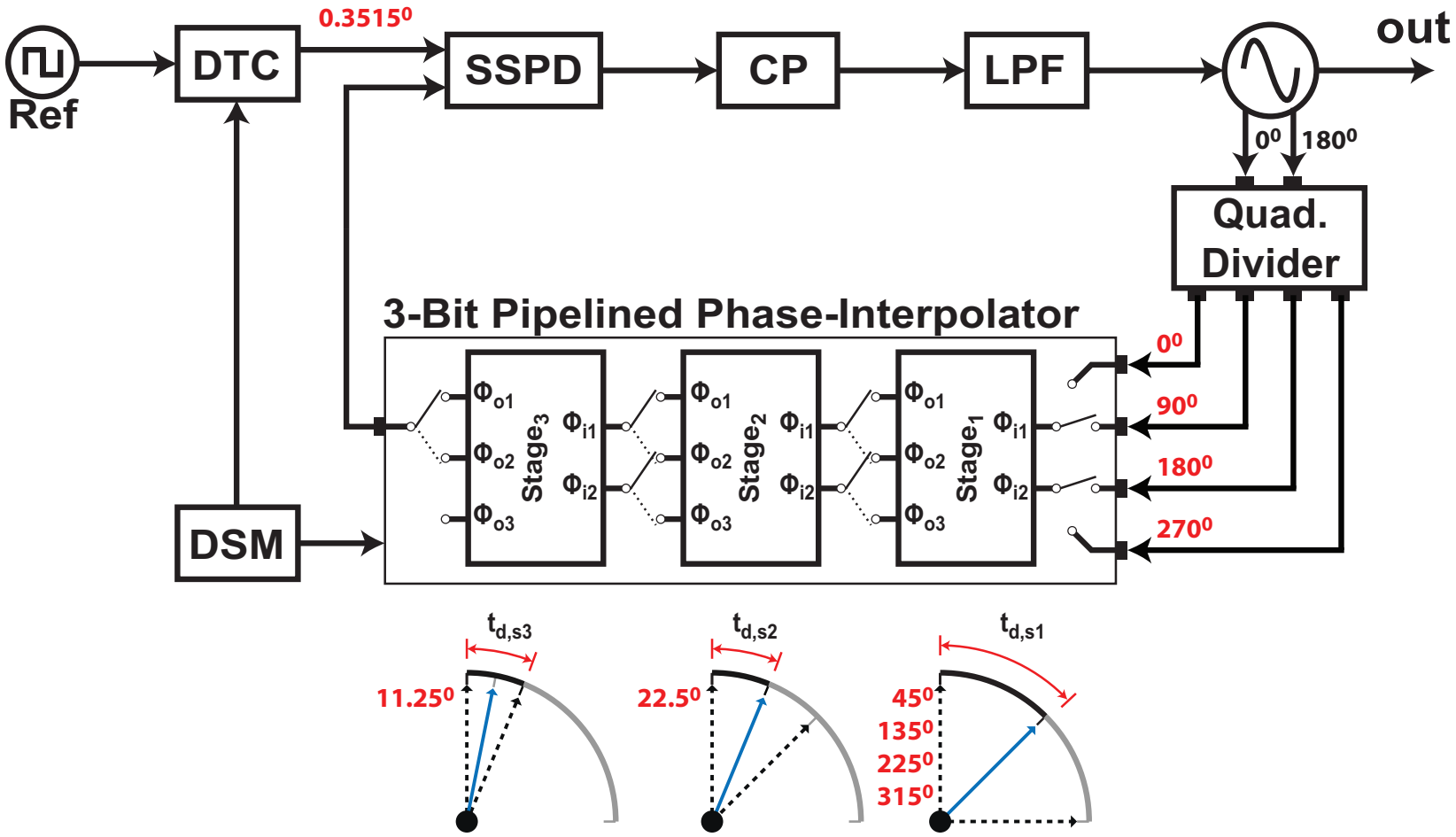
Proposed architecture reduces dynamic range requirement

Jitter Considerations



Proposed architecture minimizes jitter generation

Proposed FN-SSPLL Architecture



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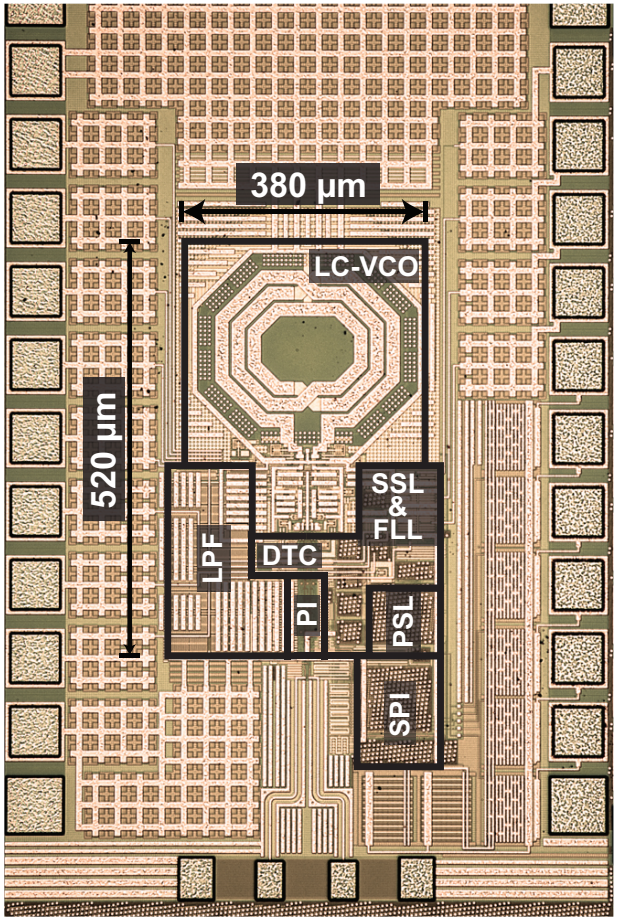
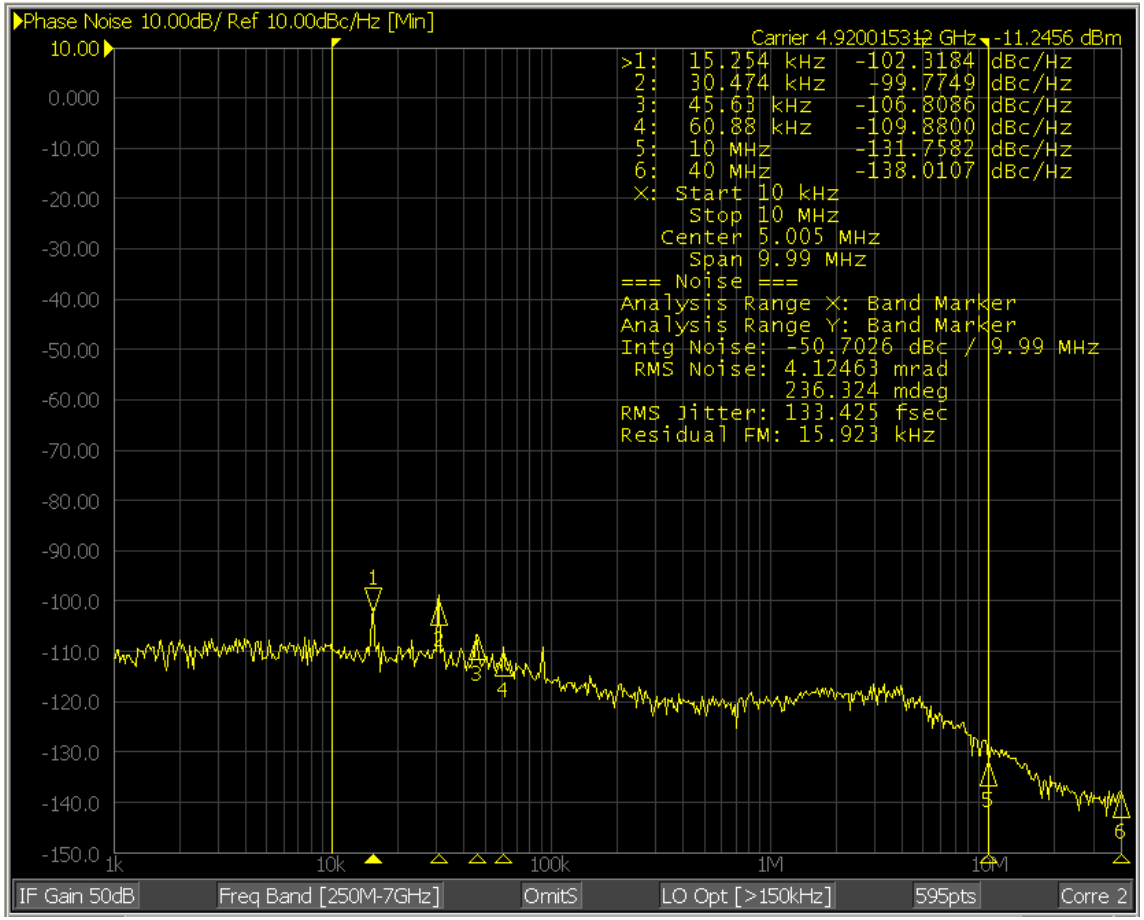
Experimental Results



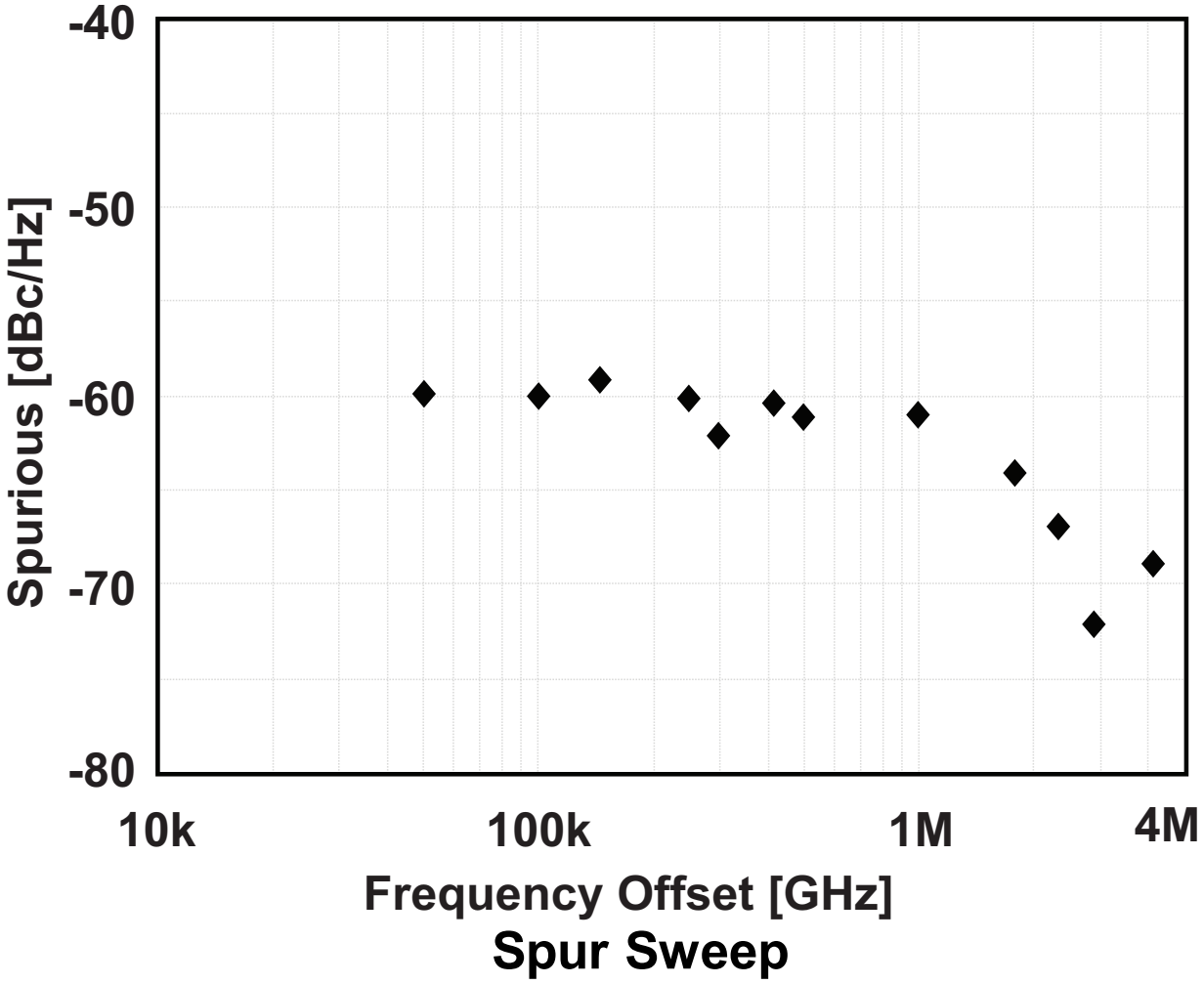
Chip Micrograph
65nm CMOS



Phase Noise

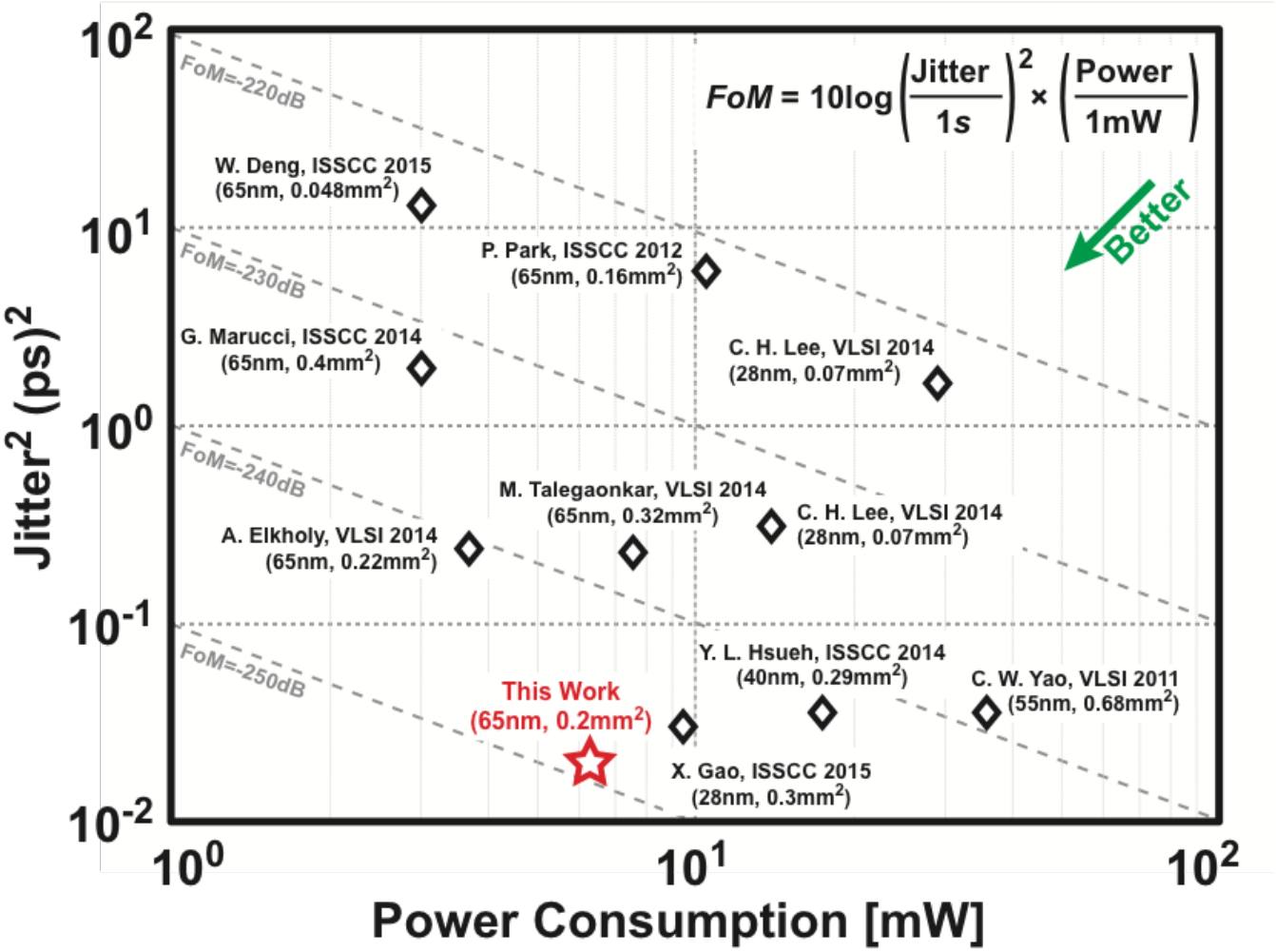
In-band phase noise of -120.3dBc/Hz is achieved at 500kHz

Experimental Results



Fractional spurs < 59dBc is achieved

FoM Comparison



The prototype achieves best reported FoM

Conclusion

- **A divider-less fractional-*N* PLL is proposed.**
  - **Uses a phase-interpolator and DTC**
  - **Lower jitter compared to conventional architecture**
  - **The pipelined phase-interpolator uses very low-power**
- **A prototype is manufactured in 65nm CMOS**
  - **Achieves -120.3dBc/Hz in-band phase noise**
  - **Fractional spurs are observed below -59dBc**
- **The proposed architecture achieves best in class performance without additional calibration.**