A 2.2 μW 15b Incremental Delta-Sigma ADC with Output-Driven Input Segmentation

B. Wang[1], M. K. Law[1], S. Mohamad[1] and A. Bermak[1,3]

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[1]Hong Kong University of Science & Technology
[2]University of Macau
[3]Hamad Bin Khalifa University

Applications

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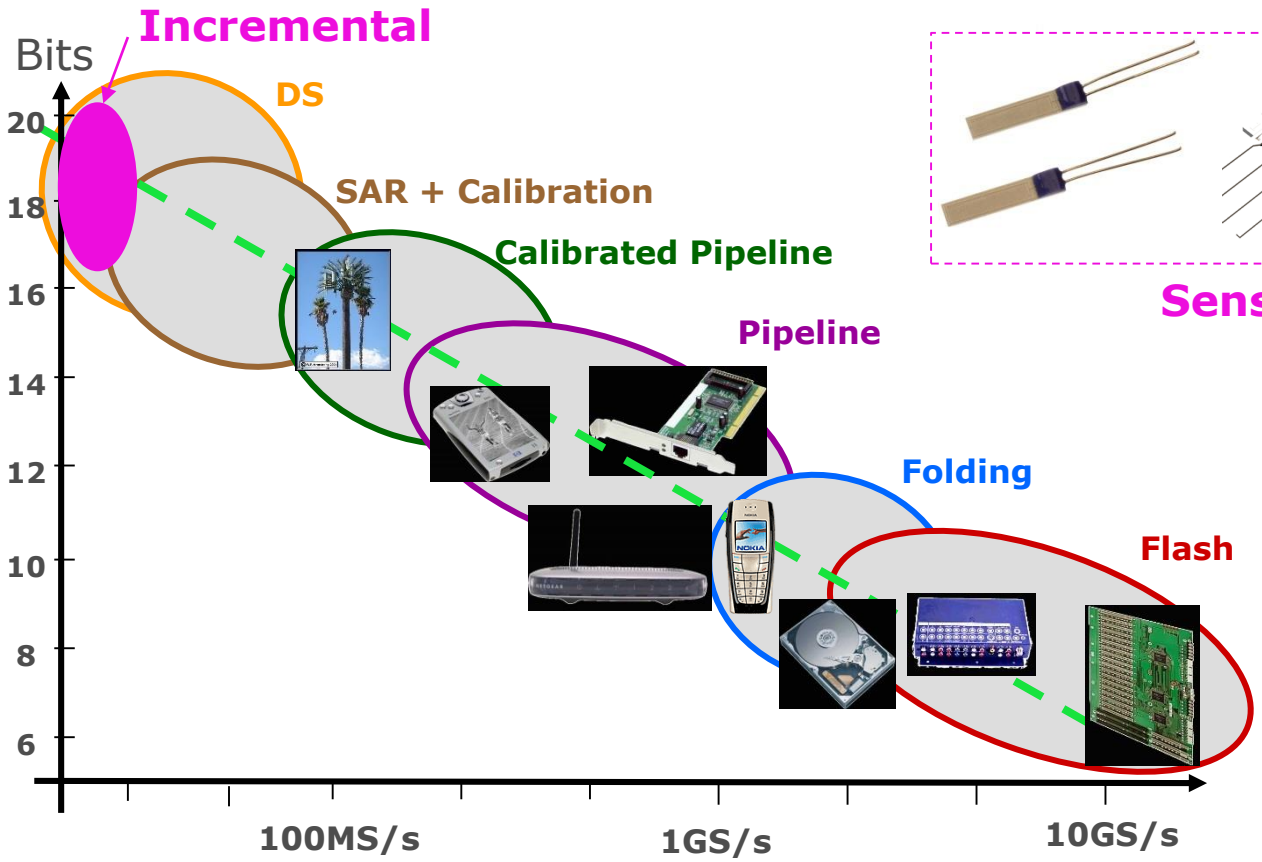
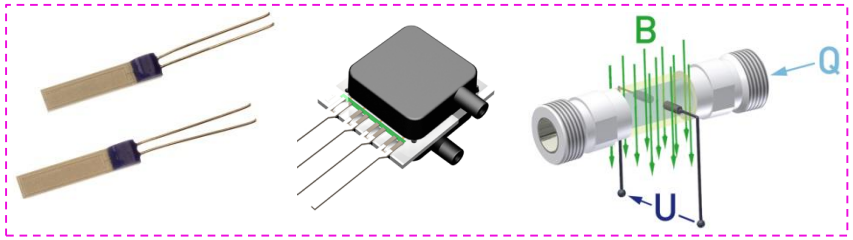
- Architecture vs. Speed and Resolution





Sensor Interfaces

- precision
- micro-power
- calibration-less

"Pipelined A/D Converters: The Basics "; A. Buchwald; Jun. 2015, HKUST Talk.

ΔΣ A/D Basics

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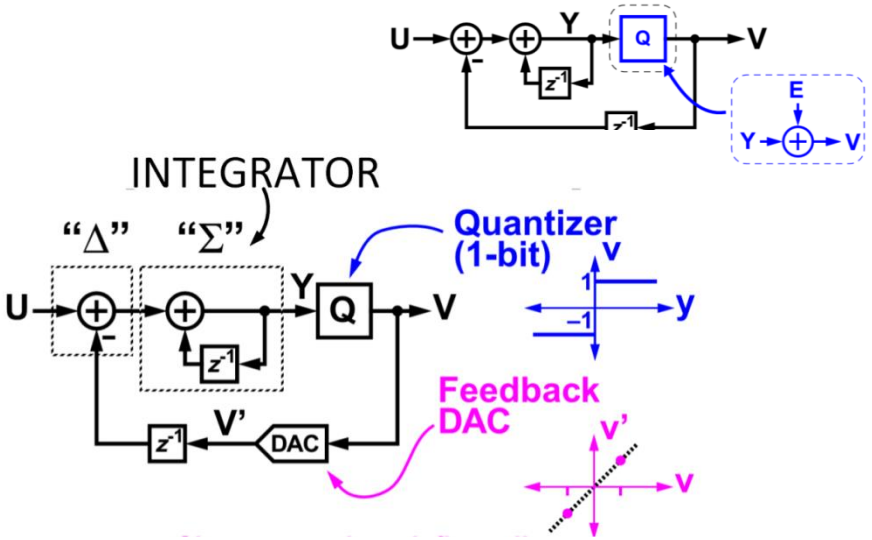
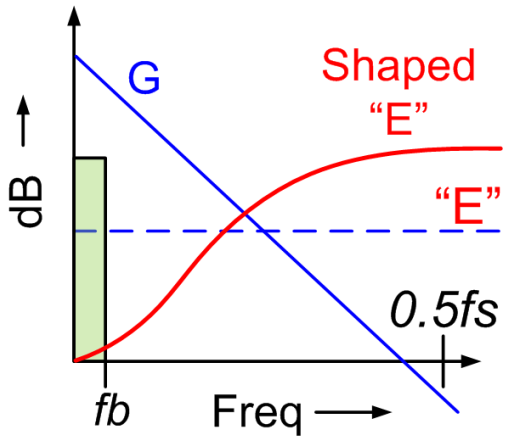
- ΔΣ data converter
  - Low speed, high resolution, tolerance to device imperfections
  - Oversampling, noise shaping



$$Y(z) = U(z) + (1 - Z^{-1})E(z)$$



- Easy to implement, (6L+3)dB SNR increase for every doubling in OSR

"Understanding Delta Sigma Data Converters"; R. Schreier , G. C. Temes; Oct. 2004 Wiley.

Incremental ΔΣ A/D

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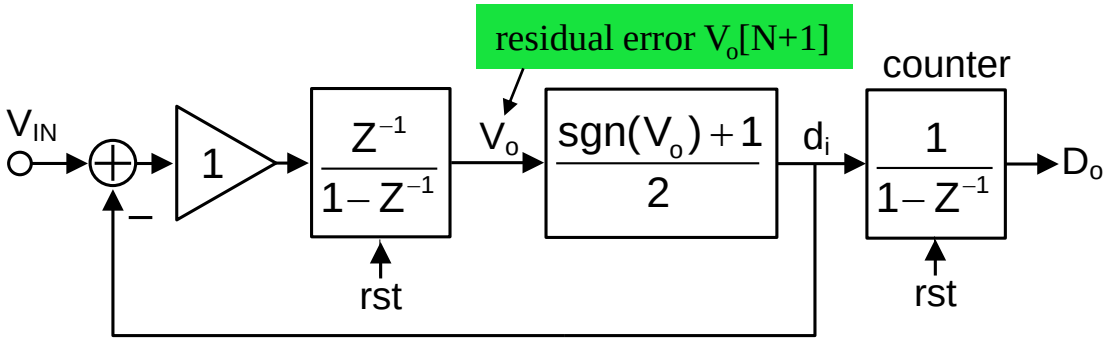
- Incremental A/D characteristics
  - Focus on absolute precision instead of spectral performance
  - Reset before every A/D conversion
  - Interested in residual error, time-domain analysis instead of frequency domain



$$N_{out} = 2^{n_{bit}}(V_{IN}/V_{REF}) + \varepsilon; \varepsilon \in [-1,1]$$

$(2^{n_{bit}}+1)$ cycles

Achieving Higher Energy Efficiency

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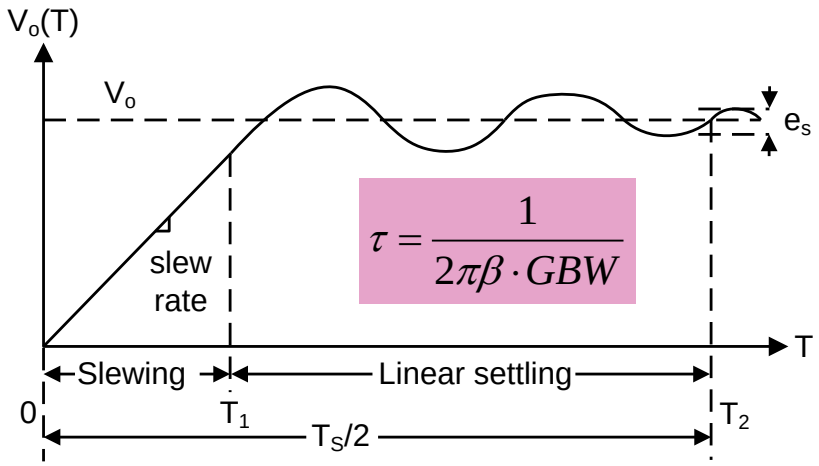
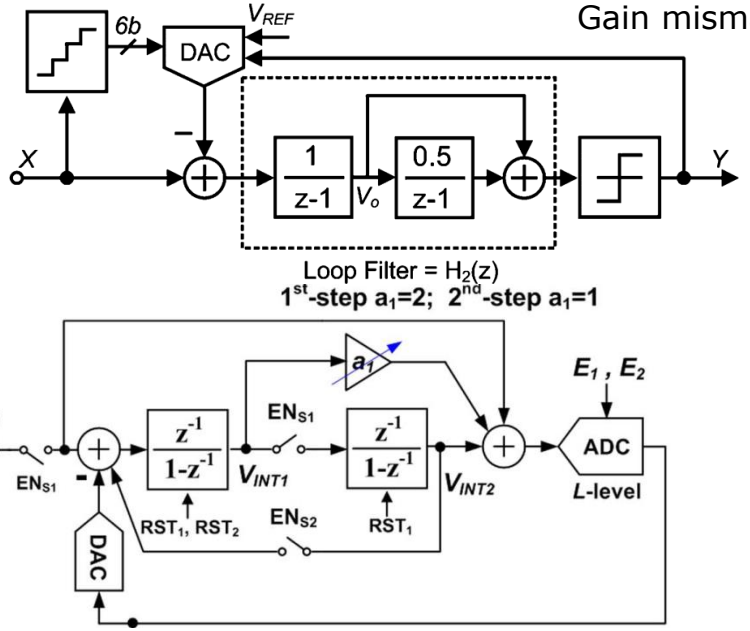
- At circuit level
  - class-AB, dynamic powered OTA, inverter, etc.
- At system level
  - high-order loop filter, multi-bit quantizer, multi-stage noise shaping-MASH, passive integrator, extended counting
  - 2-step conversion (i.e. zoom) → relaxed integrator



System & OTA design

Noise folding
Gain mismatch



Y. Chae, et. al, "A 6.3 μW 20 bit Incremental Zoom-ADC with 6 ppm INL and 1 μV Offset," IEEE J. Solid-State Circuits, vol. 48, no. 12, pp. 3019 - 3027, Dec. 2013.
Chia-Hung Chen, et. al, "A Micro-Power Two-Step Incremental Analog-to-Digital Converter," IEEE J. Solid-State Circuits, vol.50, no.8, pp.1796-1808, Aug. 2015

Proposed Topology

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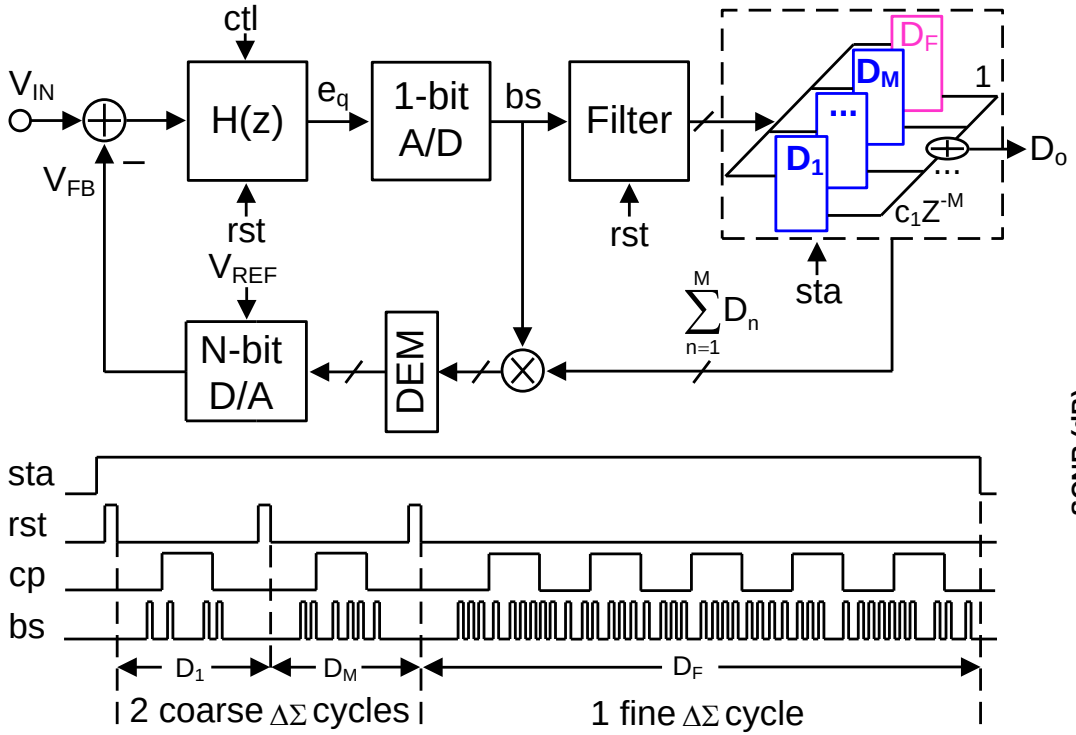
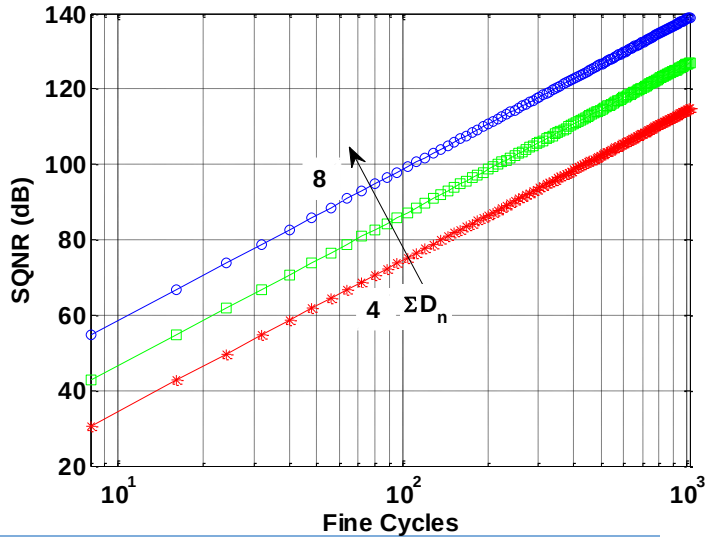
- Sequential quantization
  - Consists only of oversampling modulator → relaxed input filtering
  - Same hardware → matched gain between coarse/fine cycle



$$SQNR = 10\log\left(\frac{V_{REF}^2/8}{E^2/12}\right)$$

$$\approx 2*20\log M_3 - 21.6$$

$$+20\log(a_1 b_1 * 2^{D1+D2+\ldots+DM})$$



Guard Band

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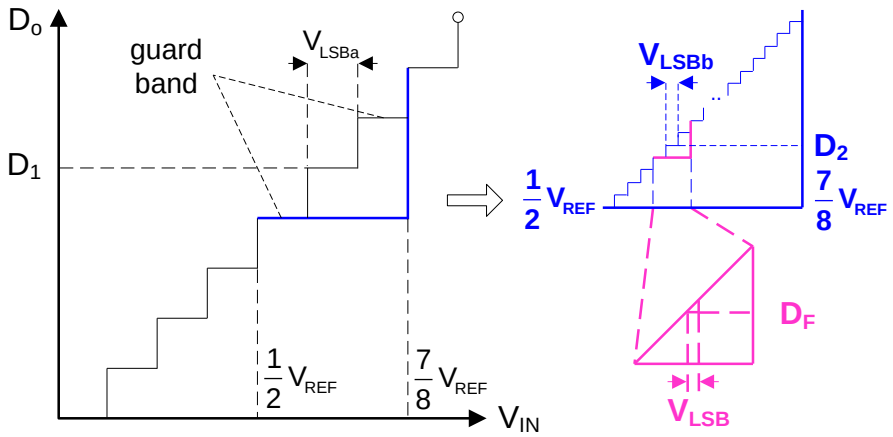
- +/-1 LSB guard band to protect INL induced transition error in MSB



$$V_1[M] = a_1\left\{\sum_{k=0}^{M}(V_{IN}[k] - d_i[k]V_{REF})\right\}$$

$$V_2[M] = a_1 b_1 \sum_{j=0}^{M-1}\sum_{k=0}^{j}(V_{IN}[k] - d_i[k]V_{REF}) - b_1\sum_{j=0}^{M-1} d_i[j]V_{REF}$$

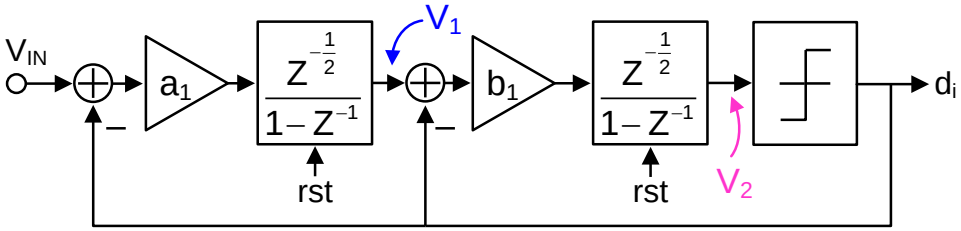
$$\Downarrow$$

$$\in [-V_{REF}, +V_{REF}]$$

$$\frac{V_{IN}}{V_{REF}} = \frac{2!}{M(M+1)}\sum_{j=0}^{M-1}\sum_{k=0}^{j} d_i[k] + \frac{1}{a_1}\sum_{j=0}^{M-1} d_i[j]$$

$$\Downarrow$$ **Final Quantization Error**

$$E = \frac{4}{M_3(M_3+1)}\,\frac{1}{a_1 b_1}\,\frac{3V_{REF}}{2^{D1+D2+\ldots D_M}}$$



I-A/D Modulator

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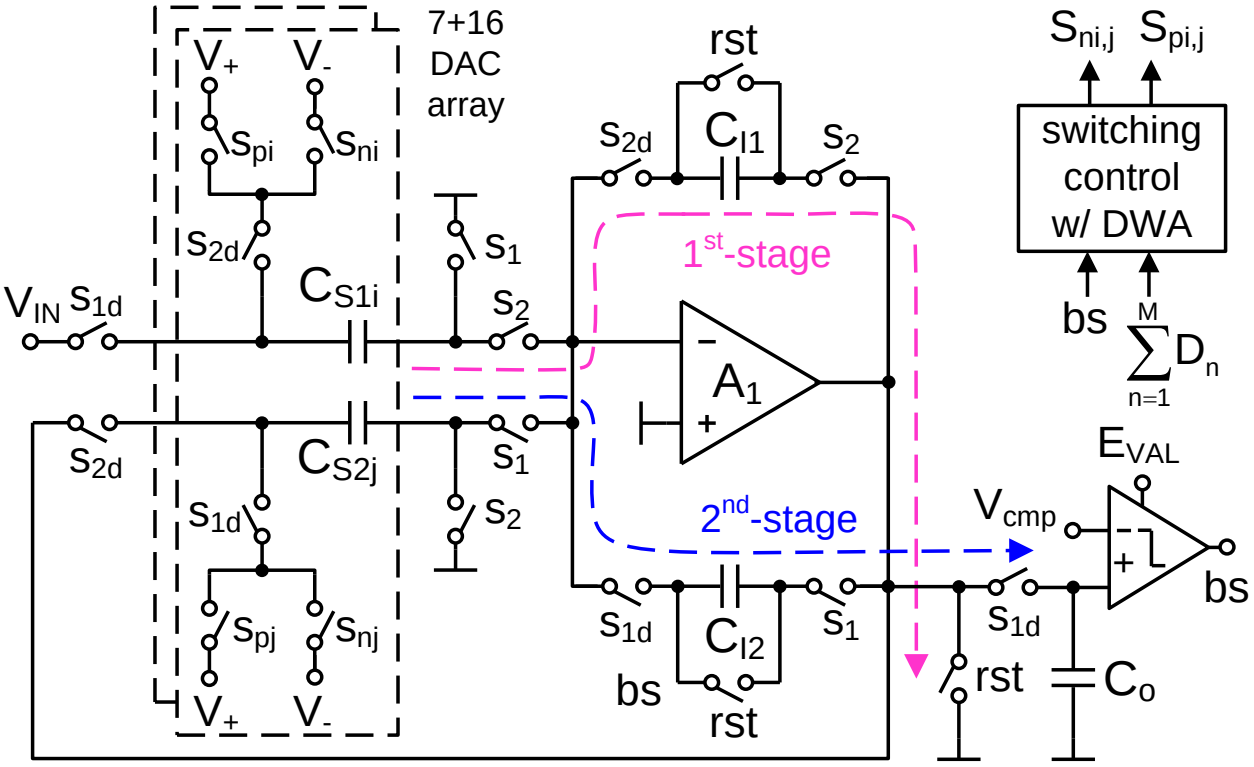
- Integrator time-multiplexing
  - w/o CDS, low frequency opamp chopping
  - Half-delay, 2nd-order ΔΣ to suppress limit cycles



Prototype & Measurement

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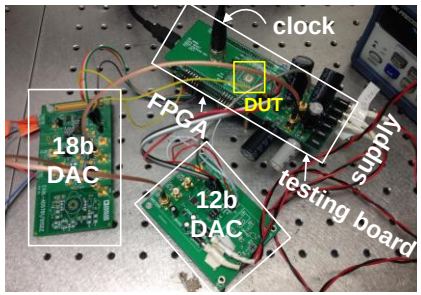
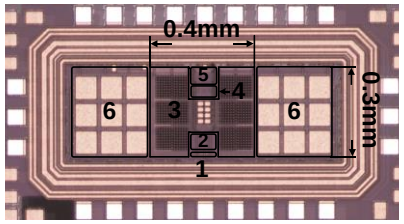
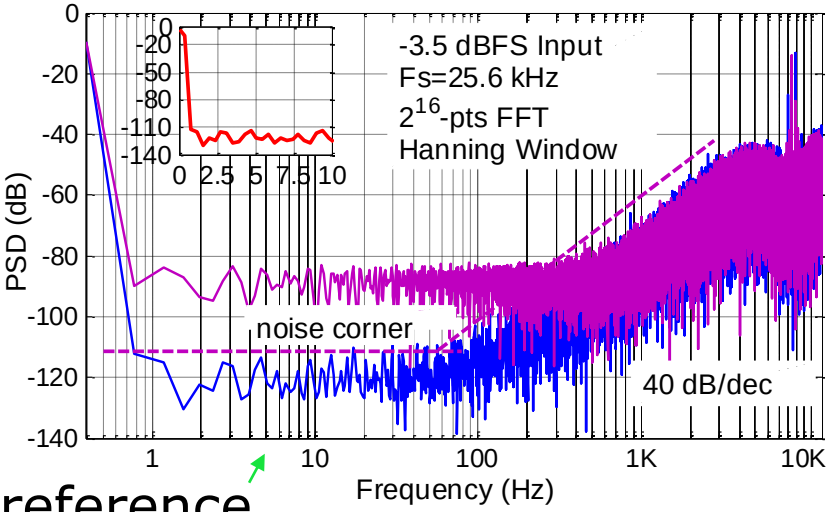
- 0.18μm CMOS, 0.12mm² area



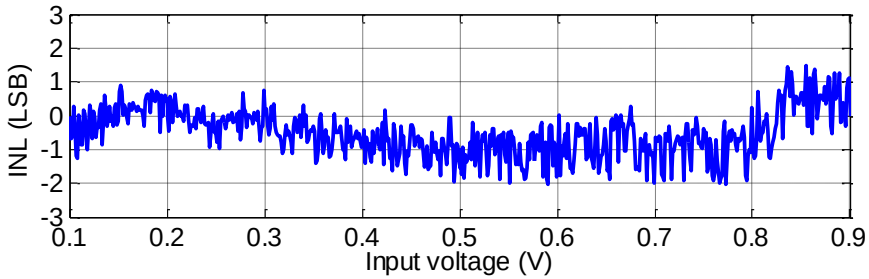


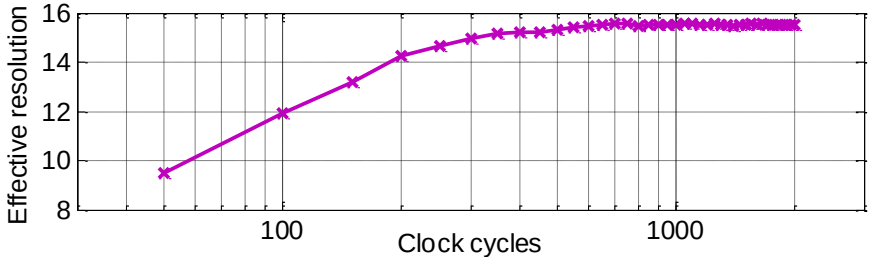
1. bias generator; 2. amplifier;
3. $C_{S1,2}$, $C_{I1,2}$, C_0 array & switches
4. comparator; 5. clk, ctl generator; 6. filtering cap

Test setup: 1.8V supply
25.6kHz clock
18b DAC for input sweep
12b DAC for biasing
Spartan 3 for signal conditioning



- -3.5dBFS (0.95V) with 1.4V reference





- Input sweep, x8 averaging at each point

Performance Summary

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- Comparison with precision ΔΣ incremental A/D

	[V. Quiqu.] JSSC, 06	[A. Agah] JSSC, 10	[C.C. Lee] TCASI, 10	[Y. Chae] JSSC, 13	[C. Chen] ISSCC, 13	**This work**
Topology	ΔΣ	ΔΣ+SAR	ΔΣ+cyclic	SAR+ΔΣ	ΔΣ	ΔΣ
Process	0.6μm	0.18μm	0.18μm	0.16μm	0.16μm	**0.18μm**
Chip area	2.08mm^2	3.5mm^2	0.5mm^2	0.37mm^2	0.45mm^2	**0.12mm^2**
Supply	3V	1.8V	2	1.8V	1V	**1.8V**
Power	300μW	38.1mW	48mW	6.3μW	20μW	2.16μW
T_{conv}	66.7ms	1ms	43.5μs	40ms	<0.75ms	**11.7ms**
Input range	6V	2V	3.6V	1.8V	0.7V	**0.8V**
[a]SNR_{max}	120dB	86.3dB	72dB	119.8dB	81.9dB	**85dB**
INL (LSB)	+/-8.4 @22b	+/-1 @14b	<2 @14	+/-6.3 @20b	-0.6/+0.4 @14b	**-2/+1.5 @15b**
[b]FoM_s	164.0dB	161.3dB	156.8dB	182.7dB	157.1dB	**158dB**
Calibration	**No**	**Yes**	**Yes**	**Yes**	**No**	**No**

$$^{a}SNR_{max} = 20 \cdot \log\left(\frac{Input\_range}{2\sqrt{2}\langle Input\text{-}referred\text{-}noise}\right); ^{b}FoM_s = SNR_{max} + 10 \cdot \log\left(\frac{1}{power \cdot T_{conv} \cdot 2}\right)$$

Thermal FoM