1S-7

A Variable-Voltage Low-Power Technique for Digital Circuit System

outline

- CK-Vdd

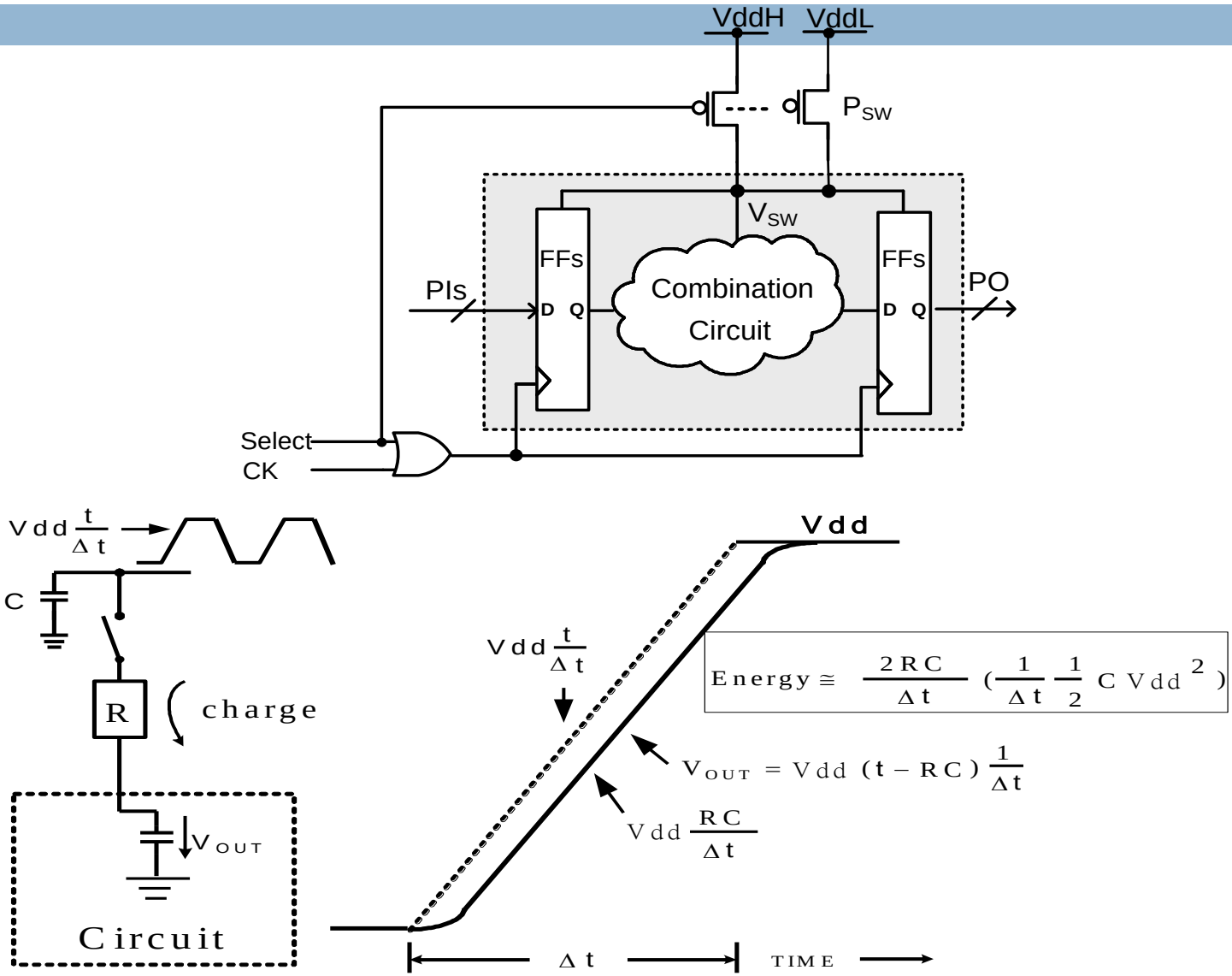
a. Propose CKVdd Circuit Structure

b. Frequency Duty Cycle Adjust (FDCA)

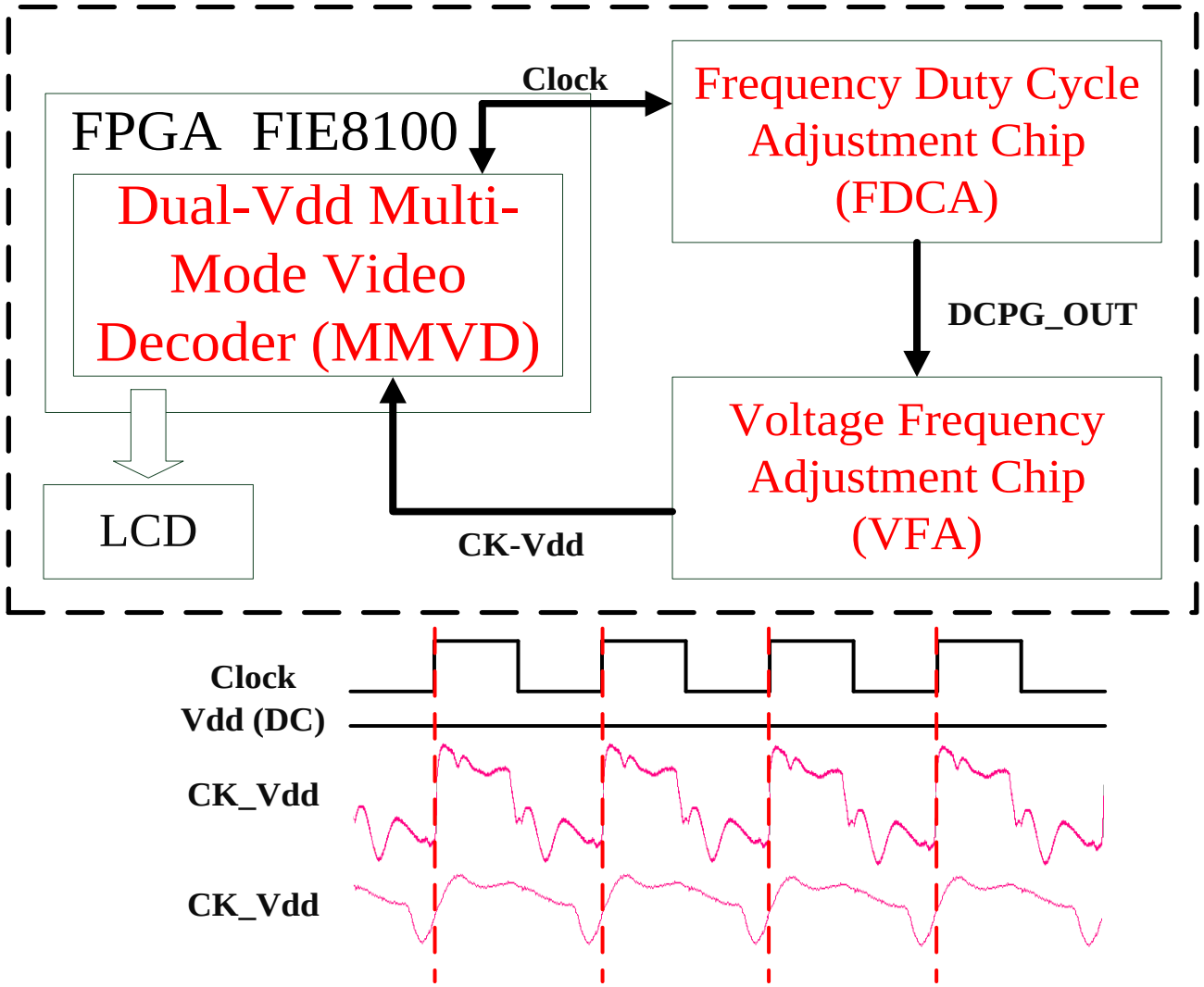
c. Voltage Frequency Adjustment (VFA)

- Chip Measurement
- Conclusion & Future Work

Propose CK-Vdd Circuit Structure

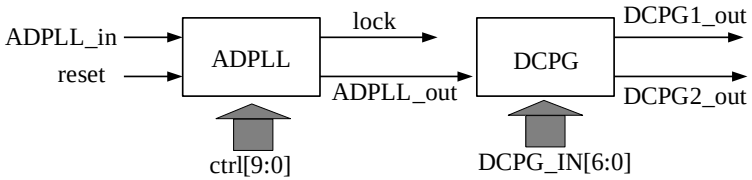


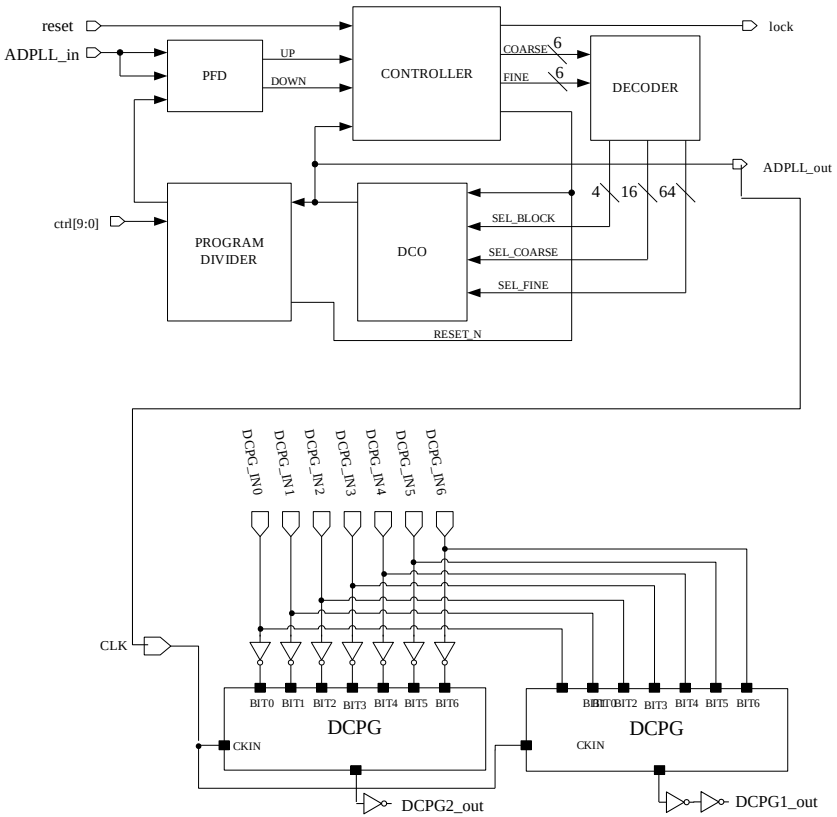
Implemented Video Decoder System based on CK-Vdd Structure



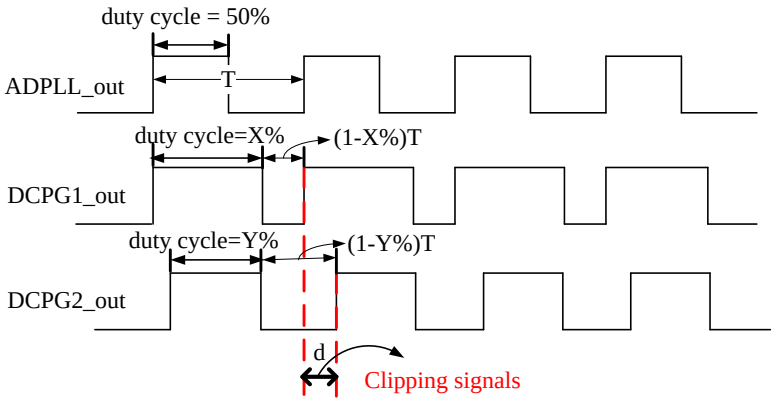
Frequency Duty Cycle Adjustment (FDCA) Chip

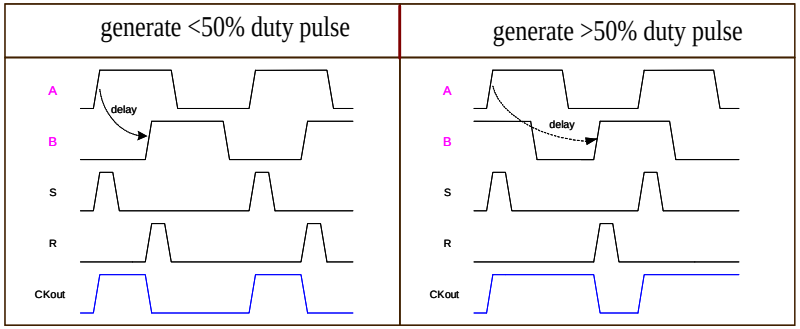
5





FDCA circuit structure

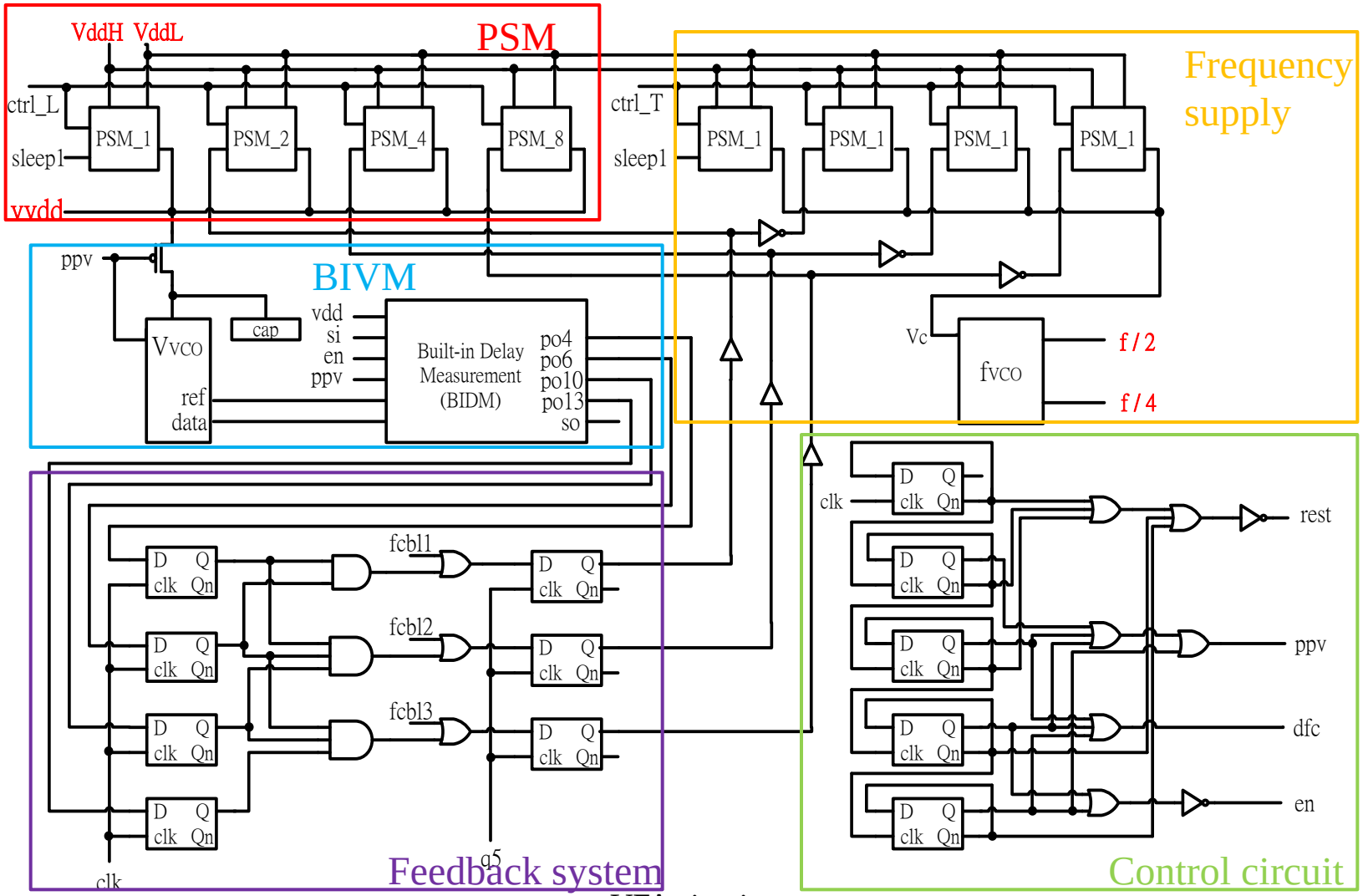




Adjusting clock duty cycle

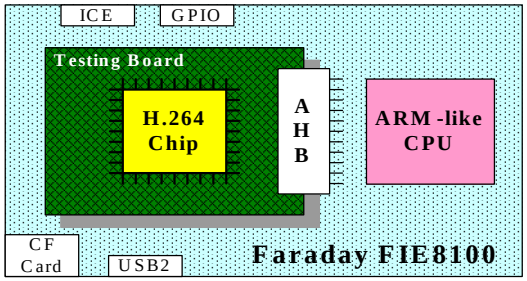
All-Digital Phase-Locked Loop (ADPLL)
Digital Controlled Pulse Generator (DCPG)

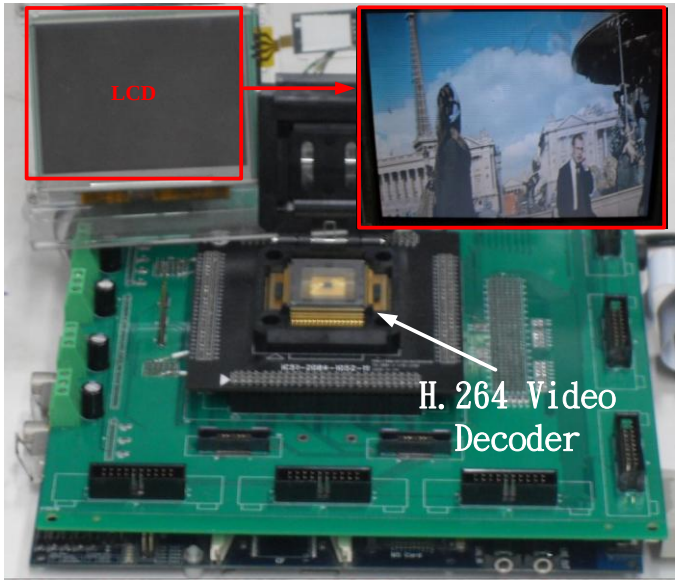
Detailed Circuit Design in VFA Chip



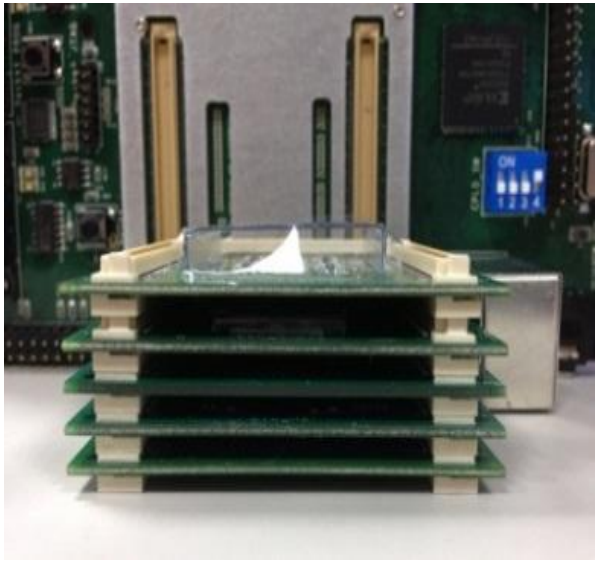
VFA circuit structure

System Validation



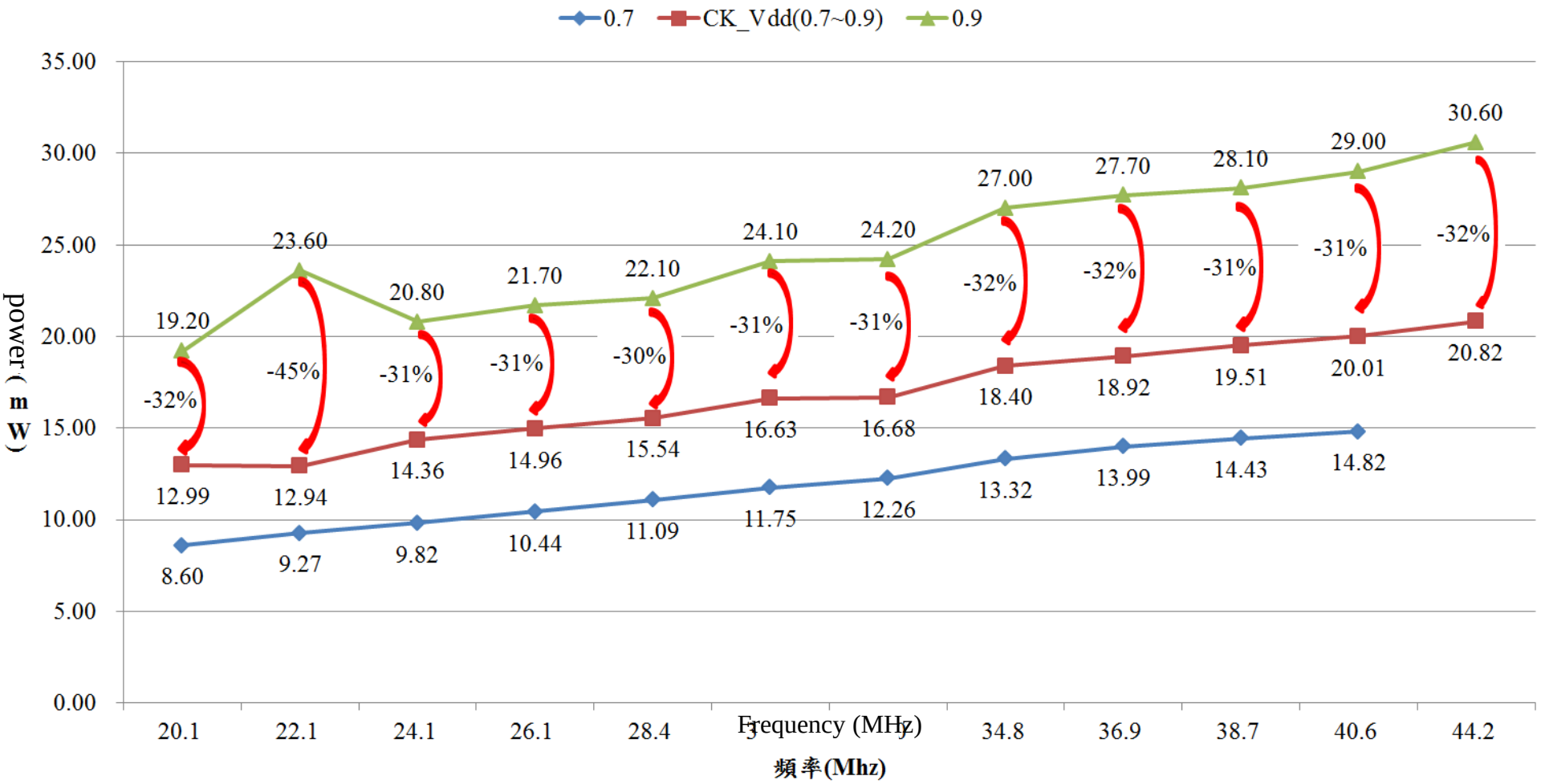


An H.264 Video Decoder implemented by the proposed technology



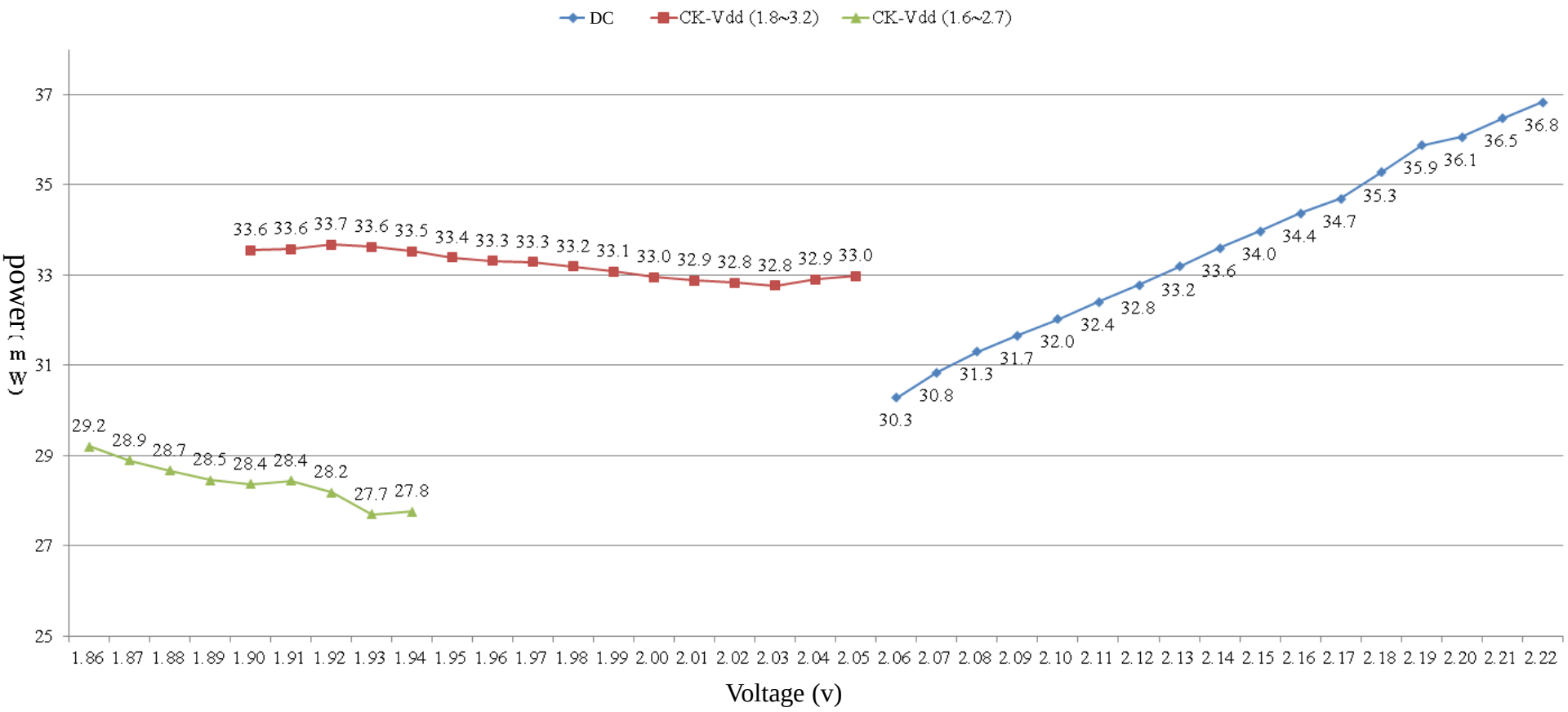
The proposed system implemented in a 3D MorPack

Proposed Chip Measurement when Doing H.264 Video Decoding



Using H.264 decoder as the load and comparing the power consumption of the design in DC (1v) and CK-Vdd supply

Proposed Chip Measurement when Doing Video Display



Using a camera as the load and comparing the power consumption of the cases using DC and CK-Vdd voltage supply

Conclusion

1. 1.We present a system that can freely adjust voltage and frequency. It can adjust different voltages for each operation case.
2. 2.Using H.264 as the load, the proposed system can save 45% power consumption when CK-Vdd is equal to 0.7v-0.9v.
3. 3.Using a camera as the load, The comparisons of using DC-voltage and CK-Vdd techniques, it is interesting the CK-Vdd technique allows a circuit system work by lower supply voltages. The CK-Vdd supply voltage can be degraded to 1.86V~1.94V, while the DC-Vdd is 2.06V~2.22V. There are 8%~ 24% power reductions.
4. 4.The power consumption cannot exponentially increased when the supply voltage is increased. The design is all digital circuits so that they can be easily integrated in a chip.