A Variable-Voltage Low-Power Technique for Digital Circuit System
outline

- CK-Vdd
  a. Propose CKVdd Circuit Structure
  b. Frequency Duty Cycle Adjust (FDCA)
  c. Voltage Frequency Adjustment (VFA)
- Chip Measurement
- Conclusion & Future Work
Propose CK-Vdd Circuit Structure

\[
\begin{align*}
V_{\text{dd}} &= \frac{t}{\Delta t} \\
C &= \text{charge} \\
\text{Circuit} &= V_{\text{OUT}} \\
\Delta t &= \text{TIME}
\end{align*}
\]

Energy \approx \frac{2RC}{\Delta t} \left( \frac{1}{\Delta t} \frac{1}{2} CV_{\text{dd}}^2 \right)

\[
V_{\text{OUT}} = V_{\text{dd}} (t - RC) \frac{1}{\Delta t}
\]

\[
V_{\text{dd}} \frac{RC}{\Delta t}
\]
Implemented Video Decoder System based on CK-Vdd Structure
Frequency Duty Cycle Adjustment (FDCA) Chip

ADPLL_in → ADPLL → lock → ADPLL_out → DCPG → DCPG1_out → DCPG2_out

reset

ctrl[9:0]

DCPG_IN[6:0]

program divider

DCO

SEL_FINE

SEL_COARSE

SEL_BLOCK

PFD

controller

DCPG

reset

lock

ADPLL_out

DCPG1_out

DCPG2_out

Controlling signals

duty cycle = 50%

T

(1-X%)T

(1-Y%)T

generate <50% duty pulse
generate >50% duty pulse

Clipping signals

ADPLL_out

DCPG1_out

DCPG2_out

Clipping signals

duty cycle = 50%

T

(1-X%)T

(1-Y%)T

generate <50% duty pulse
generate >50% duty pulse

Clamping signals

Adjusting clock duty cycle

All-Digital Phase-Locked Loop (ADPLL)
Digital Controlled Pulse Generator (DCPG)
Detailed Circuit Design in VFA Chip

Frequency supply

Built-in Delay Measurement (BIDM)

VFA circuit structure
System Validation

An H.264 Video Decoder implemented by the proposed technology

The proposed system implemented in a 3D MorPack
Proposed Chip Measurement when Doing H.264 Video Decoding

Using H.264 decoder as the load and comparing the power consumption of the design in DC (1v) and CK-Vdd supply
Proposed Chip Measurement when Doing Video Display

Using a camera as the load and comparing the power consumption of the cases using DC and CK-Vdd voltage supply.
Conclusion

1. We present a system that can freely adjust voltage and frequency. It can adjust different voltages for each operation case.

2. Using H.264 as the load, the proposed system can save 45% power consumption when CK-Vdd is equal to 0.7v-0.9v.

3. Using a camera as the load, The comparisons of using DC-voltage and CK-Vdd techniques, it is interesting the CK-Vdd technique allows a circuit system work by lower supply voltages. The CK-Vdd supply voltage can be degraded to 1.86V~1.94V, while the DC-Vdd is 2.06V~2.22V. There are 8%~ 24% power reductions.

4. The power consumption cannot exponentially increased when the supply voltage is increased. The design is all digital circuits so that they can be easily integrated in a chip.