Sub-threshold VLSI Logic Family Exploiting Unbalanced Pull-up/down Network, Logical Effort and Inverse-Narrow-Width Techniques

ID: 1S-8

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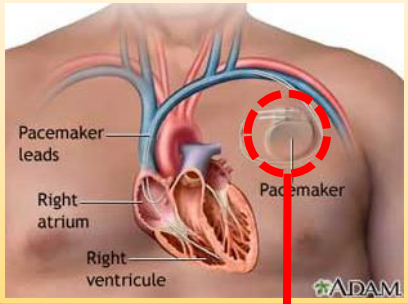
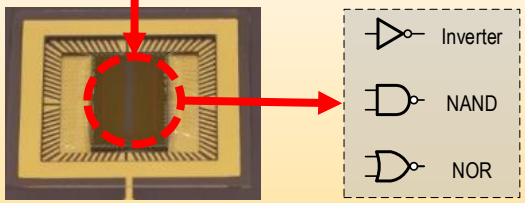
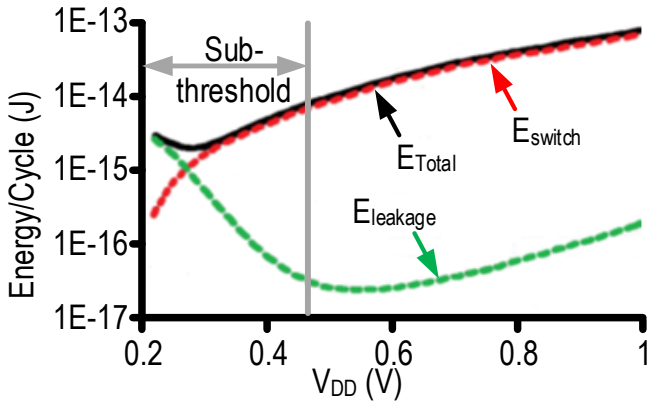
Background and Motivation



low-power dissipation & durable battery life



operations to acquire minimum energy consumption



- Minimum energy solution

$$E_{switch} = C_{eff}V_{DD}^2 \propto V_{DD}^2$$

$$E_{leakage} = W_{eff}I_{leakage}V_{DD}t_dL_{DP} \propto V_{DD}$$

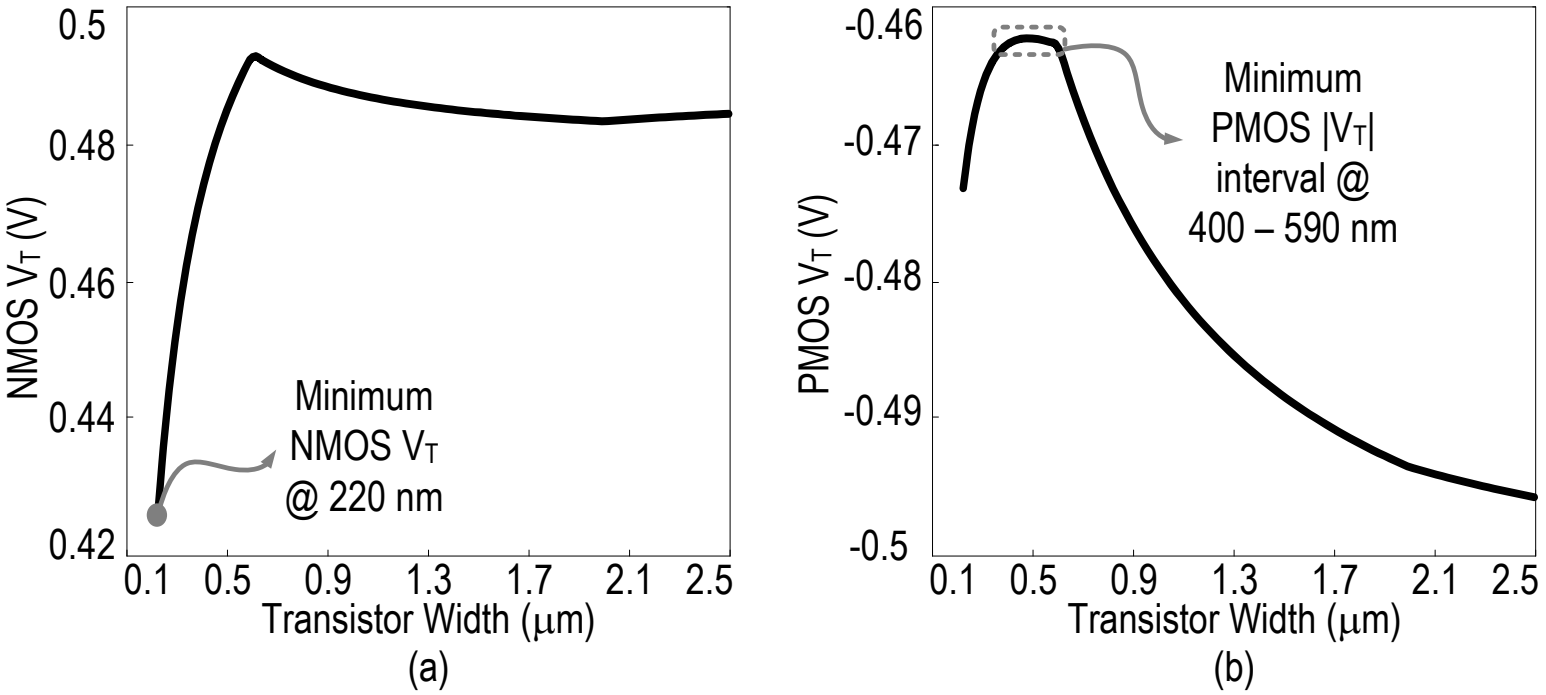
$$E_{Total} = E_{switch} + E_{leakage} \propto V_{DD}^2$$

➢ **Problems: sub-optimal energy efficiency; large silicon area**

➢ **Solutions: sub-threshold logic; low computational cost algorithm**

(circuit level) (system level)

Inverse-Narrow-Width Effect

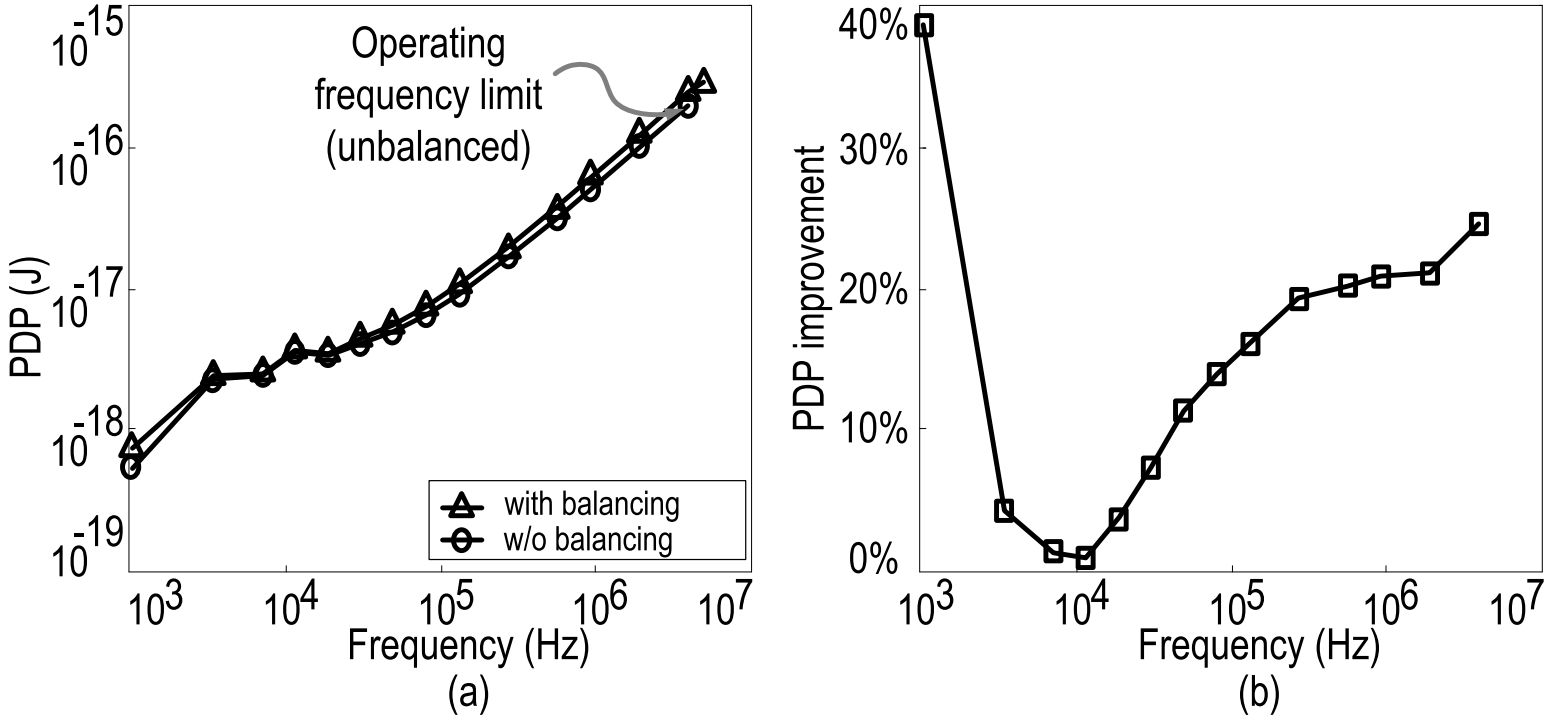


(a) NMOS, (b) PMOS VT vs. transistor width @ 0.3 V

$$I_{sub} = I_0 \cdot \mu_{eff} \cdot \frac{W}{L} \cdot e^{\frac{V_{GS}-V_T+\eta V_{DS}}{nV_{th}}} \cdot \left(1 - e^{-\frac{V_{DS}}{V_{th}}}\right)$$

$$\mu_{eff} \propto \frac{1}{V_T} \qquad t_d = \frac{\kappa V_{DD} C_L}{I_{sub}}$$

Unbalanced Network

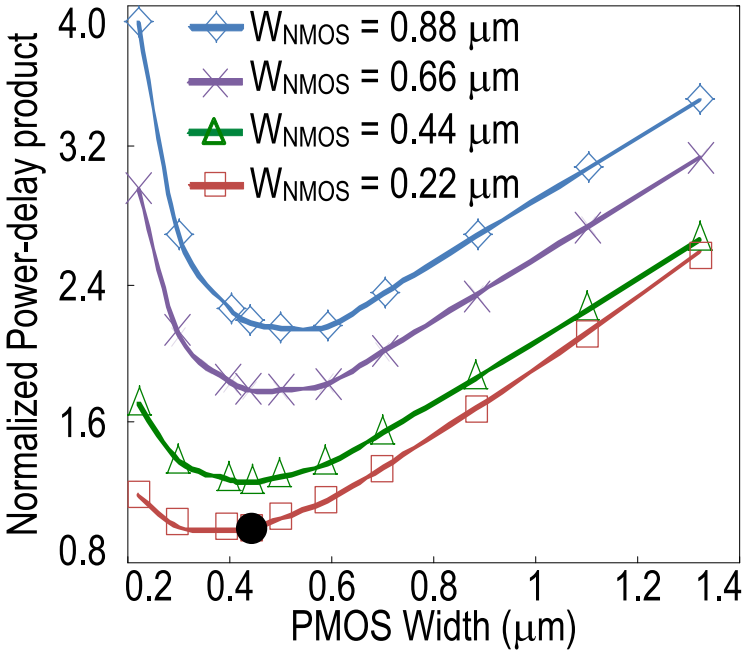


(a) PDP, and (b) PDP improvement of a reference inverter (FO4 loading) with balanced (5/1) and unbalanced (2/1) networks vs. freq. @ 0.3 V

- Balanced networks
  - P/N ratio (typical): 5/1.
  - Energy sub-optimized
  - Full operating freq. range

- Unbalanced networks
  - P/N ratio (typical): < 5/1.
  - Energy-optimized
  - Low-to-moderate operating freq.

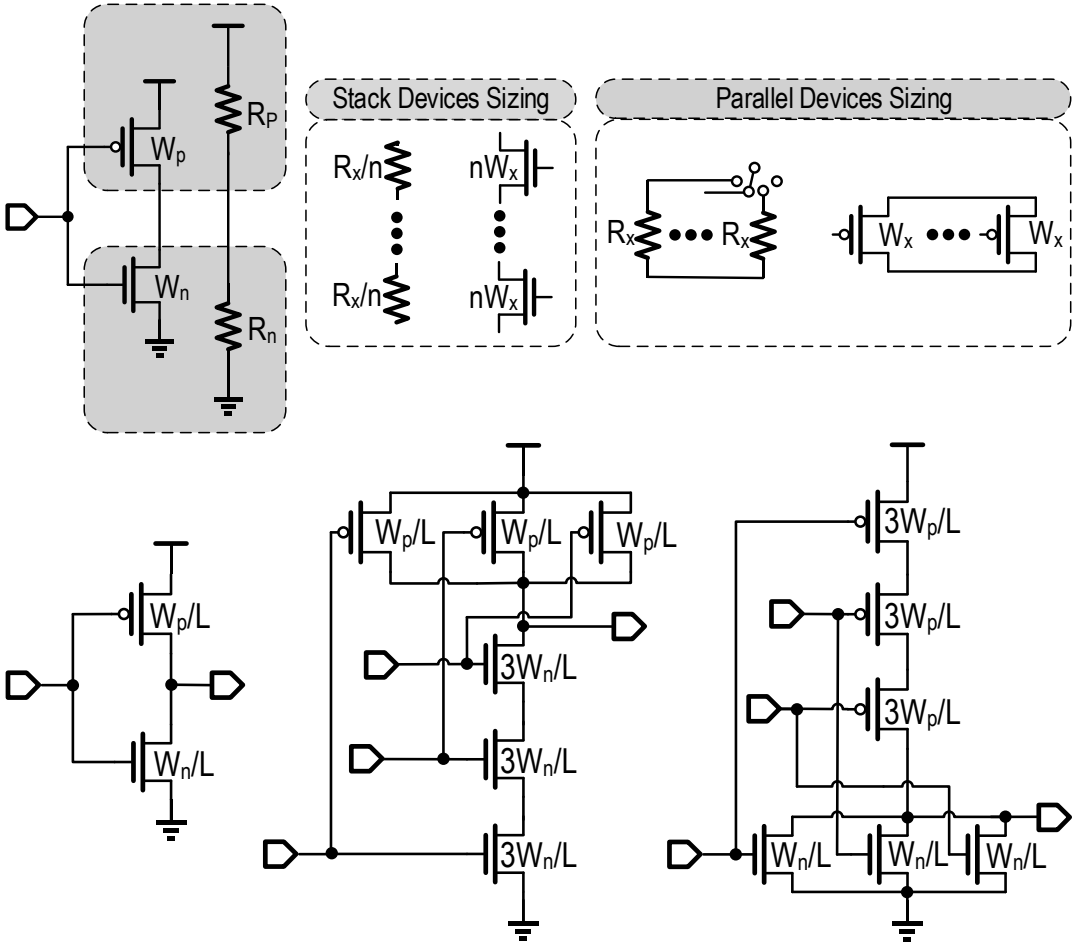
Single Stage Gates Design



•PDP @ various pMOS/nMOS width (Inverter)

- **Minimum energy solution**
- W_p = 420 nm; W_n = 220 nm.
- NAND and NOR scaling.

Resistor Model Derivatives



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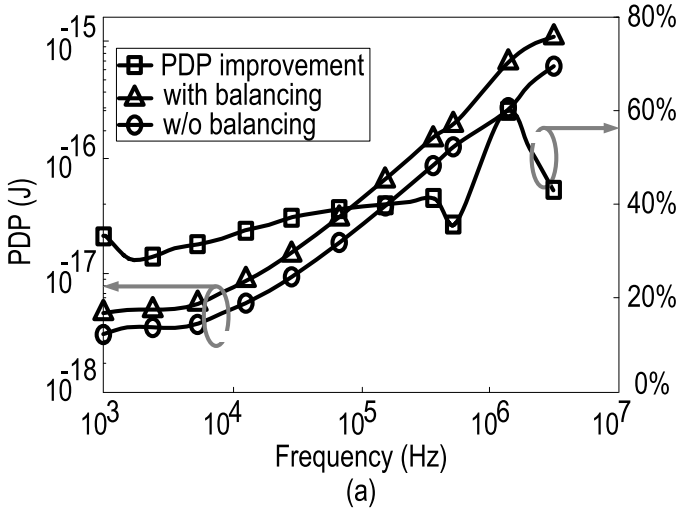
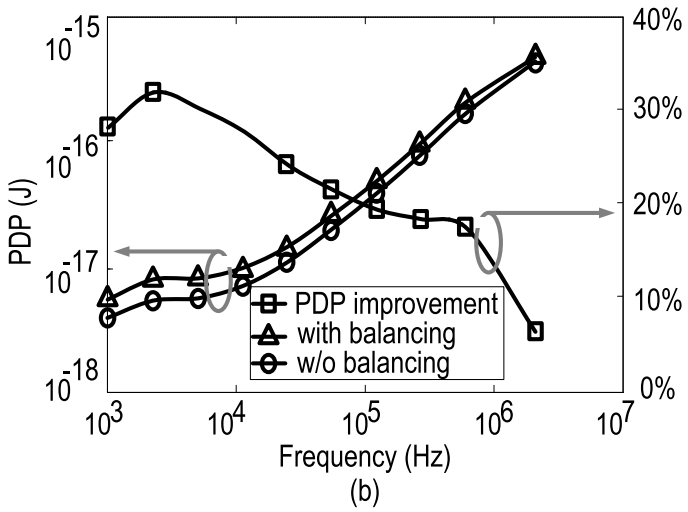
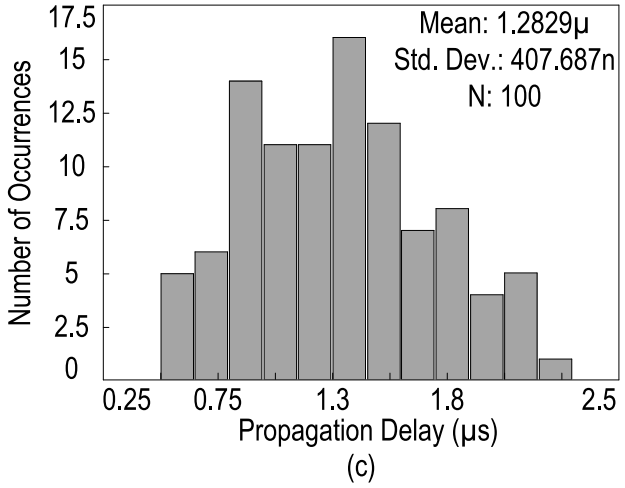
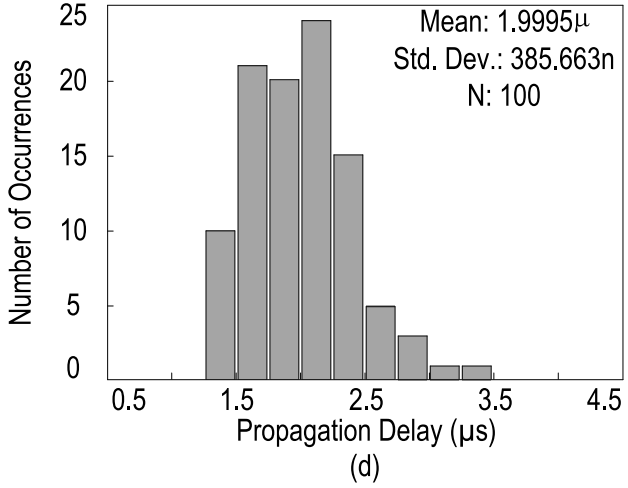
Single Stage Gates Design



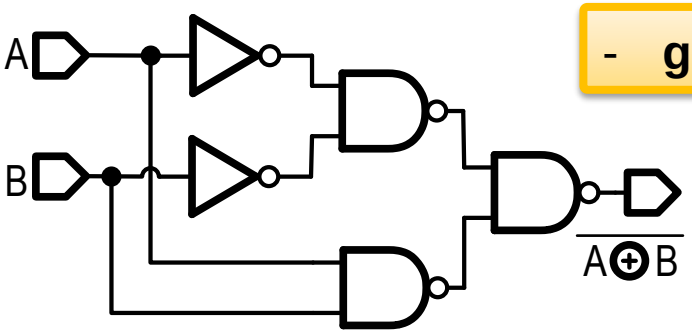






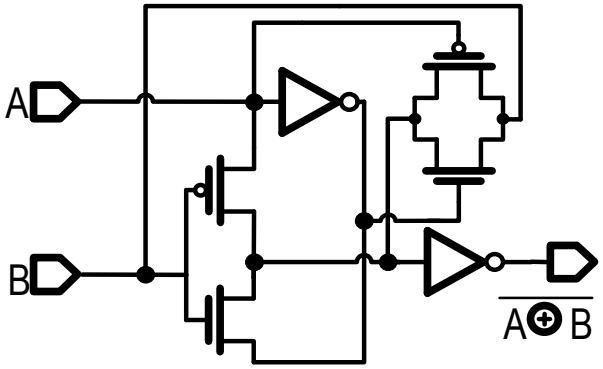
- Power-delay product of (a) NAND3, (b) NOR3 with balanced and unbalanced network vs. freq. @ 0.3 V
- 100 times Monte-Carlo simulation of (c) NAND3; (d) NOR3 for delay characterization @ 0.3 V

Multi-stage Gates Design



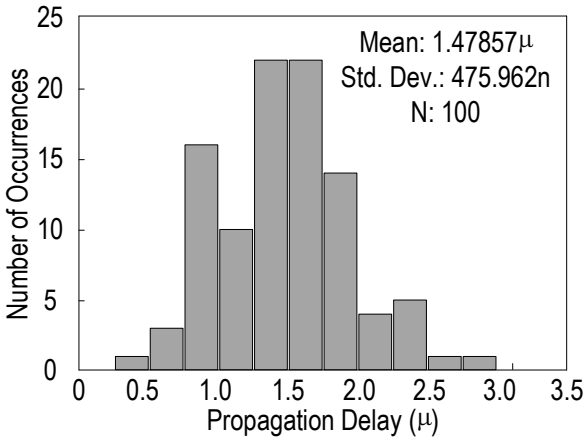
- g: 11.

- g: 4.

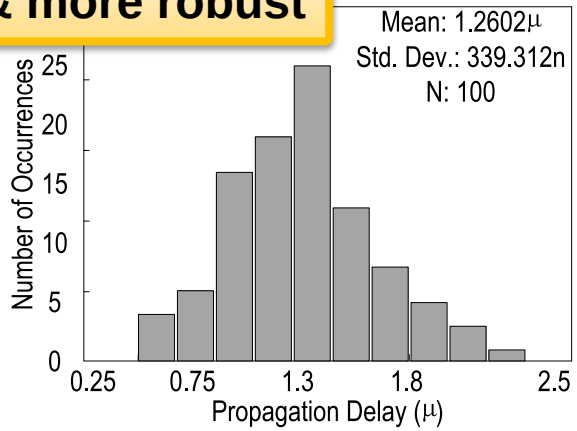


- **Logical effort (major criteria)**

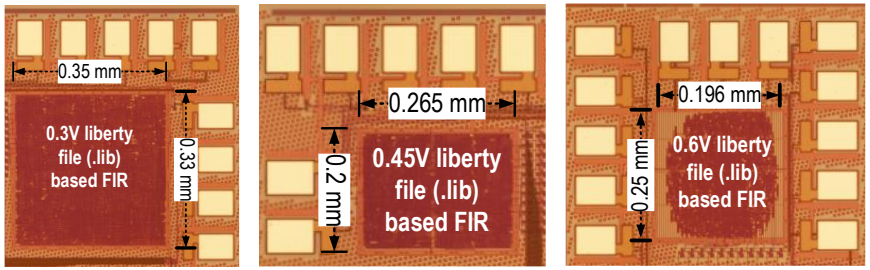
$$g = \frac{\sum C_i}{C_{inv}} = \frac{C_b}{C_{inv}} \xrightarrow{\text{L Fixed}} g = \frac{\sum W_i}{W_{inv}} = \frac{W_b}{W_{inv}}$$

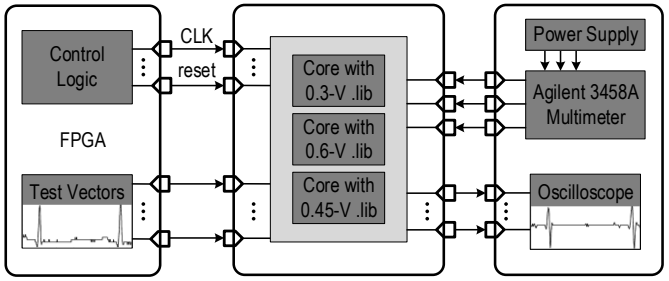


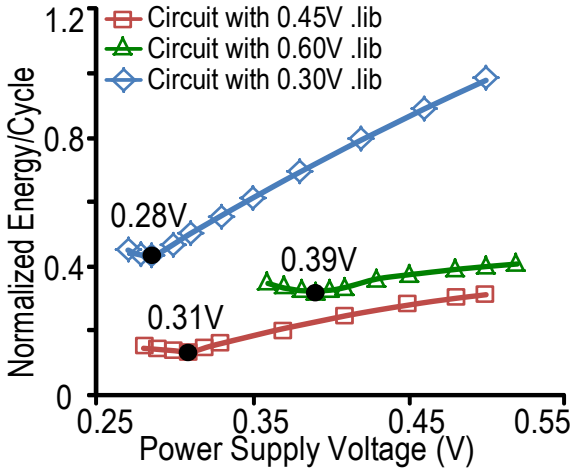
faster & more robust



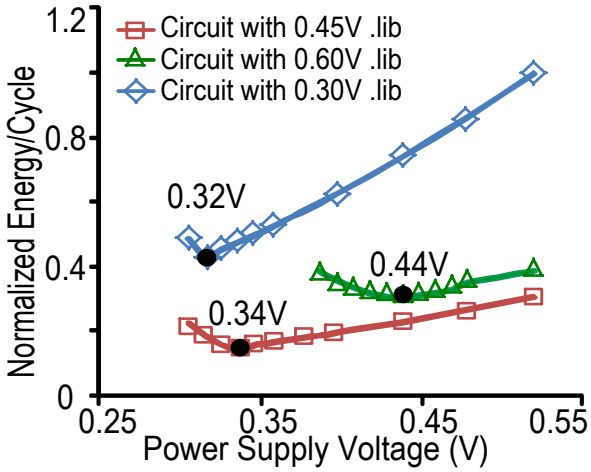
Measurement Results







(a) Energy w/ ECG signal



(b) Energy w/ random signal

Normalized energy/cycle with inputs (a) ECG signal; (b) random signal
(Black dots indicate the optimum points)

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Benchmark

	This Work		[1] TCASII'12	[2] VLSI'07	[3] JSSC'10	[4] JSSC'10
	with 0.45V .lib	with 0.6V .lib				
FIR Type	14-tap, 8-bit		30-tap, 8-bit	8-tap, 8-bit	14-tap, 8-bit	8-tap, 8-bit
Technology	0.18-µm		0.13-µm	0.13-µm	0.13-µm	90-nm
Optimum V_{DD} (V)	0.31	0.39	0.35	0.2	0.27	0.29
Freq. (Hz)	100k	100k	29k	12k	20M	148k
Energy/Tap (pJ)	**0.02735**	**0.03568**	1.1	1.19	1.11	0.6275
Power (nW)	**38.29**	**49.95**	32	114	310,000	742.96
FoM*	**0.4273**	**0.5575**	0.57	18.55	17.37	9.80
Area/Channel (mm^2)	0.053	0.049	0.058	1.54	0.38	N/A

*FIR FoM = power(nW)/freq.(MHz)/# of taps/input bit length/coefficient bit length

[1] A. Klinefelter, et. al., "A programmable 34 nW/channel sub-threshold signal band power extractor on a body sensor node SoC," *IEEE Trans. on Circuits and Systems II*, vol. 59, no. 12, pp. 937-941, Dec. 2012.

[2] H. Myeong-Eun, et. al., "An 85 mV 40 nW process-tolerant subthreshold 8 x 8 FIR filter in 130 nm Technology," in *Proc. IEEE Symp. VLSI Circuits - VLSI '07*, pp. 154-155, Jun. 2007.

[3] W.-H. Ma, et. al., "187 MHz subthreshold-supply charge-recovery FIR," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 793–803, Apr. 2010.

[4] I. J. Chang, et. al., "Exploring asynchronous design techniques for process-tolerant and energy-efficient subthreshold operation," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 401-410, 2010.

Conclusion

1. Unbalanced pull-up/down networks and logical effort are applied to realized a sub-threshold VLSI logic family for biomedical applications.
2. Three 14-tap 8-bit FIR filters were designed and measured according to different liberty timing files.
3. The achieved FoMs at the minimum energy operating points for the 0.45 and 0.6-V library designs were 0.4273 (at 0.31 V) and 0.5575 (at 0.39 V) which compared favorably with the state-of-the-art F.I.R. filter designs.