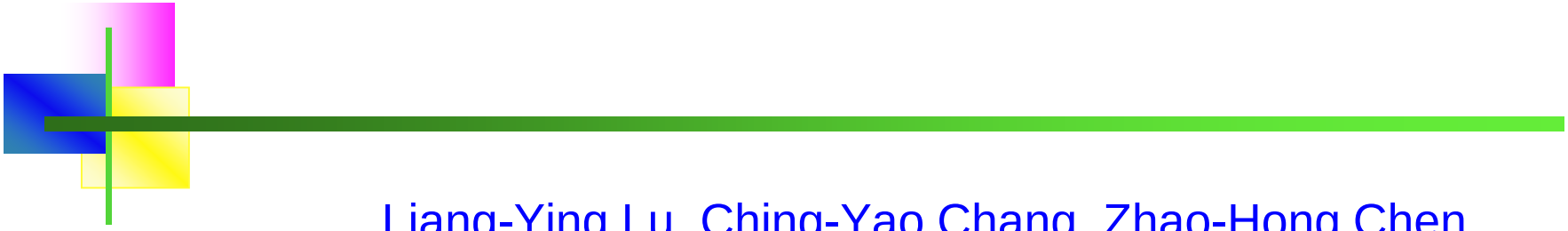
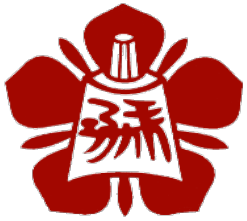
A Testable and Debuggable Dual-Core System with Thermal-Aware Dynamic Voltage and Frequency Scaling





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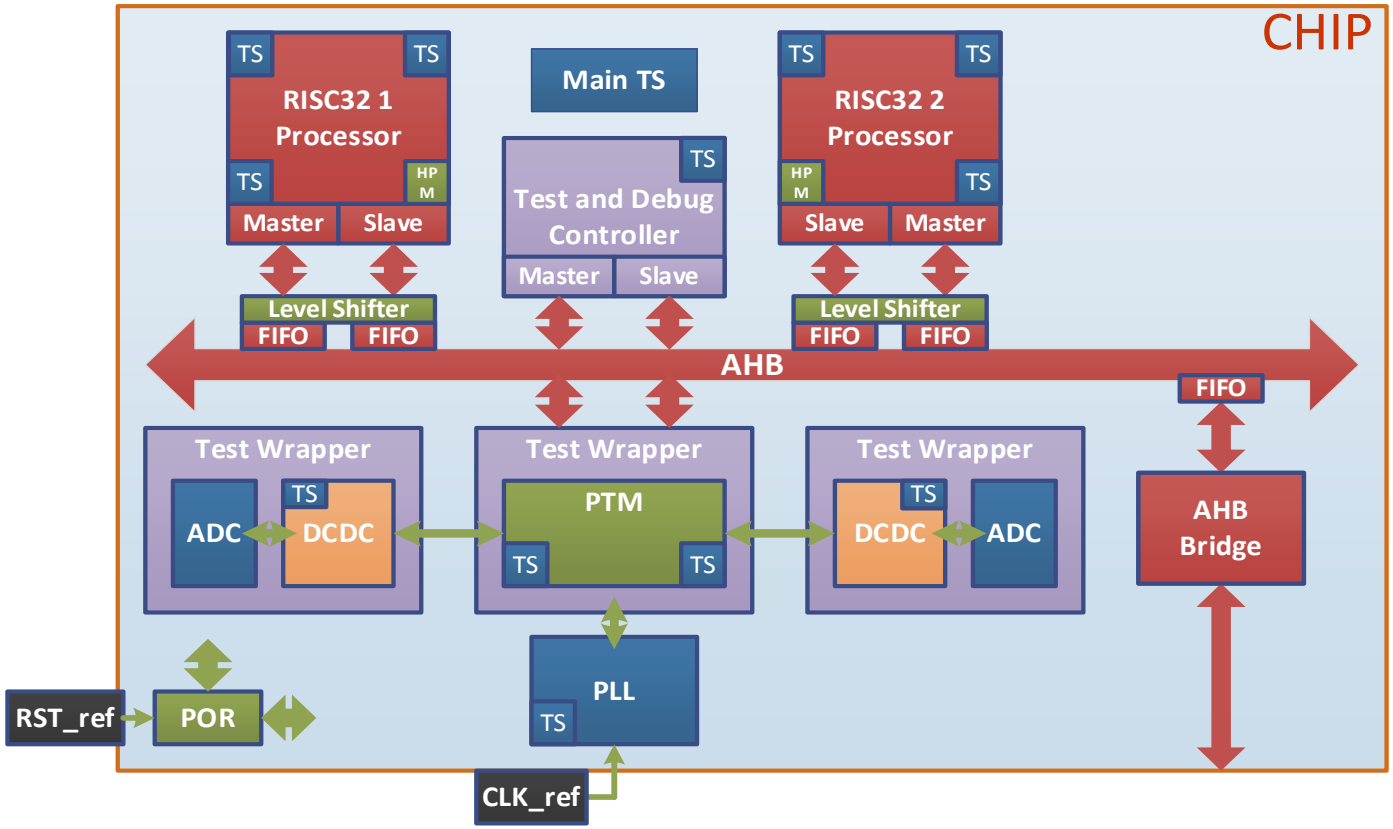
System Architecture

- Architecture and Main Components of the Design
  - ARM-like cores (RISC32), Hardware Performance Monitor(HPM), Test and Debug Controller, Power/Thermal Management controller (PTM) , DC-DC converter, ADCs, PLL and Primary-Auxiliary Temperature Sensors.

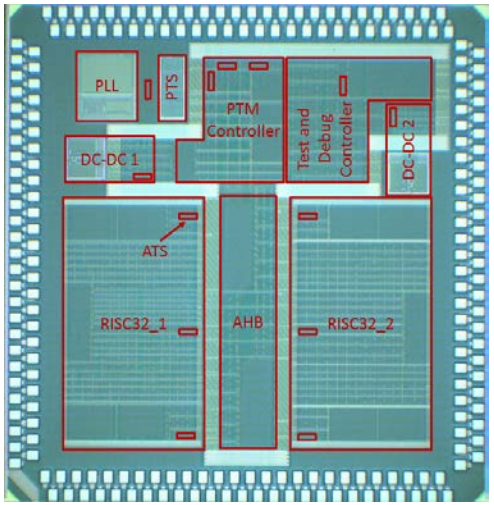


Design Features

1. High performance dual-core system
2. A low power timing error prediction mechanism with the hardware performance monitors
3. Intelligent management of operation frequency and voltage in the thermal-aware DVFS mechanism
4. A patented primary-auxiliary temperature sensing system
5. An on-chip test & debug platform for the structural test and silicon debug strategy

Fabricated Chip

- The proposed SoC was fabricated using a TSMC 90nm CMOS technology.
- The regions of voltage and frequency are from 0.7 mV to 1 mV and from 10 MHz to 150 MHz, respectively.



Die photo of the chip

Region	Voltage (V)	Frequency (Hz)
1	1.0 (1.0 ~ 0.925)	150 M
2	0.9 (0.9 ~ 0.825)	120 M
3	0.8 (0.8 ~ 0.725)	100 M
4	0.7	10M

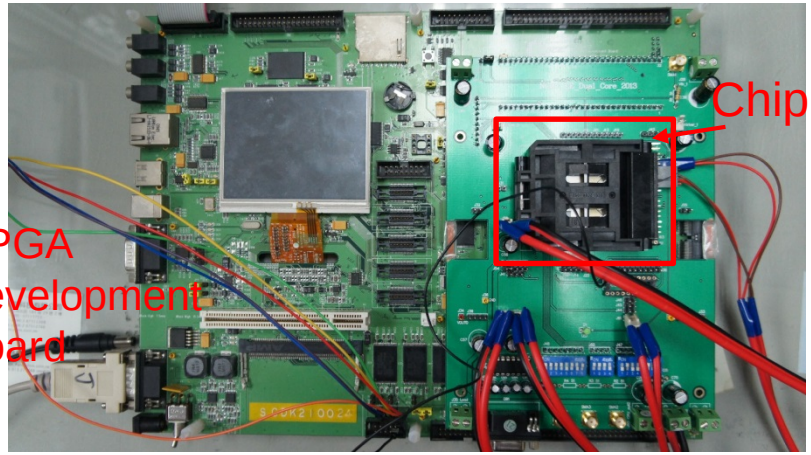
Voltage-frequency relation of DVFS

Items	Contents
Technology	TSMC 90nm (MSG)
Voltage Range	0.7~1V (25mV)
Frequency Range	10M~150M Hz
Temperature Resolution	1°C
Number of Core	nRISC32 CPU (ARM926-like) * 2
Lower Power Technique	DAVFS, Clock Gating
Die Area	2.597545*2.59608 mm^2
Package	CQFP208 (208 Pins)

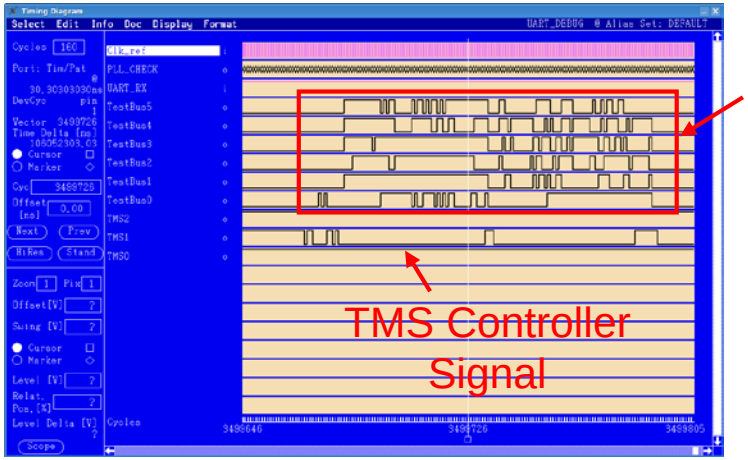
Chip Characteristics

Measurement Environment and Results

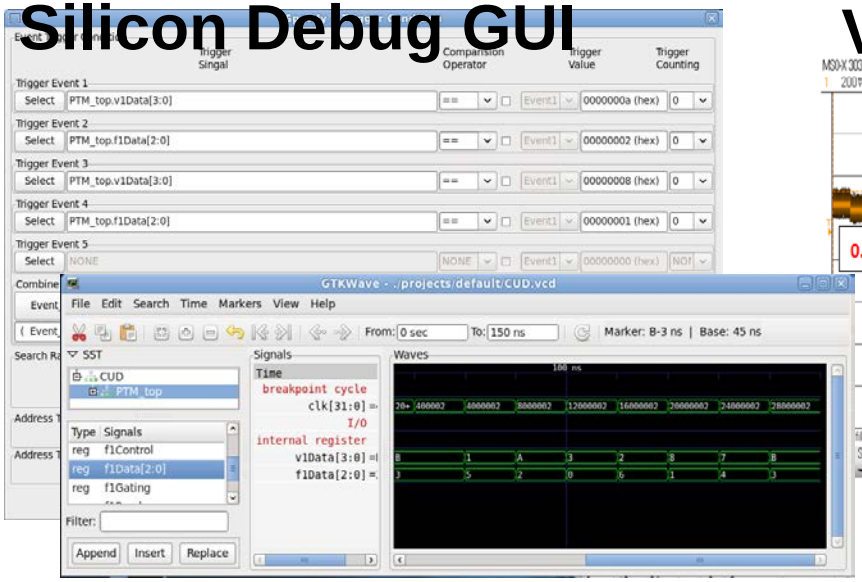
Measure environment



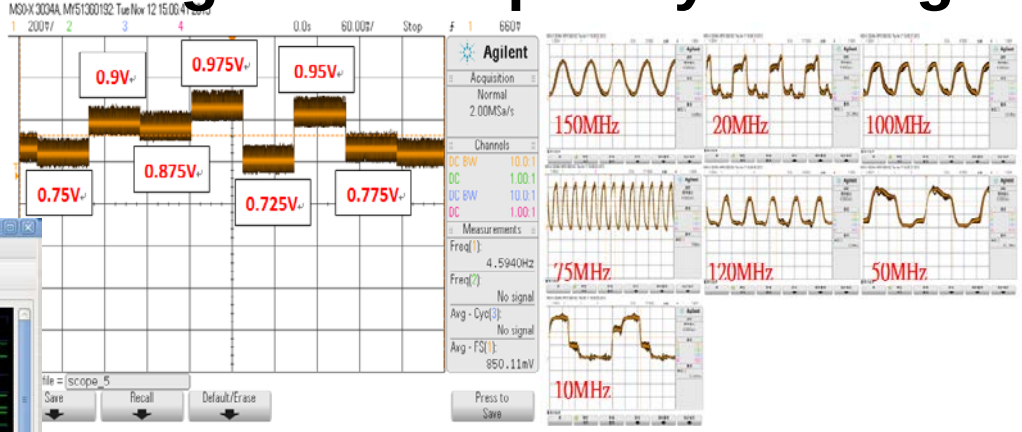
On-chip testing



Silicon Debug GUI



Voltage and frequency Scaling



Measured/Test Items

Measured items	Measured results	Measured items	Measured results
DVFS (PLL, DCDC, PTM, TS, ADC)		Dual-core CPU (nRISC processor) & AHB bus	
1.PLL produces 7 type of frequency and bypass function	Pass	16. Processor executes the foundational instruction and addressing mode to complete the verification	Pass
2.DCDC DVS self-testing (external ADC)	Pass	17. Processor connects on-chip AHB via asyn-bridge	Pass
3.DCDC DVS self-testing (internal ADC)	Pass	18. Processor accesses on-chip slave device	Pass
4.PTM accesses program in ROM to execute DVS self-testing	Pass	19. Processor connects off-chip AHB	Pass
5.PTM accesses program in ROM to execute DFS self-testing	Pass	20. Processor accesses off-chip slave device	Pass
6.PTM accesses external program from AHB	Pass	21. Processor connects off-chip AHB via asyn-bridge	Pass
7.PTM accesses temperature sensor and writes to external memory	Pass	22. Processor accesses off-chip slave device via asyn-bridge	Pass
8.PTM controls DCDC, external ADC and PLL to process DVFS	Partially pass	23. Startup memory management unit (MMU) and Translation Lookaside Buffer (TLB)	Pass
9.PTM accesses temperature sensor to process DVS	Pass	24.Start up function of Cache	Pass
Build in Test Access Mechanism Controller		25.Process system execution in asynchronous	Pass
10.Processor accesses TAMC's internal register and memory	Pass	26. Process system execution in different voltage	Pass
11.Processor setups and boots up TAMC to process DCDC's scan test and on-chip comparison	Pass	27. Connect Internal AHB asyn-bridge and off-chip AHB	Fail
12.Processor setups and boots up TAMC to process PTM's scan test and on-chip comparison	Pass	28.Process compression of executed instructions with MISR	Pass
13. Processor setups and boots up TAMC to process ADC self-test	Pass	29.Start TestShell	Pass
Hardware Debug Mechanism		30.Processor executes software-based self-test	Pass
14. Processor setups and boots up TAMC to process cycle-based debug. Utilizing external debugging software to process debug function of breakpoint and single step.	Pass	31.Second processor processes the execution	Partially pass
15. Processor setups and boots up TAMC to process event trigger debug, Utilizing external debugging software to set trigger conditions	Pass	32.BootLoader (u-Boot)	Pass
A total of 33 items, 30 items completely pass, 2 items partially pass.		33.Start Linux	Pass

Conclusions

- For this successful academic collaborating design, we develop a chip containing two high-performance processors, several ADC circuits, a DVFS system, several hardware performance monitors, a primary-auxiliary temperature sensing system and a powerful test and debug controller.
- Measurement results validate most functionalities of the chip as well as the efficiencies of the proposed techniques.