A Novel Low-Cost Dynamic Logic Reconfigurable Structure Strategy for Low Power Optimization

***Yu-Guang Chen, Wan-Yu Wen, Yun-Ting Wang, You-Luen Lee, and Shih-Chieh Chang**

Department of CS, National Tsing Hua University, HsinChu, Taiwan

Outline

- Introduction
- Proposed DLRS Designs
- Low-Power Optimization Framework
- Experimental Results
- Conclusions

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Introduction

- Power consumption has become one of the most significant problems in modern IC designs
- Several low power design methodologies have been proposed
  - Dynamic Voltage and/or Frequency Scaling (*DVFS*)
  - Reconfiguration-oriented Approximate Computing

Motivation

- Most previous works only address on either DVFS or logic reconfiguration at one time
- For further investigation, we explore the idea about novel **Dynamic Logic Reconfigurable Structure** (*DLRS*) designs
  - Power saving
  - Data integrity
  - Only marginal area overhead

Design Concepts

- We propose novel low-cost DLRS adder and multiplier, and a comprehensive framework for low power designs.
  - Higher speed (larger power) vs. lower speed (smaller power)
  - Sharing basic components of both structures
  - Reconfiguration can be done instantly

Advantages

- We further integrate our DLRS designs with DVFS to create more flexibility
  - For DVFS, module can only be scaled down to the lowest available VDD candidates
  - With DLRS, we can perform DVFS on different structures of the same design thus creating more timing and power flexibility
  - Better trade-off between performance and power consumption

Major Contributions

- A novel DLRS methodology
  - Configure a design to high performance or low power
  - Keep data integrity
- Low cost DLRS adder and multiplier
  - Can be configured to two different structures
- A low power design framework
  - Integrates both DVFS and DLRS techniques to provide more flexibility
  - Low power optimization

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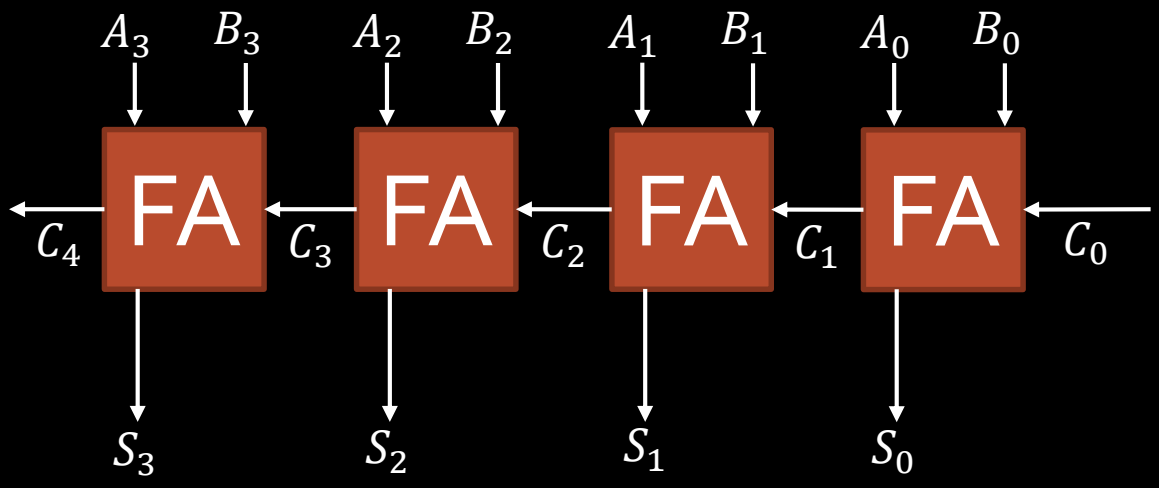
DLRS Adder

- The DLRS adder is constructed by integrating the carry look-ahead adder and the ripple carry adder
  - The former can provide higher speed yet consume larger power
  - The later runs in slower speed yet consume smaller power

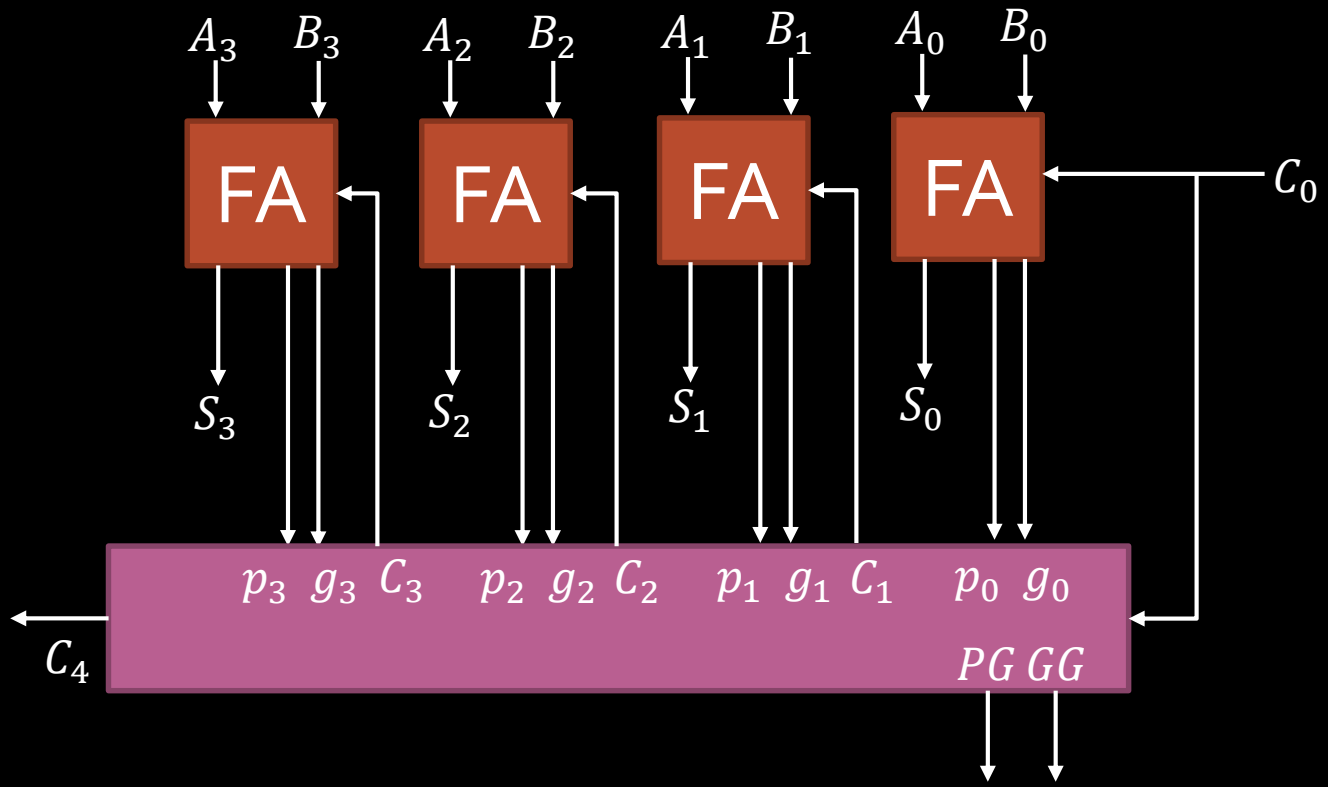
4-bit Ripple Carry Adder

- Carry input needs to propagate through the serial chains of full adders
  - Slow
  - Low power consumption



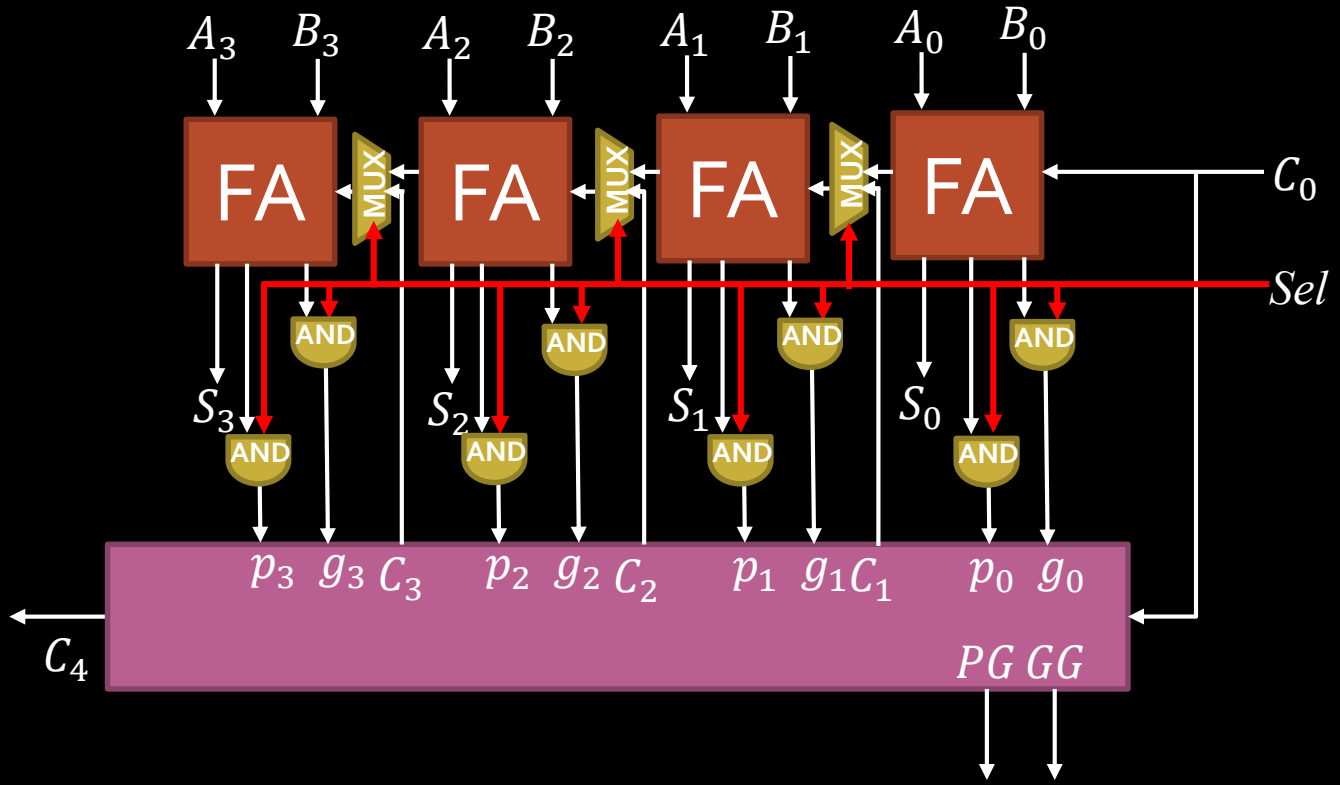
4-bit Carry Look-ahead Adder

- Use two additional binary signals and a computation block to process carry
  - Faster
  - High power consumption



4-bit DLRS Adder

- Both adder have similar structures and basic components
- Integrate two structures by sharing components

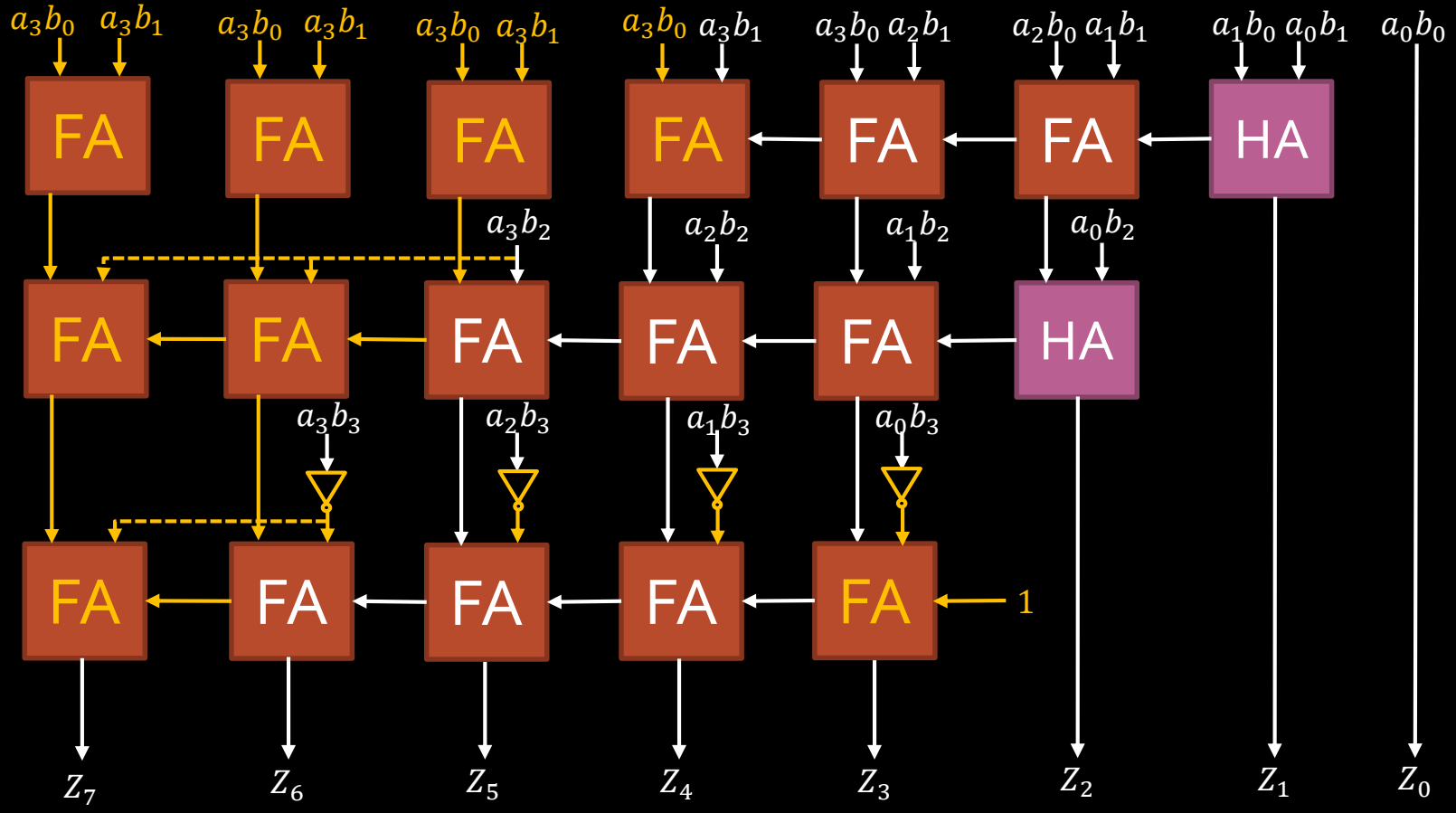


DLRS Multiplier

- We use the similar idea of creating the DLRS adder to create the DLRS multiplier
  - Array multiplier is constructed using the carry select adder and the ripple carry adder
  - Wallace-tree multiplier reduces the multiplication layer and propagation delay by applying the booth-encoding scheme

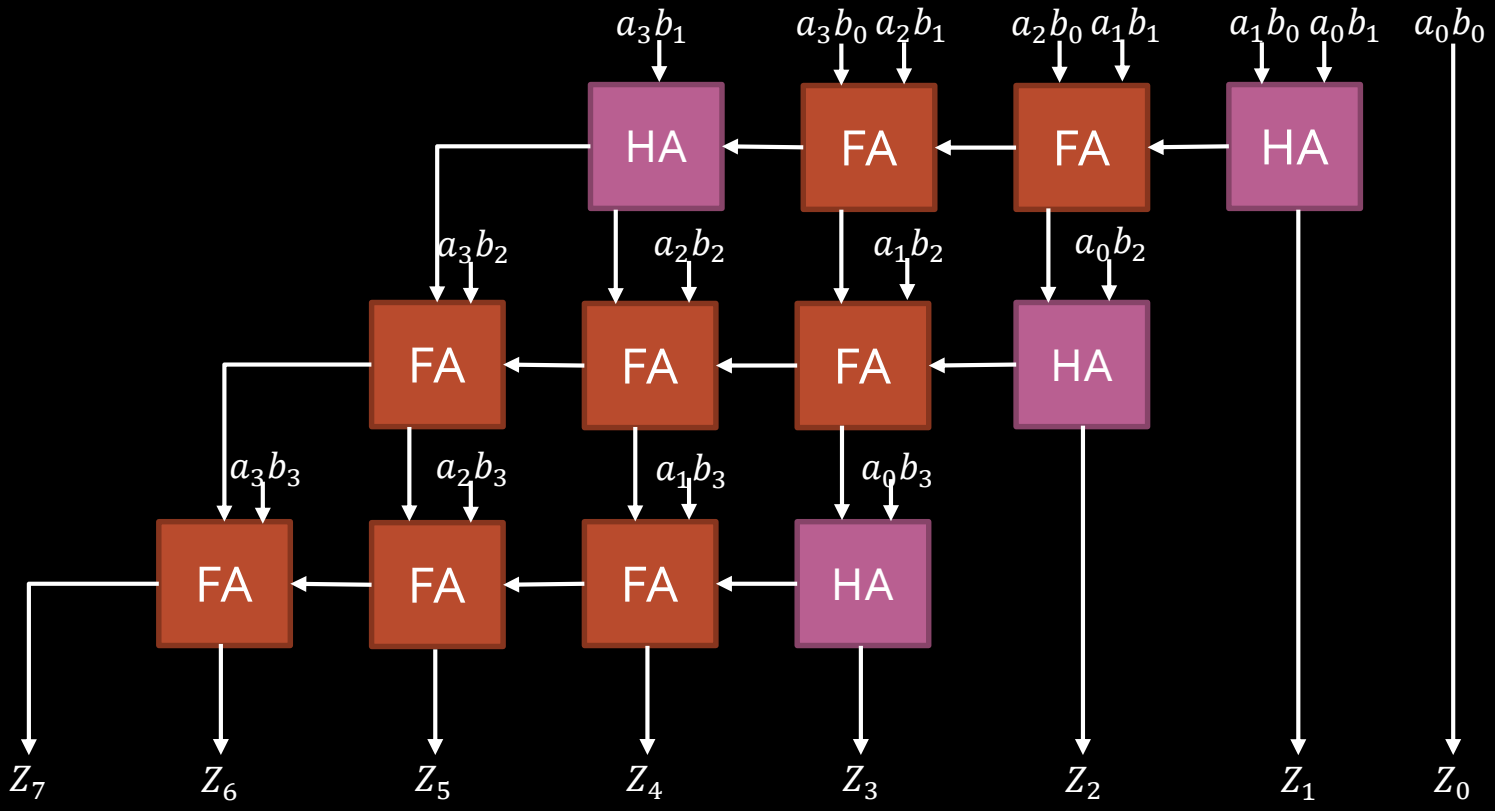
4-bit Array Multiplier (Signed)

- 18 adders and 4 inverters



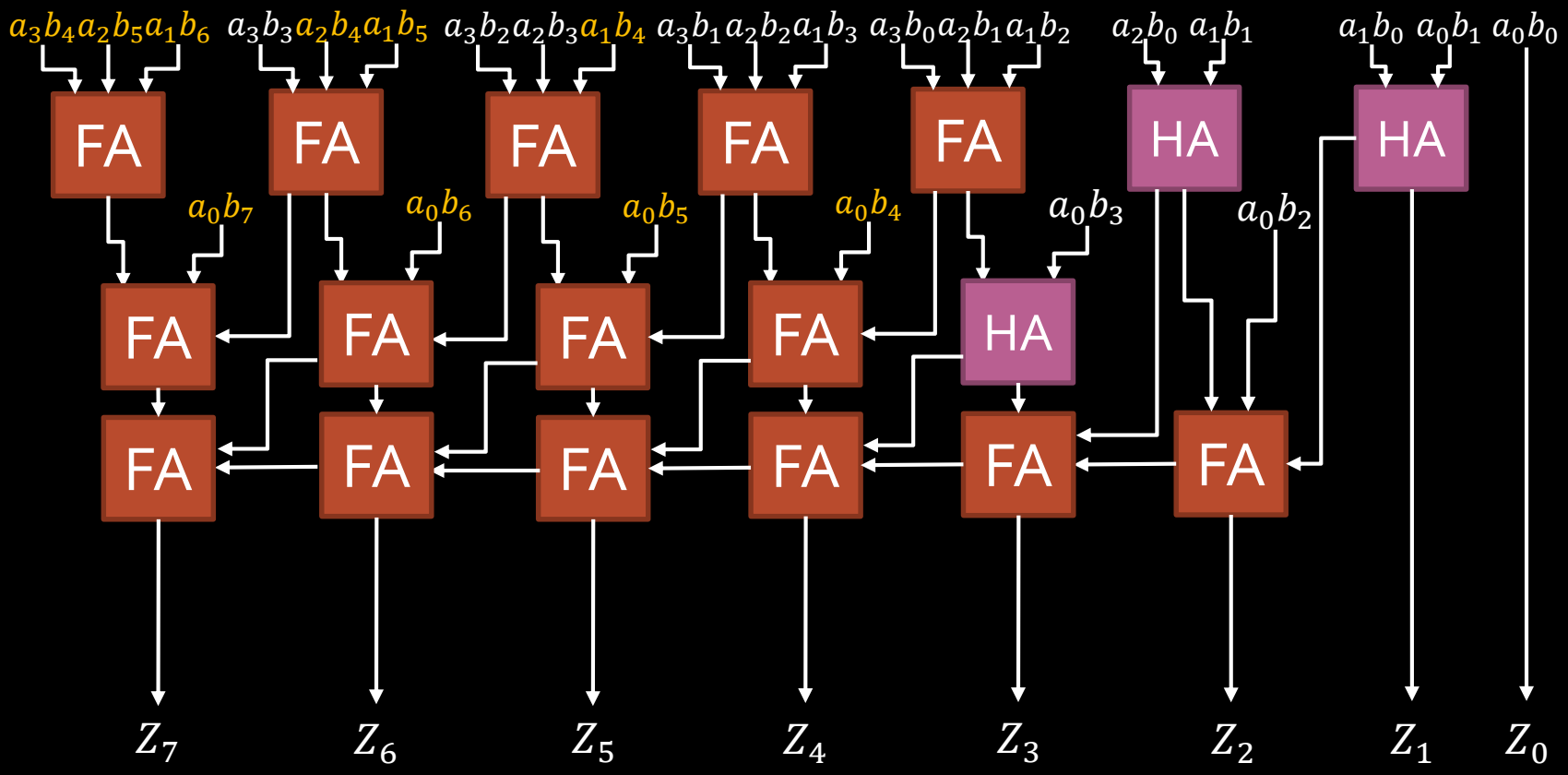
4-bit Array Multiplier (Unsigned)

- 8 full adders and 4 half adders
- Consumes less power
- Low Speed



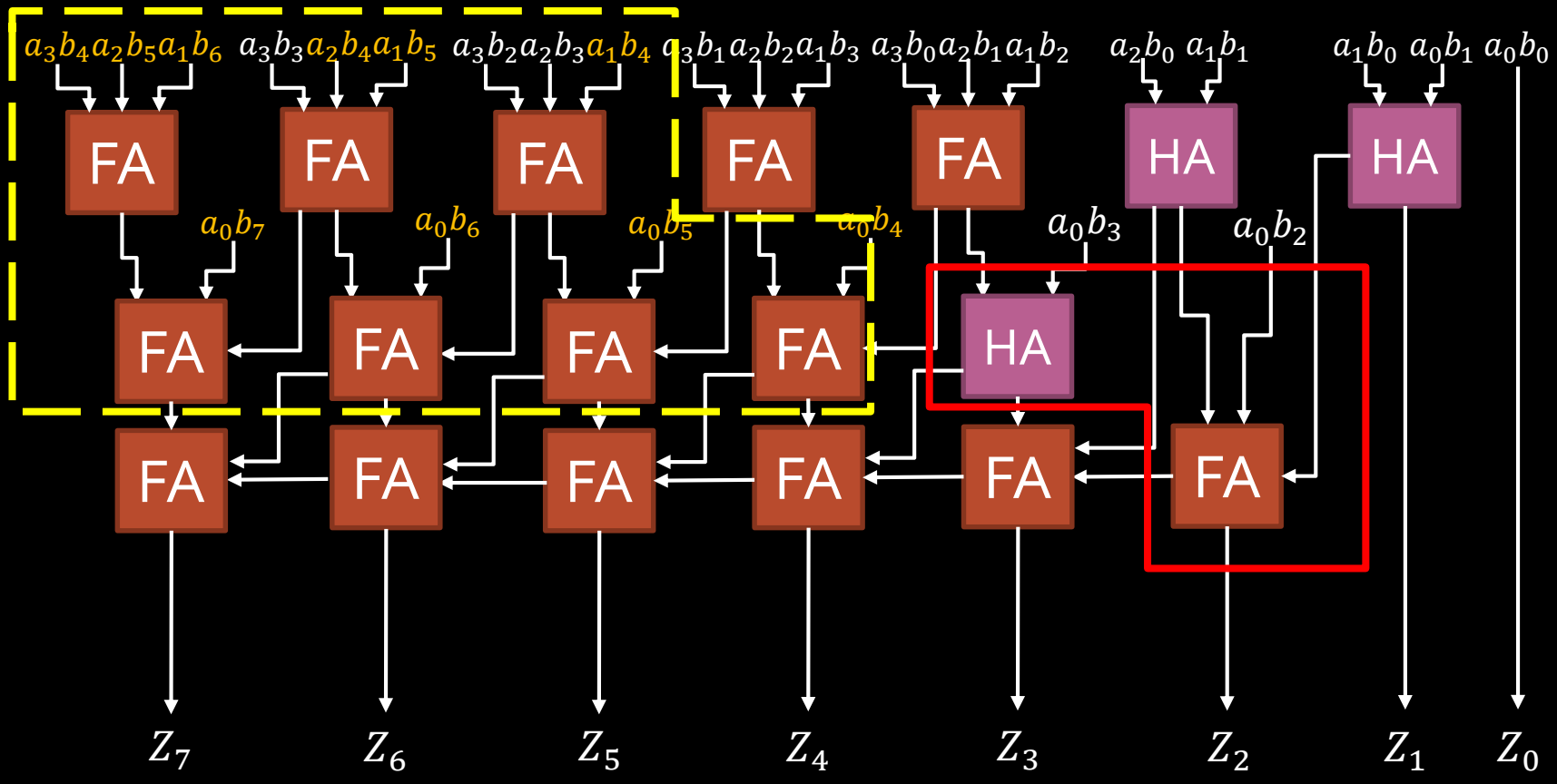
4-bit Wallace-tree Multiplier

- 15 full adders and 3 half adders
- Consumes more power
- High Speed



4-bit DLRS Multiplier (Draft)

- Solid contour shows those modules may need reconfiguration
- Dotted contour shows modules can be powered-off for unsigned calculation



Summary

- In general, all logics can be designed with reconfiguration if
  - They can have logic sharing between the high speed mode and power saving mode for area consideration
- We will explore more DLRS logic components in the future

Problem Formulation

- Given
  - (1) a circuit with DLRS adders and multipliers,
  - (2) all possible reconfiguring options of DLRS adders and multipliers,
  - (3) a DVFS scheme and corresponding voltage candidates
- Object
  - Determine optimal configurations under timing constraints in the circuit
- Subject to
  - the operating power is minimized

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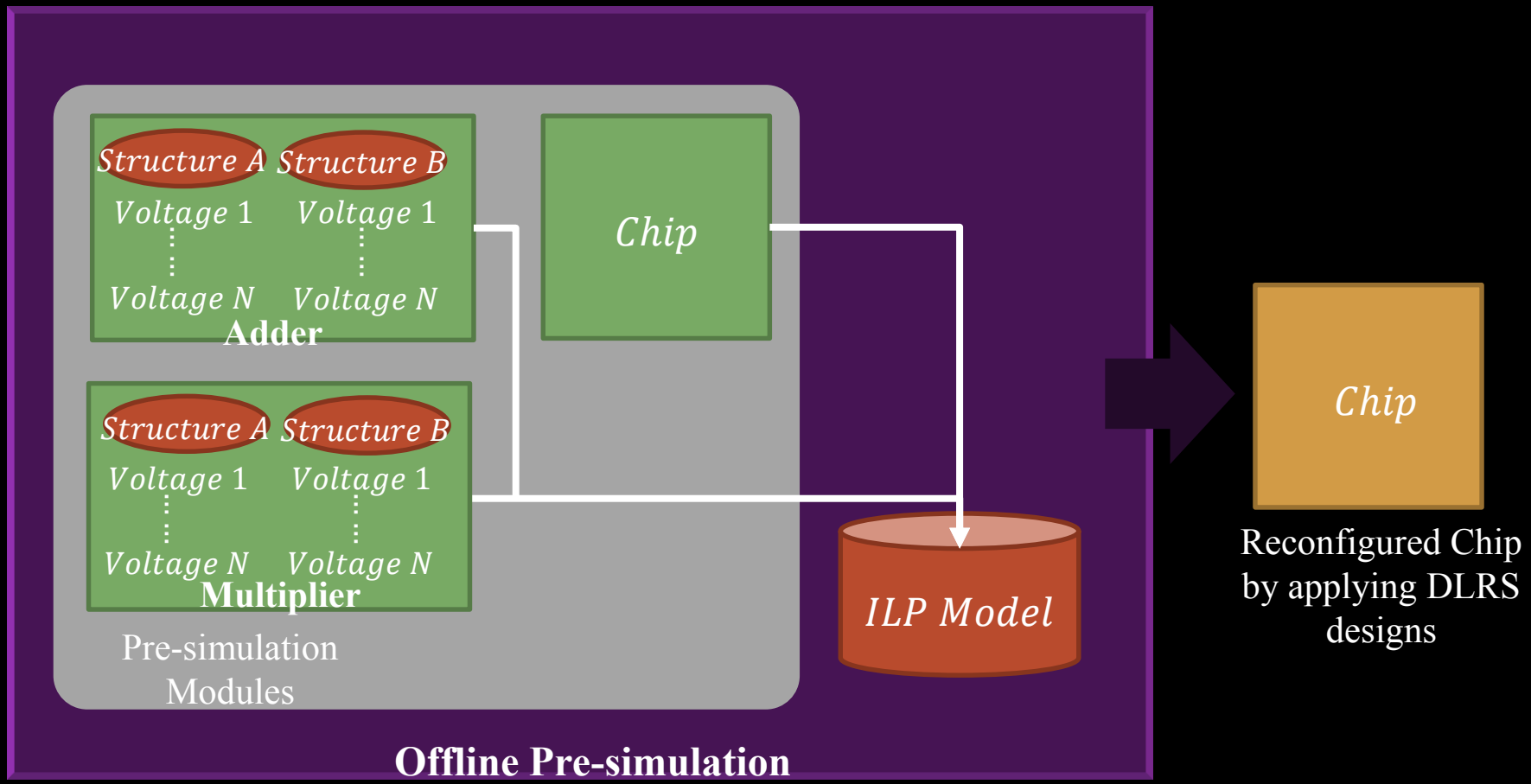
Framework


Structure A
Structure B
Voltage 1
Voltage 1
Voltage N
Voltage N
Adder
Structure A
Structure B
Voltage 1
Voltage 1
Voltage N
Voltage N
Multiplier
Pre-simulation Modules
Chip
ILP Model
Offline Pre-simulation
Chip
Reconfigured Chip by applying DLRS designs

ILP-based Algorithm

- Objective
  - minimize total power consumption
  - satisfying circuit timing constraint
- min: $\sum_{i=1}^{M} P_i$
- $T_{li} < T_{c,constraint} \quad \forall\, l_i \epsilon L$
- $T_{li} = \sum_{i=1}^{q} T_i + T_{other\_fixed\_gates}$
- $\sum_{j=1}^{2N} S_{i,j} = 1, \forall i \in M$
- $P_i = \sum_{j=1}^{2N} S_{i,j} \times P_{i,j}, \forall i \in M$
- $T_i = \sum_{j=1}^{2N} S_{i,j} \times T_{i,j}, \forall i \in M$

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Experimental Results

- On 8-core, 2.40GHZ, Intel Xeon E5620 CPU, with 32GB memory, CentOS release 5.9 machine
- Operating voltage candidates are set to 0.8V, 0.9V, and 1V
- Three different timing constraints (i.e. tight, medium and loose) for each circuit
- Three benchmark circuits with 90nm technology are used

Circuit Designs	# Components in Circuits				
	Adder	Multiplier	Subtractor	Comparator	Divider
HAL	2	6	2	1	0
IDCT	16	20	10	0	2
DIST	96	0	0	16	0

Experimental Results

Circuit Designs	Operating Timing Constraint	DVFS	DLRS/DVFS Joint				
		Power Consumption (mW)	# Reconfigured DLRS adder (%)	# Reconfigured DLRS multiplier (%)	Power Consumption (mW)	Power Reduction (%)	Area Overhead
HAL	Tight	10.9864	0 (0%)	6 (100%)	4.4244	59.73	6.13
	Medium	9.8878	0 (0%)	6 (100%)	4.3369	56.14	
	Loose	8.7891	2 (100%)	6 (100%)	4.1044	53.30	
IDCT	Tight	40.7069	12 (75%)	20 (100%)	16.2625	60.05	6.55
	Medium	36.6362	13 (81.25%)	20 (100%)	16.0812	56.11	
	Loose	32.5655	16 (100%)	20 (100%)	15.7692	51.58	
DIST	Tight	42.0221	93 (96.8%)	--	23.9472	43.01	4.74
	Medium	37.8199	96 (100%)		23.6352	37.51	
	Loose	33.6177	96 (100%)		23.6352	29.69	

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Conclusions

- We propose the concept of DLRS designs
  - allows logic reconfiguration
  - creates more flexibility to trade-off between performance and power consumption
- We propose a comprehensive framework for low power designs
  - smoothly integrate our DLRS designs with DVFS schemes
- Our methodology can obtain up to 60.05% power reduction with only 6.55% area overhead


Thank You
Q&A