MCMM Clock Tree Optimization based on Slack Redistribution Using a Reduced Slack Graph

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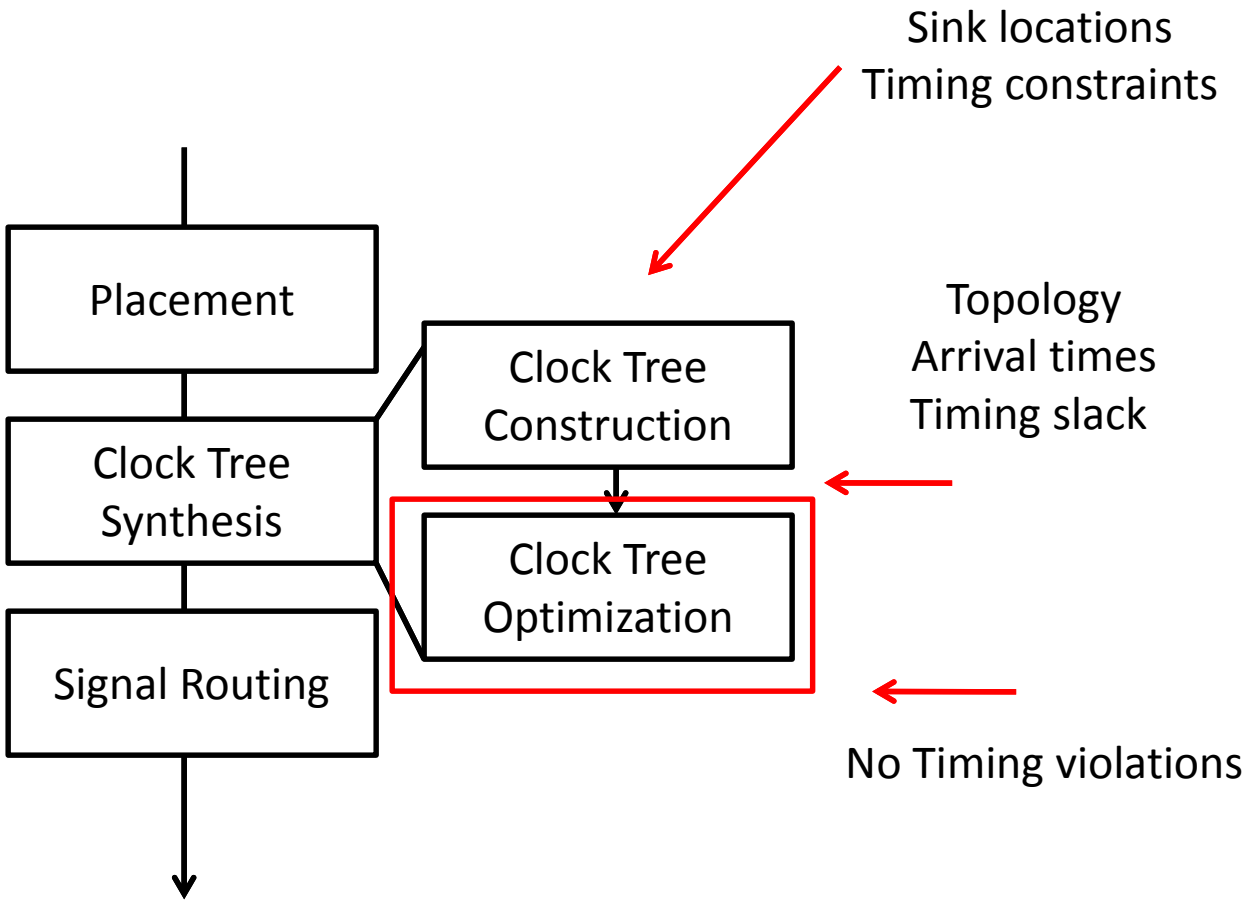
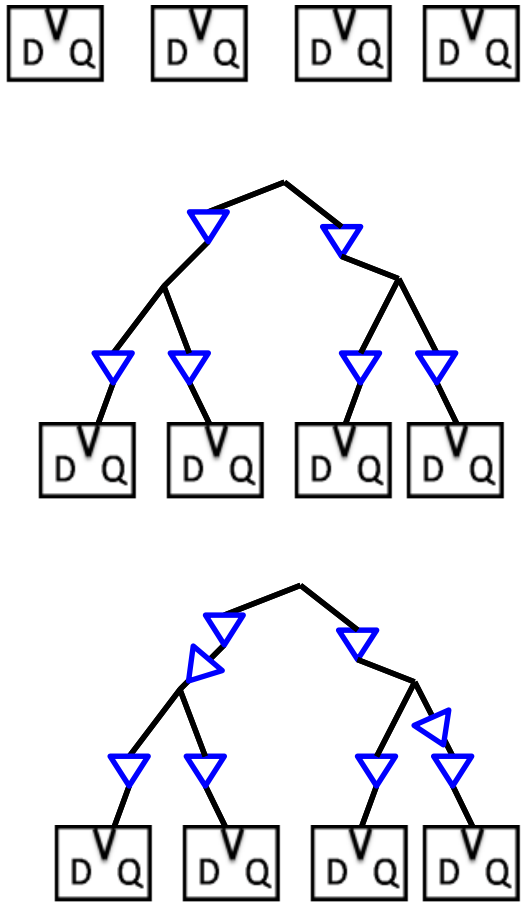
ASP-DAC 2016

Clock Tree Synthesis

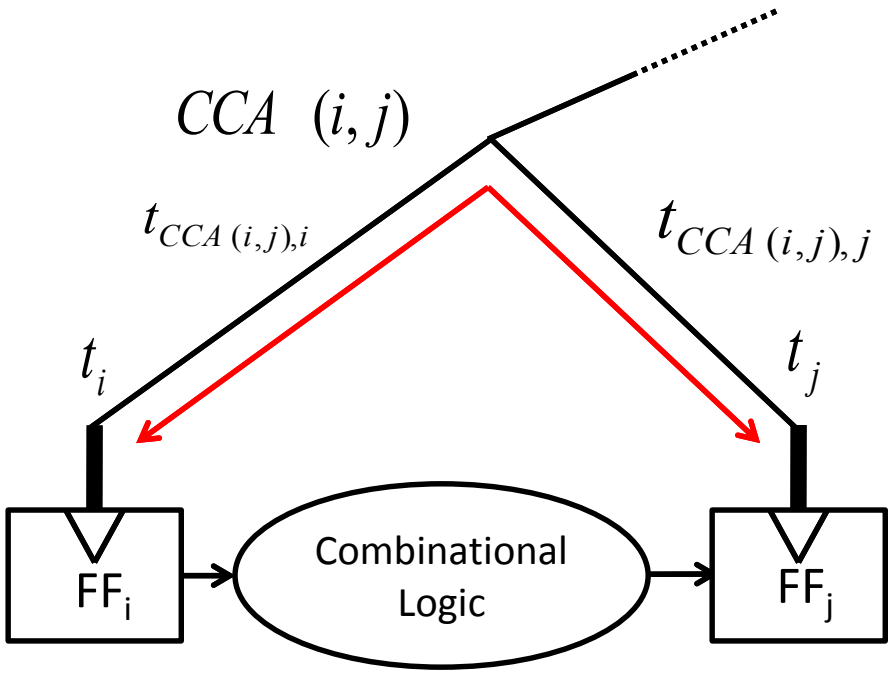




Timing Slack

$$slack_{ij}^{setup} = T - t_i^{CQ} - t_{ij}^{\max} - t_j^{S} + t_j - t_i - \delta_j - \delta_i$$

$$slack_{ji}^{hold} = t_i^{CQ} + t_{ij}^{\min} - t_j^{H} + t_i - t_j - \delta_j - \delta_i$$



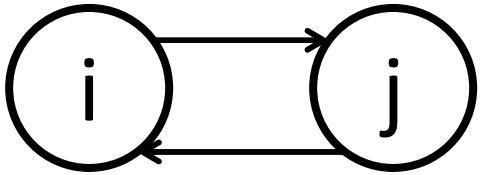
On-chip variations

$$\delta_i \propto t_{CCA\,(i,j),i}$$

$$\delta_j \propto t_{CCA\,(i,j),j}$$

Slack Graph (SG)

$$w_{ji} = slack_{ij}^{setup}$$



$$w_{ij} = slack_{ij}^{hold}$$

Problem Formulation

$$t_i^{new} = t_i + \Delta_i$$

$$t_j^{new} = t_j + \Delta_j$$

$$slack_{ij}^{setup} = T - t_i^{CQ} - t_{ij}^{\max} - t_j^S + t_j - t_i - \delta_j - \delta + \Delta_j - \Delta_i$$

$$w_{ji}$$

$$slack_{ij}^{setup} = w_{ji} + \Delta_j - \Delta_i$$

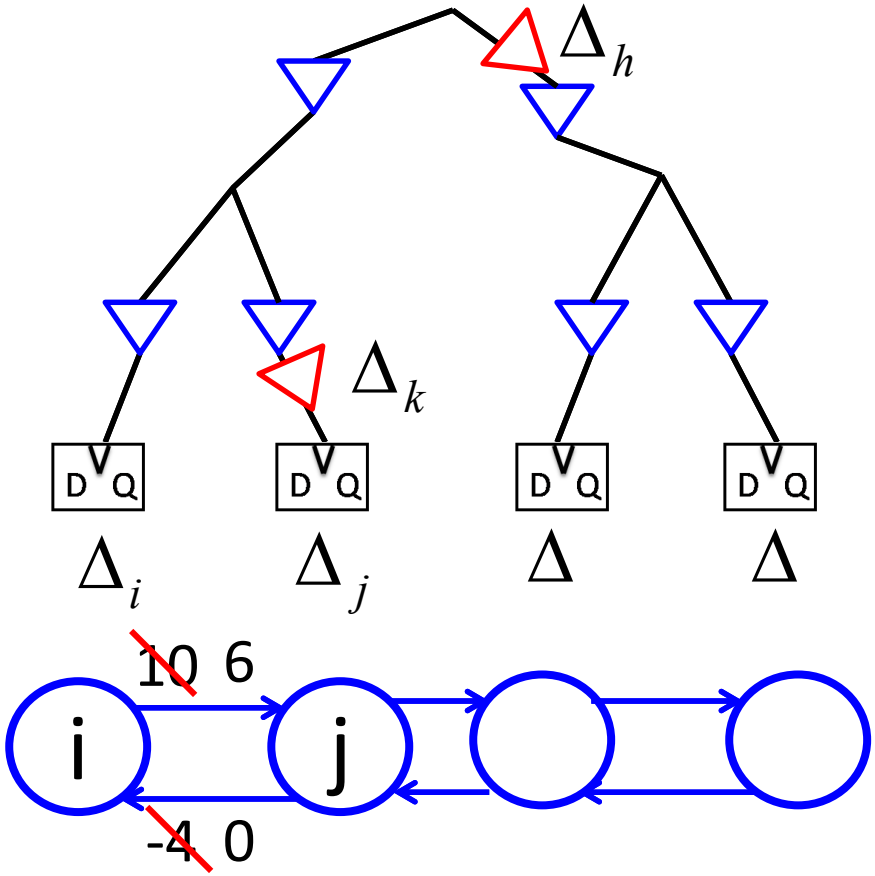
$$0 \le slack_{ij}^{setup}$$

$$\Delta_i - \Delta_j \le w_{ji} = -4$$

$$\Delta_j - \Delta_i \le w_{ij} = 10$$

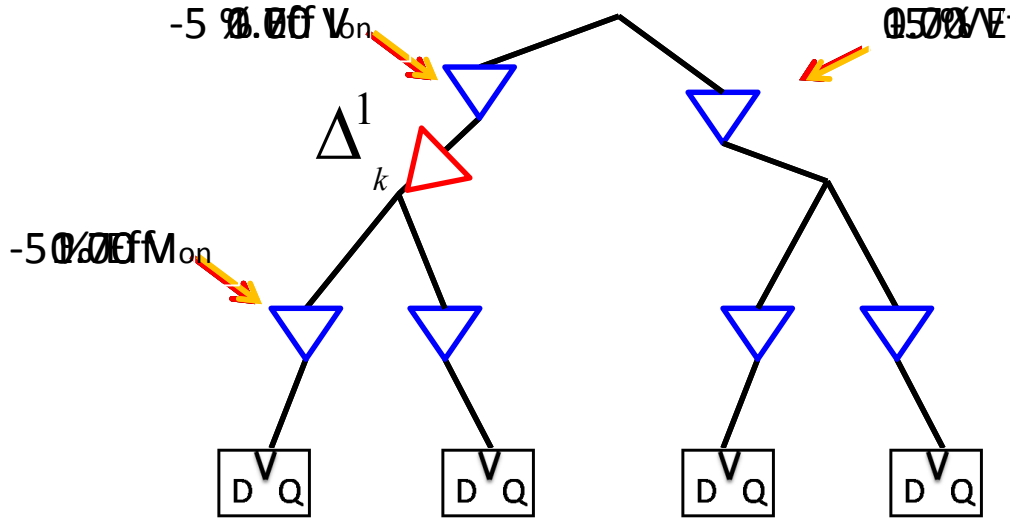
$$\Delta_i = 0$$

$$\Delta_j = 4$$



Problem: Find delay adjustments that remove the negative slacks!

Multiple Corners Multiple Modes



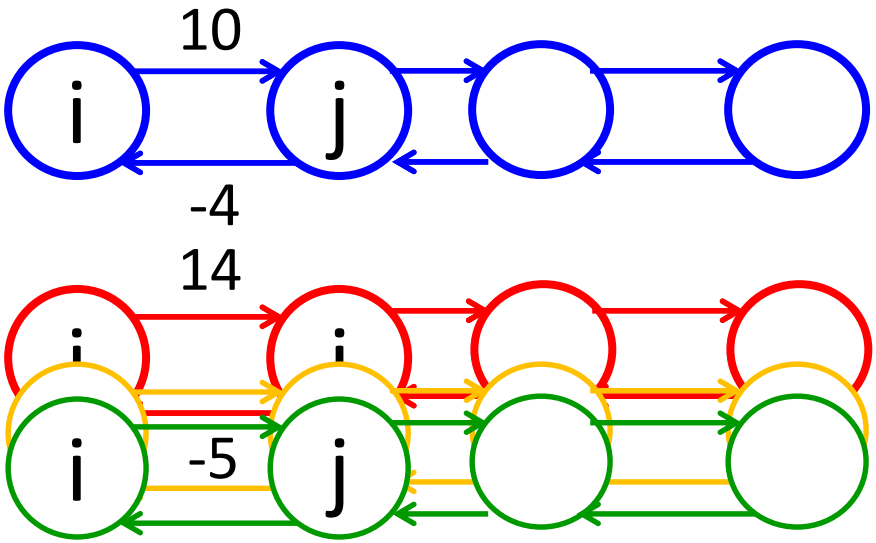
$$\Delta^1_k \rightarrow (\Delta^2_k, \Delta^3_k, \Delta^4_k)$$

1.00 V, 100 % Eff Ion

0.70 V, 100 % Eff Ion

0.70 V, 95 % Eff Ion

0.70 V, 95 % Eff Ion



$$\Delta^1_i - \Delta^1_j \leq w^1_{ji}$$

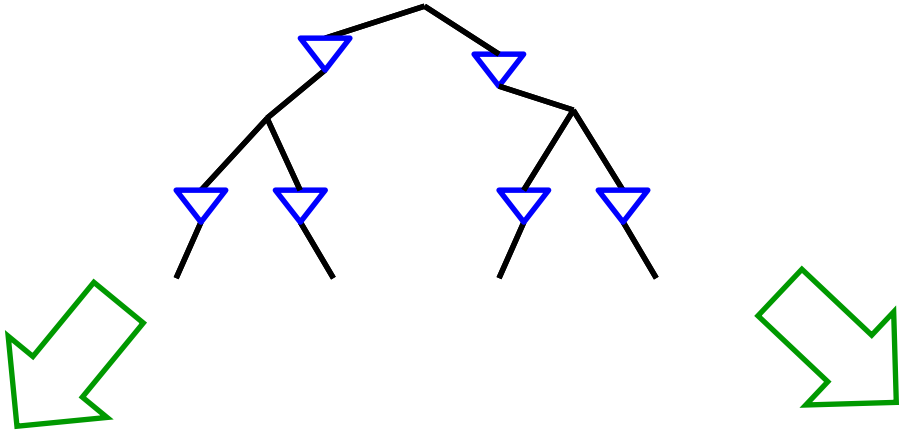
$$\Delta^2_i - \Delta^2_j \leq w^2_{ji}$$

$$\Delta^3_i - \Delta^3_j \leq w^3_{ji}$$

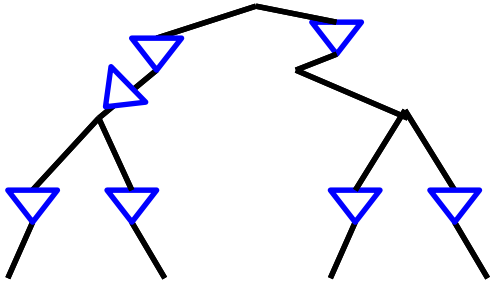
$$\Delta^4_i - \Delta^4_j \leq w^4_{ji}$$

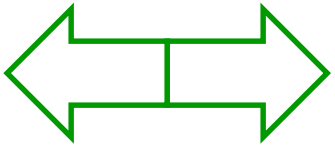
Previous Work

Clock tree with violations across MCMM

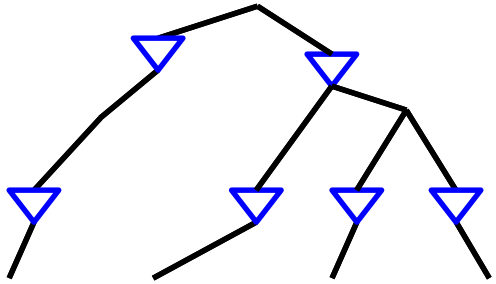


Assignment of delay adjustments

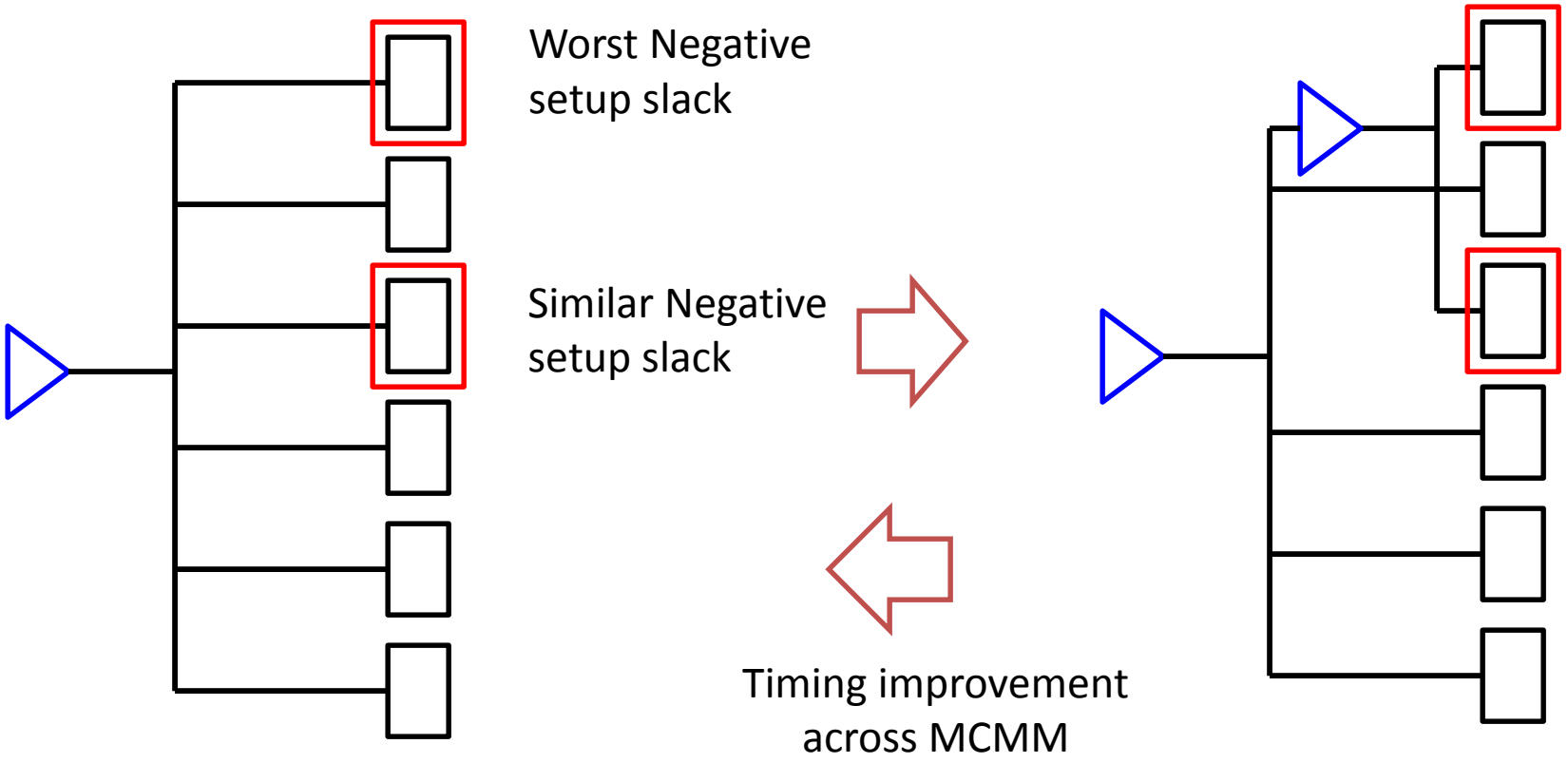




Realization of delay adjustments

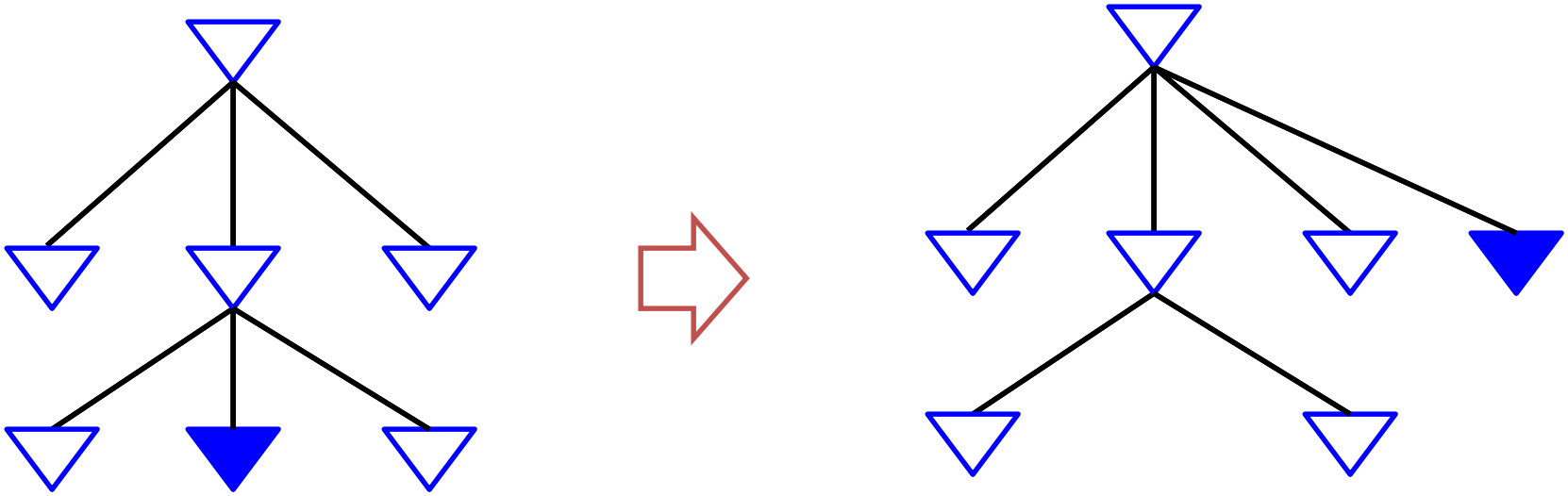


MCMM Optimization in [14]



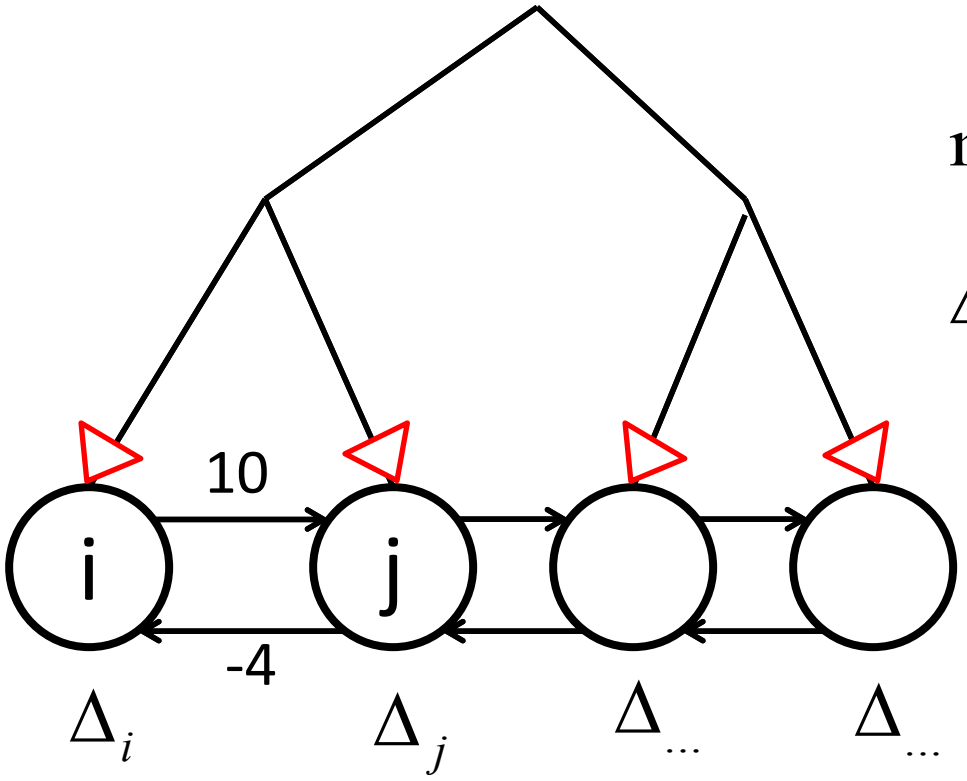
[14] W. Shen, Y. Cai, W. Chen, Y. Lu, Q. Zhou, and J. Hu. Useful clock skew optimization under a multi-corner multi-mode design framework. ISQED'10, pages 62–68, 2010.

Clock Tree Resynthesis in [16]



[16] S. Roy, P. Mattheakis, L. Masse-Navette, and D. Pan. Clock tree resynthesis for multi-corner multi-mode timing closure. IEEE Tran. on CAD of IC and Sys., pages 589–602, 2015.
[1] T.-B. Chan, K. Han, A. B. Kahng, J.-G. Lee, and S. Nath. OCV-aware top-level clock tree optimization. GLSVLSI ’14, pages 33–38, 2014.

SCSM Slack Redistribution in [10]



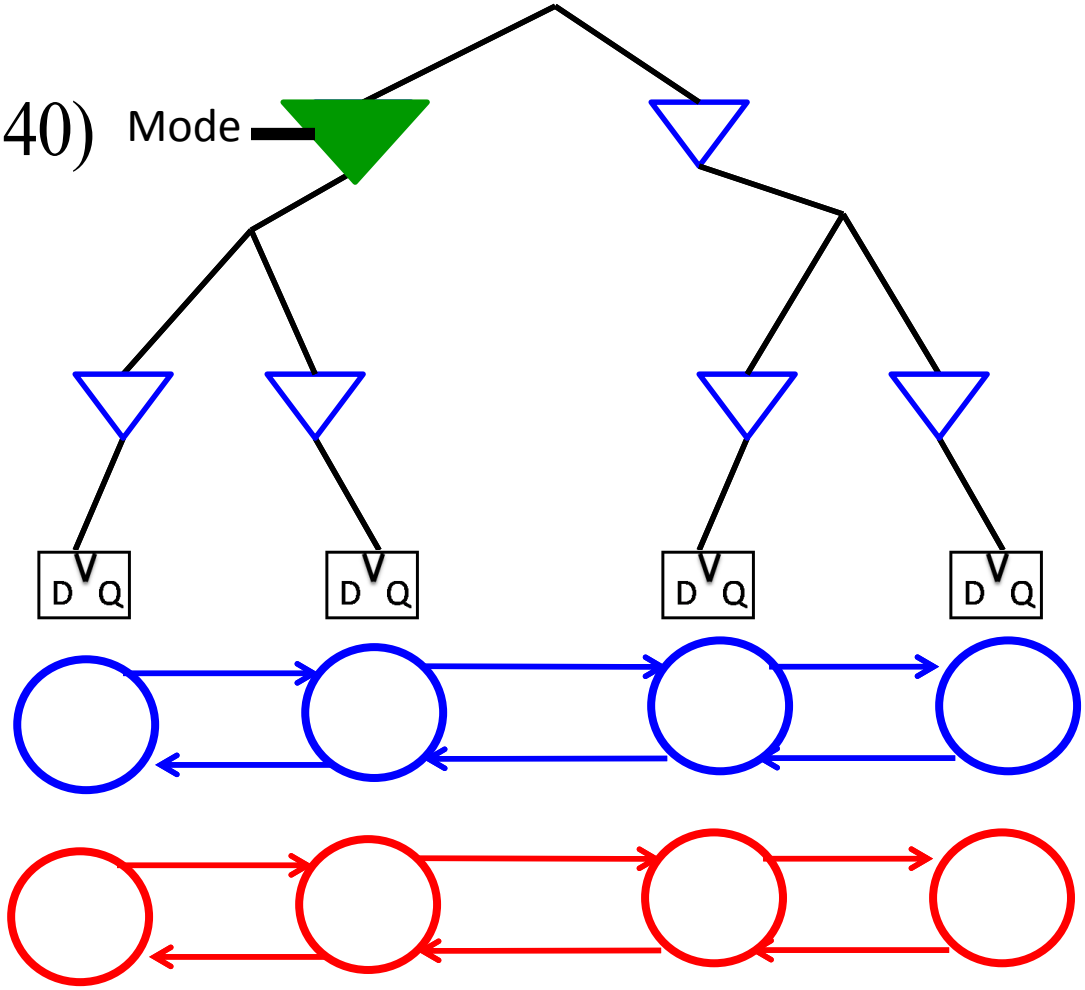
$$\min \sum_{k \in V} \Delta_k$$

$$\Delta_h - \Delta_k \le w_{kh}, \quad \forall (k,h) \in E$$

[10] J. Lu and B. Taskin. Post-CTS clock skew scheduling with limited delay buffering. In Circuits and Systems, pages 224–227, 2009.

Mode Adjustable Delay Buffers

$(\Delta_k^1 = 20, \Delta_k^2 = 40)$

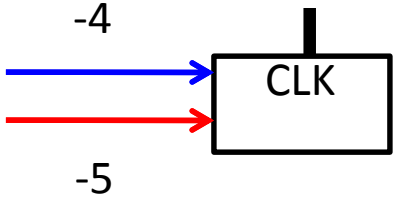


[8] J. Kim and T. Kim. Useful clock skew scheduling using adjustable delay buffers in multi-power mode designs. ASP-DAC'15, pages 466–471, Jan 2015.

MCMM Optimization

Corner compression in [15]

$$S^{*\mathrm{mod}}_{req} = S^{*}_{req} - (S^{*}_{slack} - \alpha S^{'}_{slack})\gamma$$



LP formulation in [12]

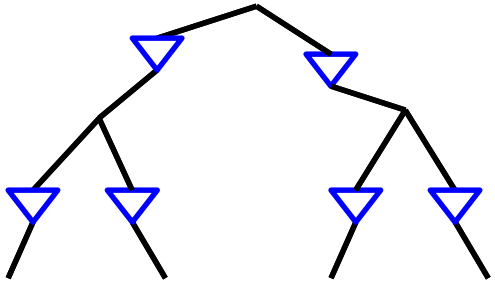
$$c_i \Delta_i - c_j \Delta_j - s_{ij} = pathslack_{ij}$$

[12] V. Ramachandran. Construction of minimal functional skew clock trees. ISPD'12, pages 119–120, 2012.

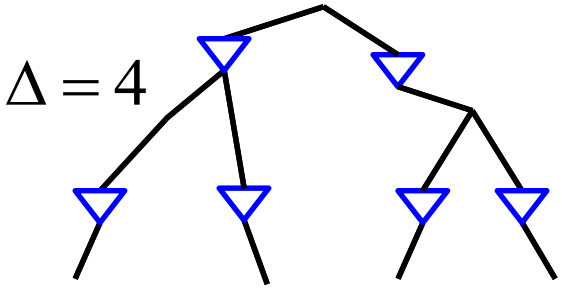
[15] M. Shrivastava and C. Park. Compressing scenarios of electronic circuits, Apr. 15 2014. US Patent 8,701,063.

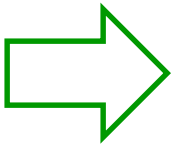
Our Work

Clock tree with violations across MCMM

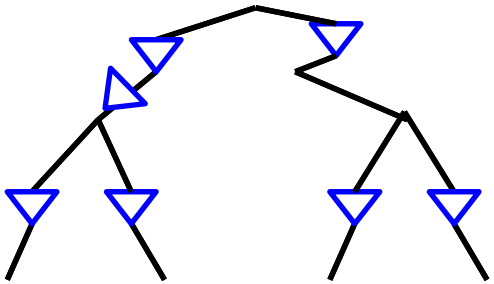


Assignment of delay adjustments





Realization of delay adjustments



Linearization of Delay Adjustments

$$\Delta_i^1 - \Delta_j^1 \le w_{ji}^1 \qquad \Delta_i^2 - \Delta_j^2 \le w_{ji}^2$$

$$\Rightarrow \quad \Delta_i^1 - \Delta_j^1 \le w_{ji}^1 \qquad \Delta_i^1 - \Delta_j^1 \le \frac{w_{ji}^2}{c^{12}}$$

$$\Rightarrow \quad \Delta_i^1 - \Delta_j^1 \le \min\{w_{ji}^1, \frac{w_{ji}^2}{c^{12}}\}$$

Linearization of delay adjustments

$$\Delta^2 = c^{12}\Delta^1$$

$$\Delta_i^2 - \Delta_j^2 \le w_{ji}^2$$

$$c^{12}\Delta_i^1 - c^{12}\Delta_j^1 \le w_{ji}^2$$

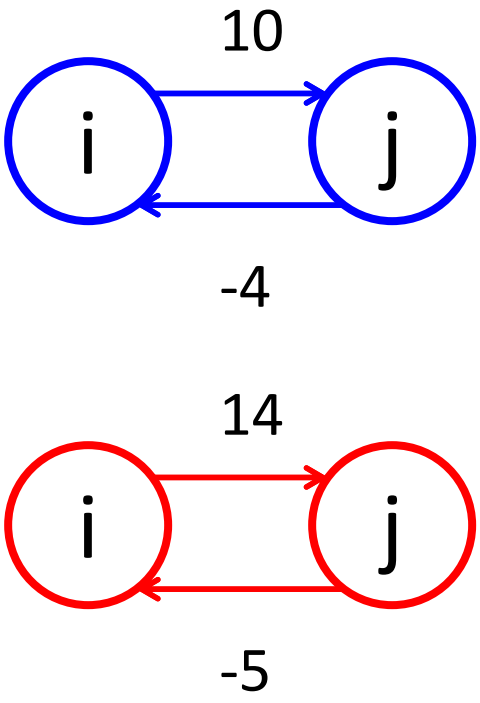
$$\Delta_j^1 - \Delta_i^1 \le \frac{w_{ij}^2}{c^{12}}$$

Scenario reduction

$$\Delta_i^1 - \Delta_j^1 \le \min_{s \in S} \frac{w_{ji}^s}{c^{1s}}$$

Proposed Reduced Slack Graph (rSG)

|S| Slack Graphs

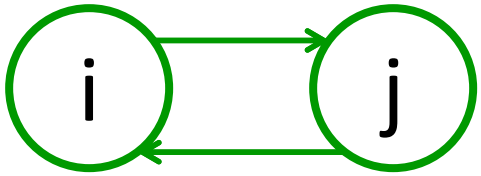


Linearization of delay adjustments

$$\Delta^2 = c^{12}\Delta^1$$
$$c^{12} = 2$$

One Reduced Slack Graph (rSG)

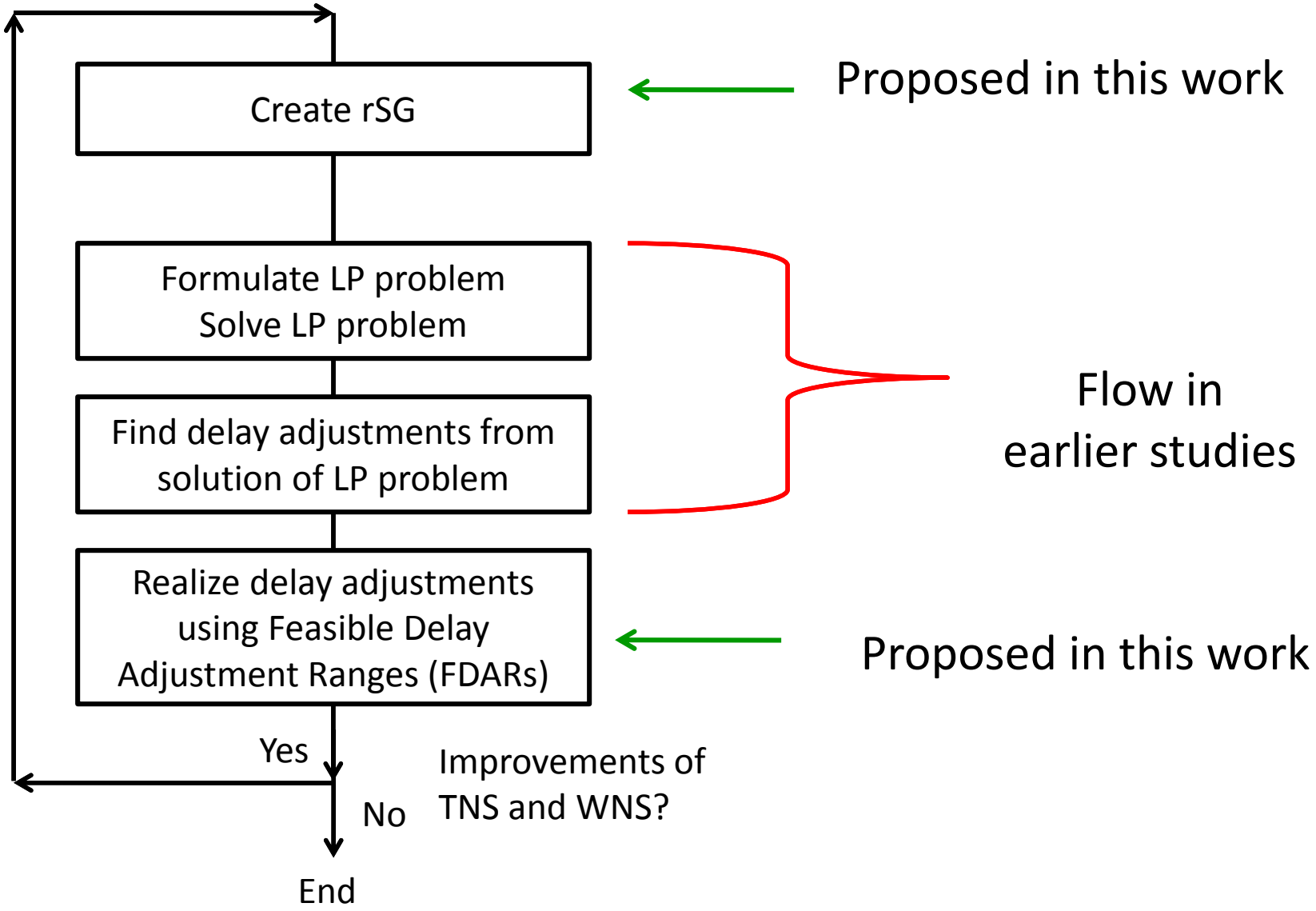
min{10,14/2} = 7



min{-4, -5/2} = -4

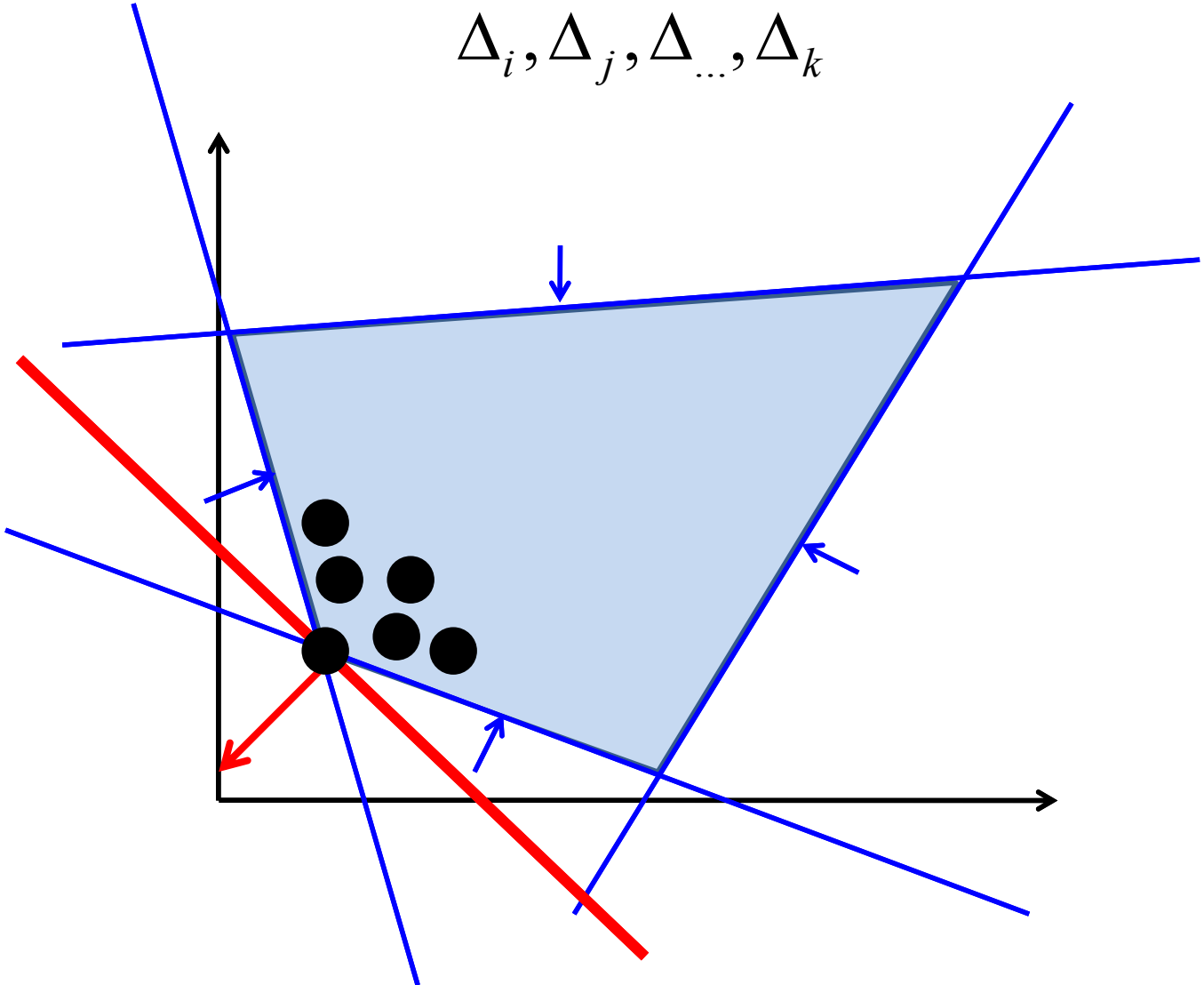
[10] J. Lu and B. Taskin. Post-CTS clock skew scheduling with limited delay buffering. In Circuits and Systems, pages 224–227, 2009.

Modified CTO Flow



LP solution

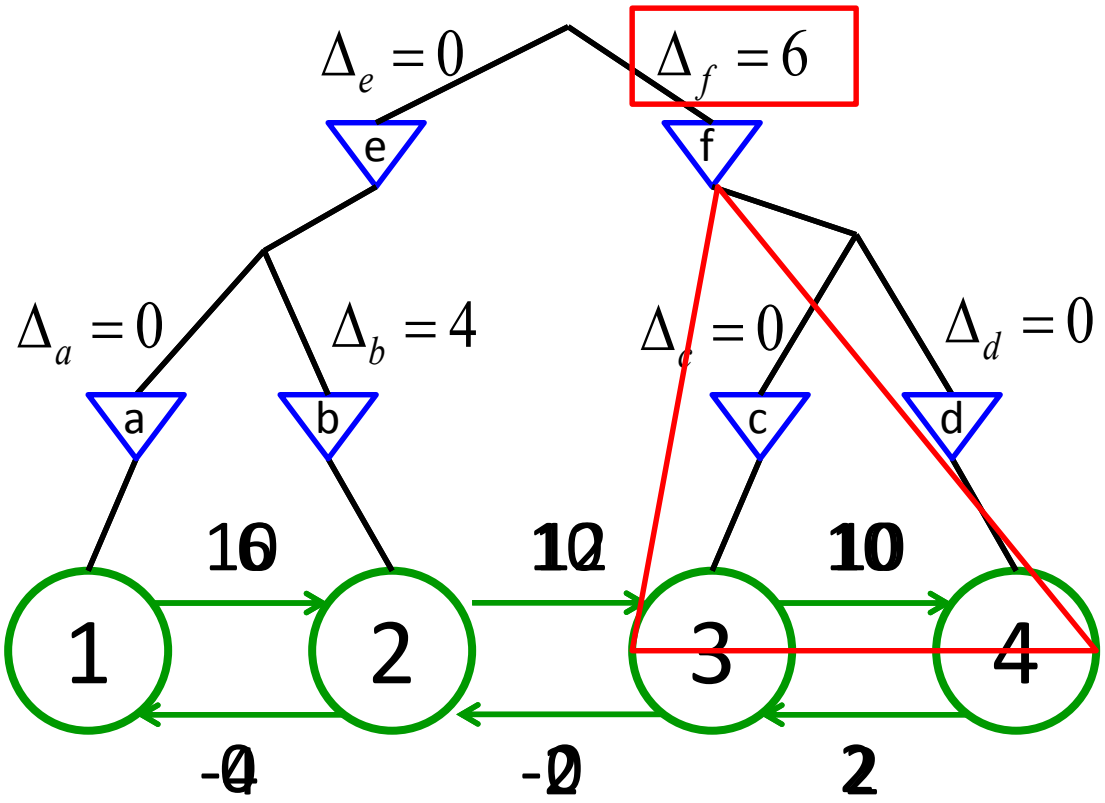
$$\Delta_i, \Delta_j, \Delta_{...}, \Delta_k$$



Feasible Delay Adjustment Ranges (FDARs)

$$FDAR_{\Delta_f} = [\Delta_f - w_{b_f}^{out}, \Delta_f + w_{b_f}^{in}]$$

$$FDAR_{\Delta_f} = [6-0, 6+10] = [6, 16]$$



Experimental Evaluation

- Circuits [3] based on Open Cores verilog spec.[11]
- Optimization guided by (estimates) TNS and WNS
  - Linear estimates of OCV on a path
- Evaluation using Monte Carlo framework
  - OCV similar to in the ISPD 2010 contest.
  - Variations generated using quad tree
  - Performance measured in Yield

[11] OpenCores. http://opencores.net/. 2014.

[3] R. Ewetz, S. Janarthanan, and C.-K. Koh. Benchmark circuits for clock scheduling and synthesis. https://purr.purdue.edu/publications/1759, 2015.

CTO guided by TNS and WNS

Circuits	Structure	TNS/WNS (ps/ps)	Cap (pF)	Run-time (min)
mcmm_fpu	pre-CTO	220/22	3.23	15
	post-CTO	0/0	3.37	25
	CT in [4]	177/27	3.78	8
	RCT in [4]	79/14	4.12	6
mcmm_ecg	pre-CTO	184/18	16.76	66
	post-CTO	0/0	16.89	92
	CT in [4]	1914/30	17.27	53
	RCT in [4]	1335/21	17.92	37
mcmm_aes	pre-CTO	2147/29	46.68	224
	post-CTO	462/9	48.73	326
	CT in [4]	8702/77	61.59	131
	RCT in [4]	3208/43	83.06	198

[4] R. Ewetz, S. Janarthanan, and C.-K. Koh. Construction of reconfigurable clock trees for MCMM designs. DAC'15, 2015.

CTO Evaluation in Yield

Circuits	Structure	Yield (%)	Cap (pF)	Run-time (min)
mcmm_fpu	pre-CTO	87.3	3.23	15
	post-CTO	100.0	3.37	25
	CT in [4]	67.6	3.78	8
	RCT in [4]	98.8	4.12	6
mcmm_ecg	pre-CTO	98.4	16.76	66
	post-CTO	100.0	16.89	92
	CT in [4]	94.0	17.27	53
	RCT in [4]	99.6	17.92	37
mcmm_aes	pre-CTO	71.2	46.68	224
	post-CTO	99.3	48.73	326
	CT in [4]	16.7	61.59	131
	RCT in [4]	99.1	83.06	198

[4] R. Ewetz, S. Janarthanan, and C.-K. Koh. Construction of reconfigurable clock trees for MCMM designs. DAC'15, 2015.

Summary and Questions

- Defined a reduced slack graph to capture MCMM constraints
- Use FDARs to realize delay adjustments
- High yield at low capacitive overhead
- Future work
  - Investigate making topological changes