NICS 清華大學

Tsinghua University

CP-FPGA:Computation Data-Aware Software/Hardware Co-design for Nonvolatile FPGAs based on Checkpointing Techniques

Zhe Yuan, Yongpan Liu, Hehe Li, Huazhong Yang

2015/1/28

Outline

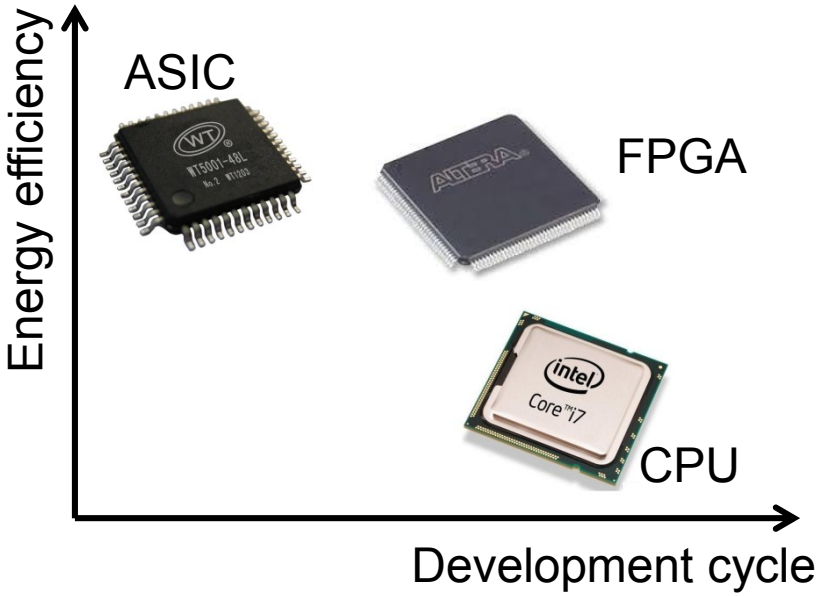
- Background
- Architecture Design
- Software Schemes
- System Evaluation
- Conclusion

IOT applications

- Internet of things(IoT)
  - Wearable devices
  - Structure health monitoring
  - Smart transportation
  - Etc..

Silicon Chips for IoT

- Chips——bricks of IoT



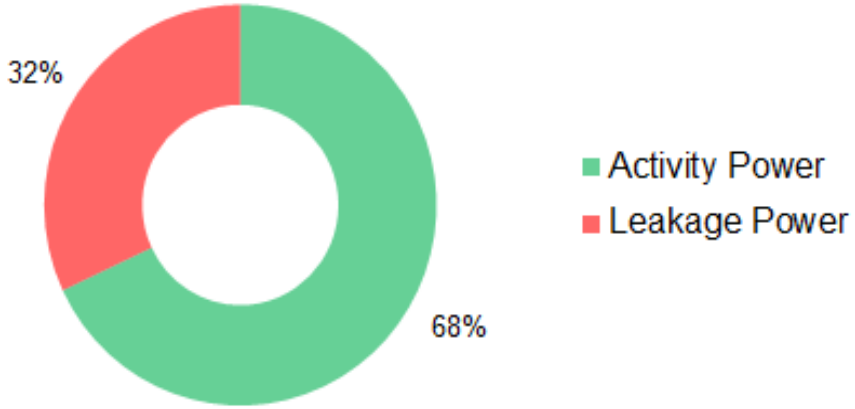
A chip

high energy efficiency

short development cycle

Challenge of FPGA

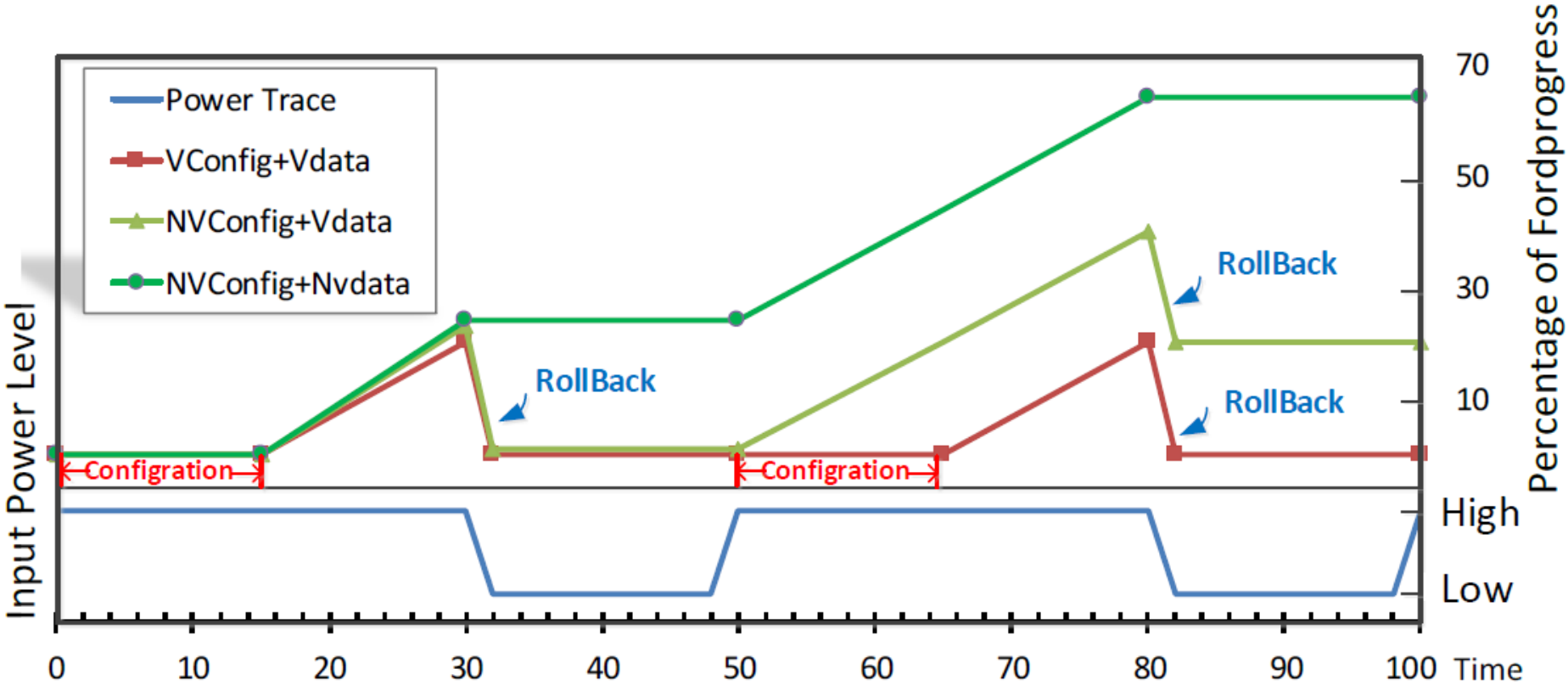
- Large Leakage
  - 1/3 total power(activity)
  - Dominate power consumption(idle)
- Power Gating
  - Reduce Leakage
  - Large Overhead
    - Reconfiguration
    - Rollback



[FPGA Power Simulation by VTR]

Nonvolatile FPGA

- Nonvolatile Configuration + Volatile Computation
- Nonvolatile Configuration + Nonvolatile Computation



This work

- Target
  - Nonvolatile FPGA
- Technology
  - Checkpoint
- Main Steps
  - A hardware architecture
  - A set of software schemes
    - Map application
    - Reduce redundant data

Outline

- Background
- Architecture Design
- Software Schemes
- System Evaluation
- Conclusion

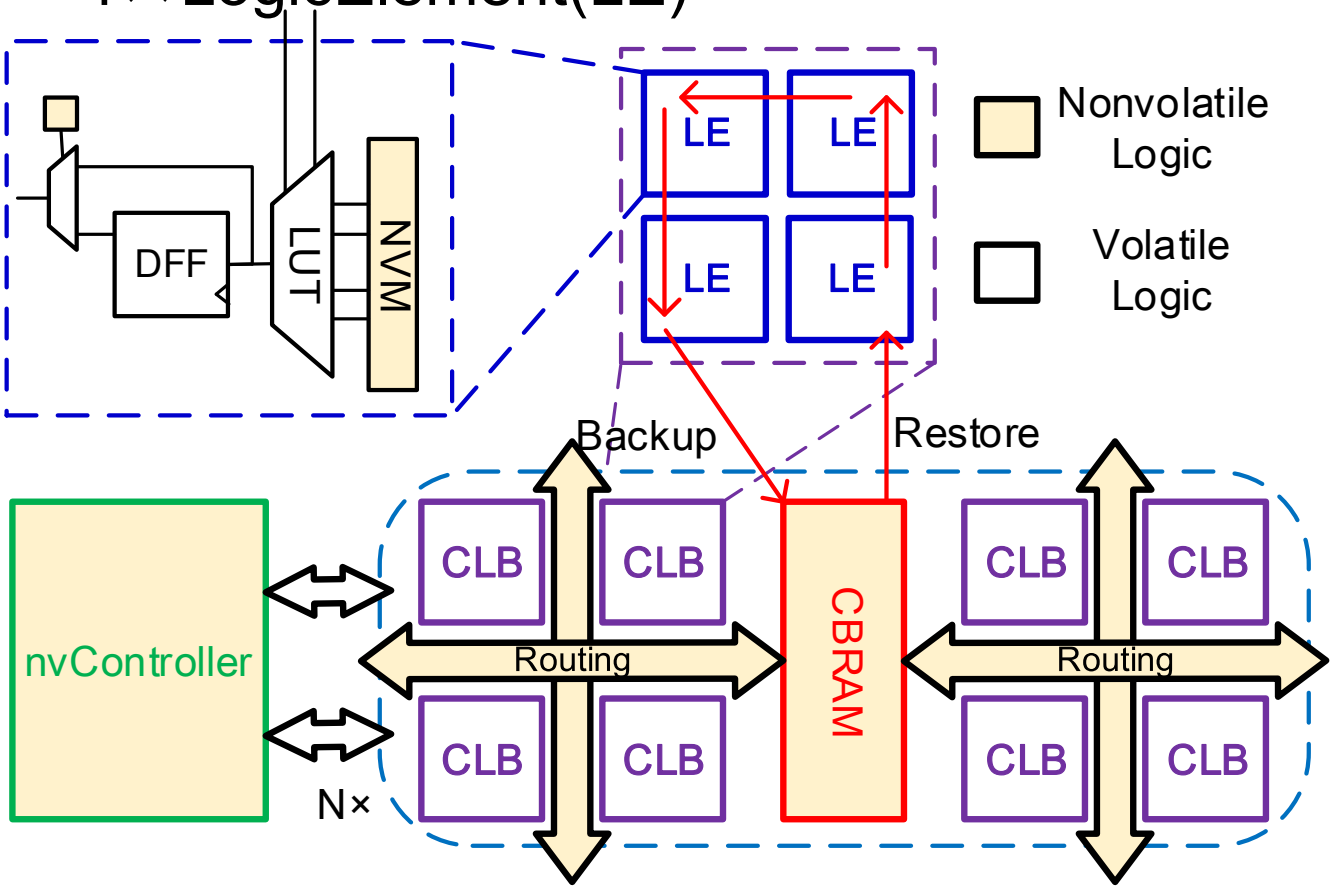
Architecture Overview

- CPFPGA = Island FPGA + nvController

N×(8×CLB + Routing + CBRAM)

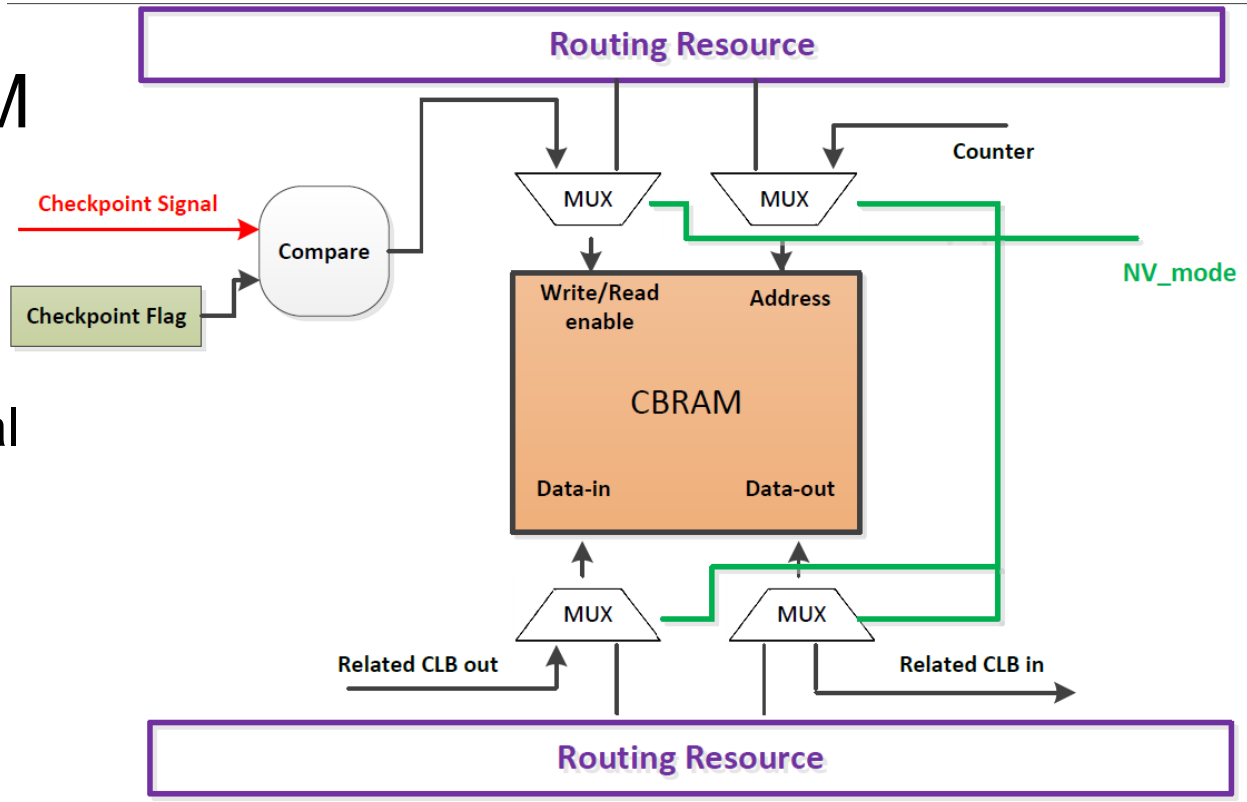
Two new module

4×LogicElement(LE)



Checkpoint BRAM

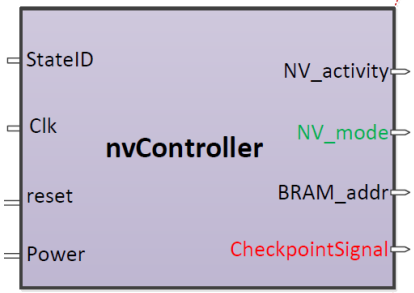
- Checkpoint BRAM
  - Backup/Restore
  - Data Reduction
    - Checkpoint Signal
    - Checkpoint Flag

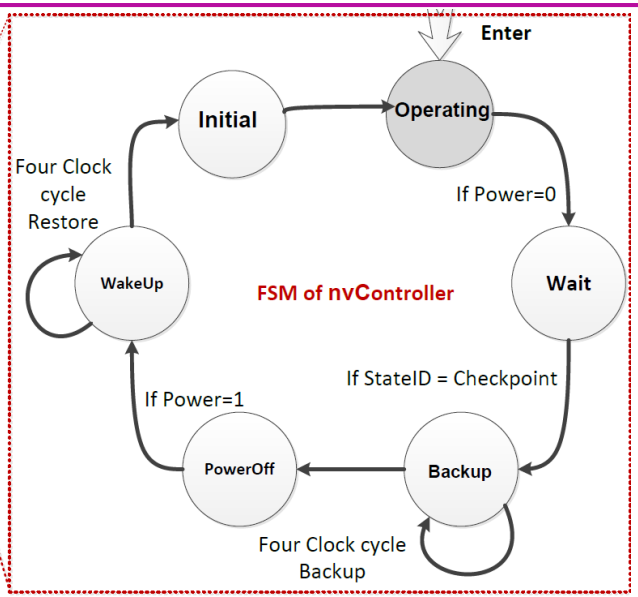


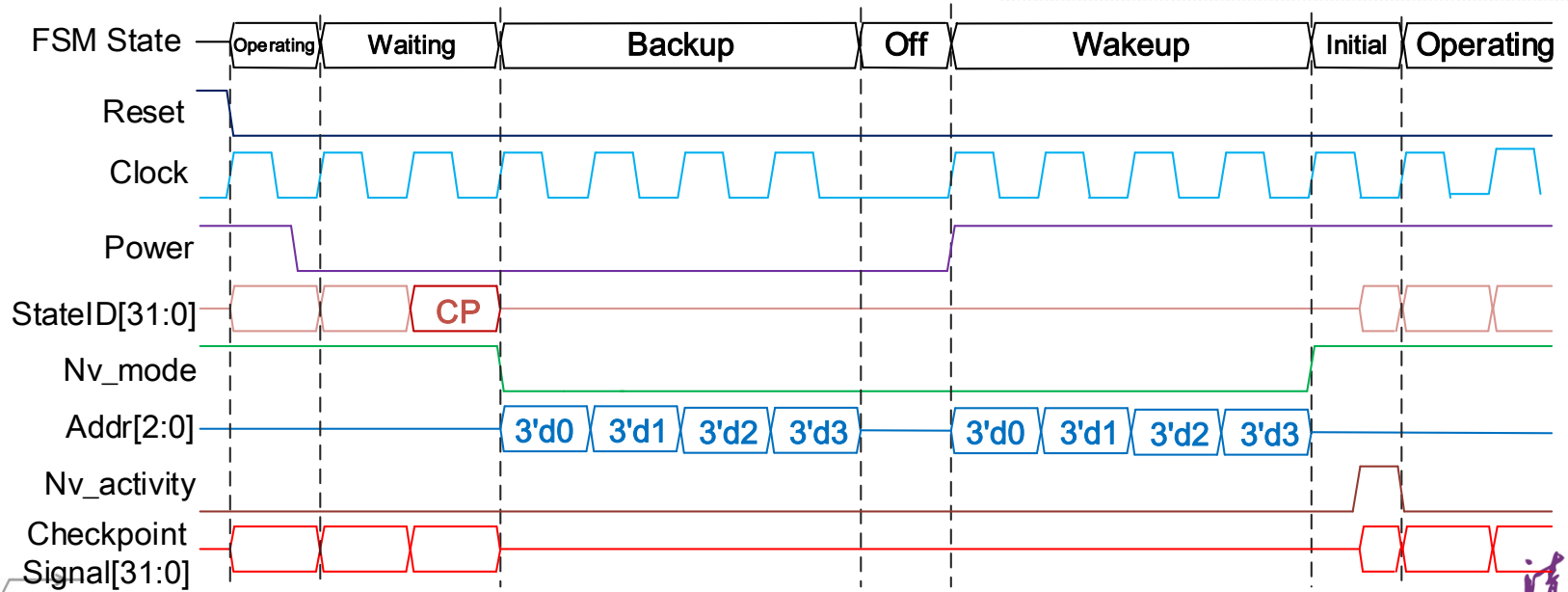
BRAM State	NV mode	Operation	Write Enable	Address[31:0]	Data-in[7:0]	Data-out[7:0]
Checkpoint BRAM	1	Backup	Checkpoint Signal[31:0] &Checkpoint Flag[31:0]	Counter[2:0]	CLB_OUT[7:0]	X
		Restore	0	Counter[2:0]	X	CLB_IN[7:0]

nvController

- FSM
  - Six Different States





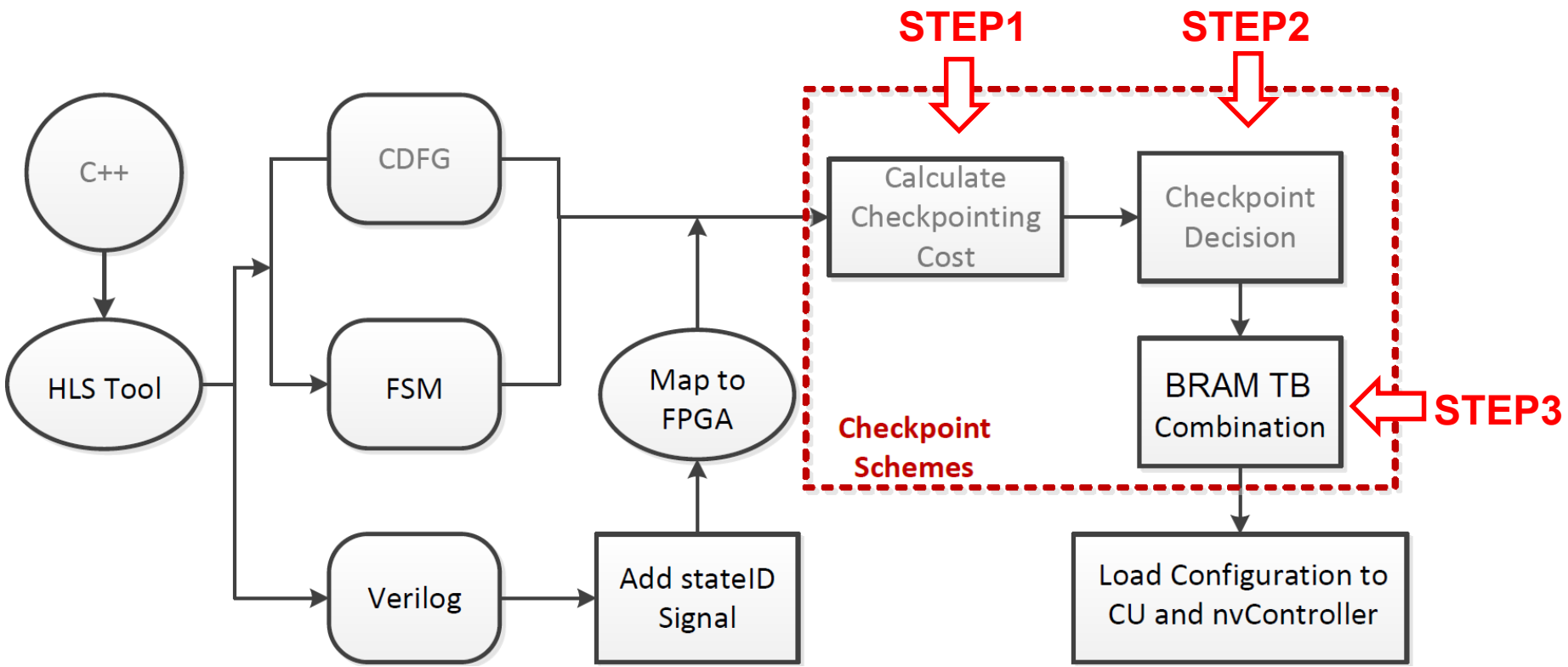


Outline

- Background
- Architecture Design
- Software Schemes
- System Evaluation
- Conclusion

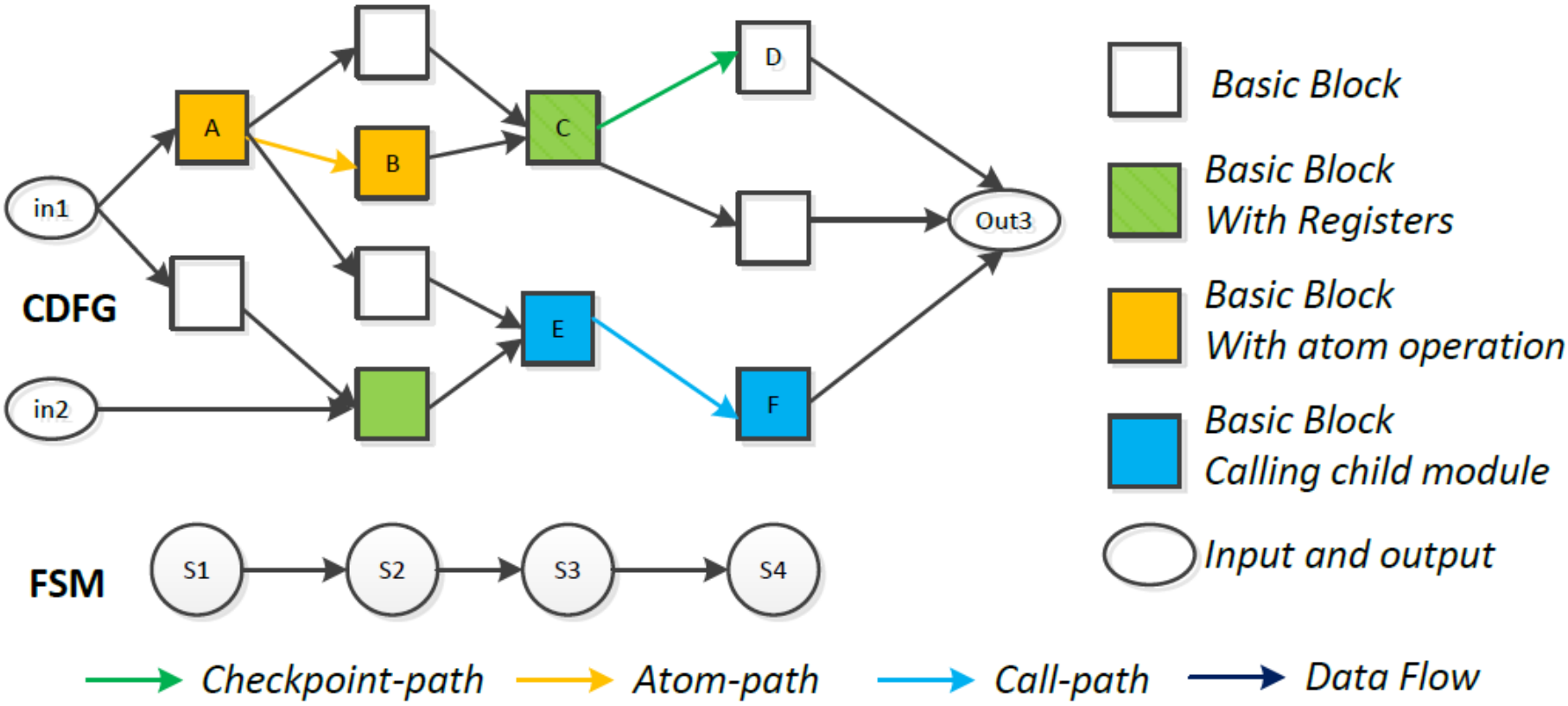
Software Overview

– Map an application to proposed architecture

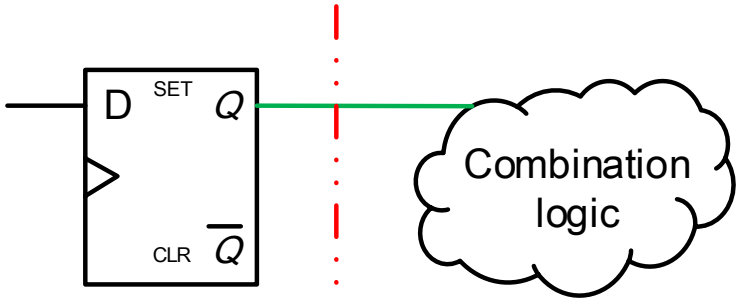


STEP1：Checkpoint Cost

– Checkpoint Cost Ci: Data need to backup

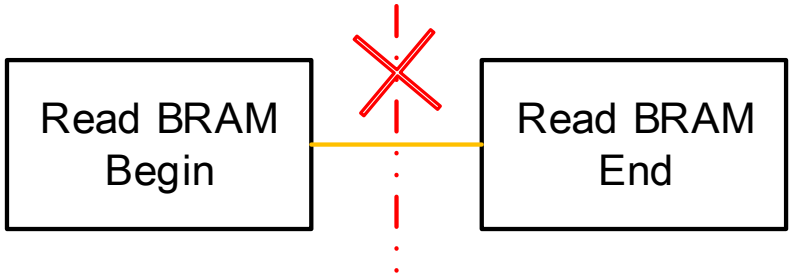


STEP1：Checkpoint Cost



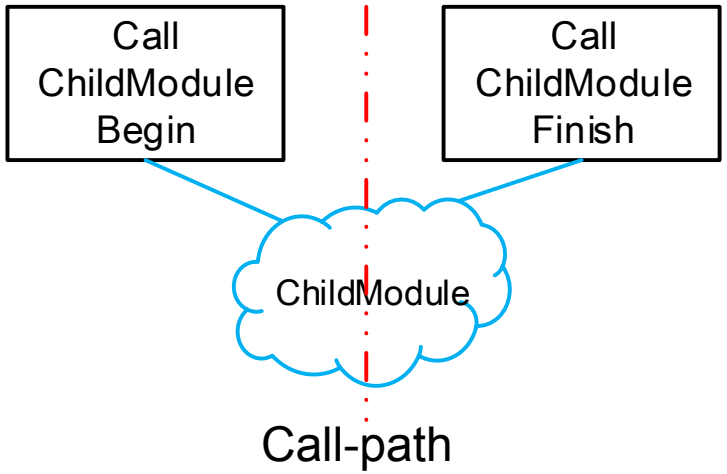
Checkpoint-path

Cost = Cost + 1



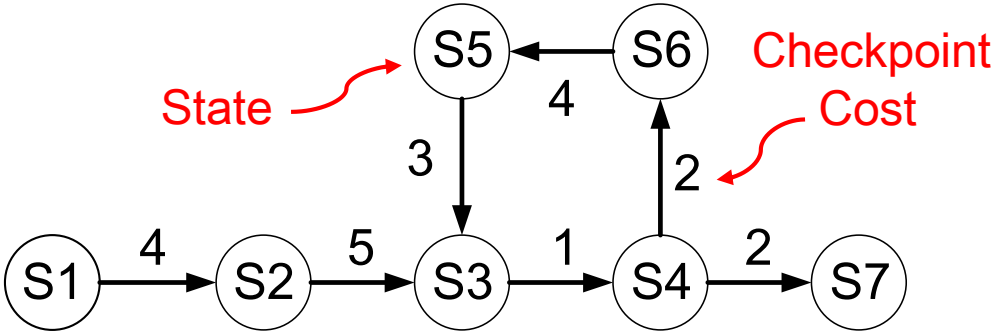
Atom-path

Avoid insert checkpoint



Call-path

Cost = Cost + Cost(ChildModule)



STEP2:Checkpoint Decision

- Choose a set of checkpoints from FSM

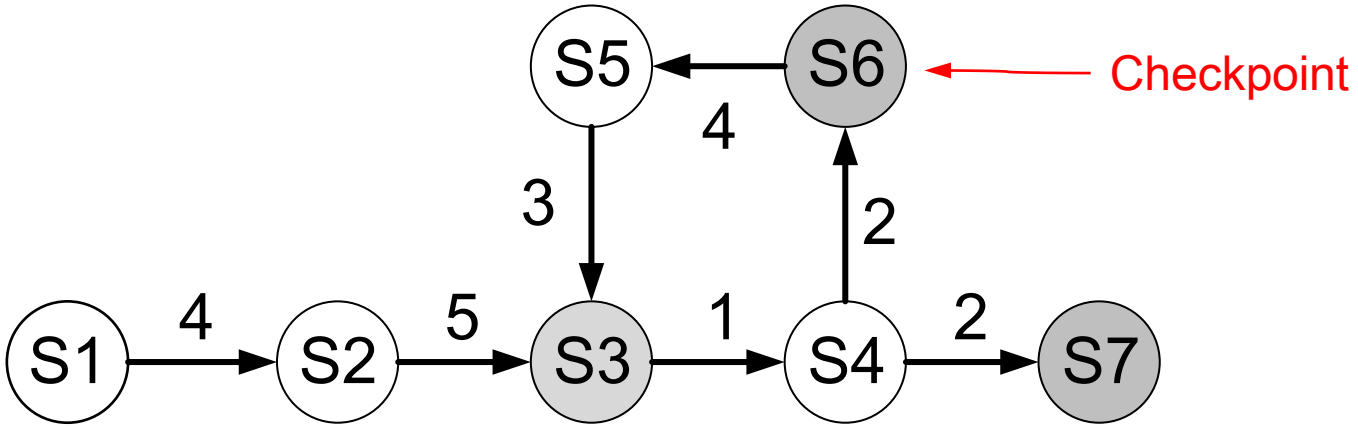
$$\min \sum_{\forall i} U_i b_i$$

bi =1 If state i is chose as a checkpoint

$$U_i = \frac{\alpha(D - d_i)}{D} + \frac{\beta c_i}{CostM}$$

$$s.t. \forall b_m b_n = 1, |m - n| < D$$

D：Max Distance between two checkpoint



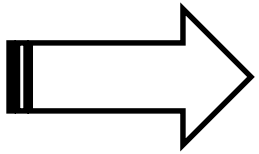
STEP3:BRAM Table Combination

- Similarity definition

$$S(X, Y) = \frac{\text{sizeof}(X \cap Y)}{\max\{\text{sizeof}(X), \text{sizeof}(Y)\}}$$

- An example:

Checkpoint	BRAM
1	1002
	1003
	1004
2	1008
	1009
3	1002
	1003
	1006



Checkpoint	BRAM
1,3	1002
	1003
	1004
	1006
2	1008
	1009

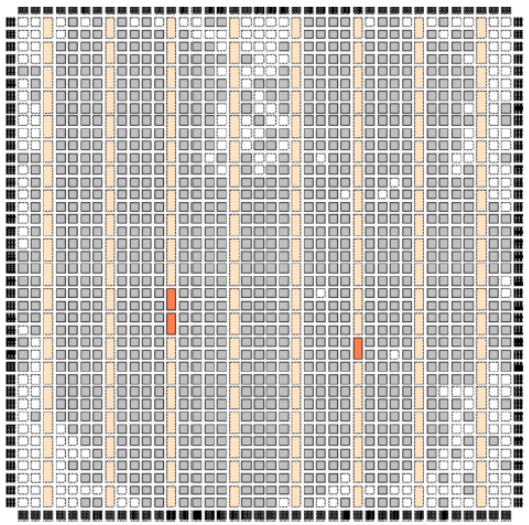
Outline

- Background
- Architecture Design
- Software Schemes
- System Evaluation
- Conclusion

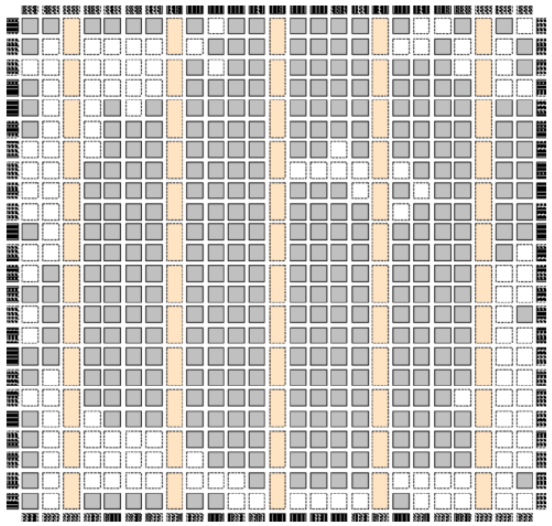
Experiment Setup

- Test Set
  - CHStone
  - MachSuite
- Tool
  - VivadoHLS2012
  - VTR7.0
  - Modelsim10.1a
- Clock
  - 100MHz

Benchmark	FIR	KMP	SORT	AES	SHA
CLB	90	151	359	1062	1323
total CLB	144	168	480	1280	1656
IO	69	173	342	154	130
total IO	432	464	784	1290	1456



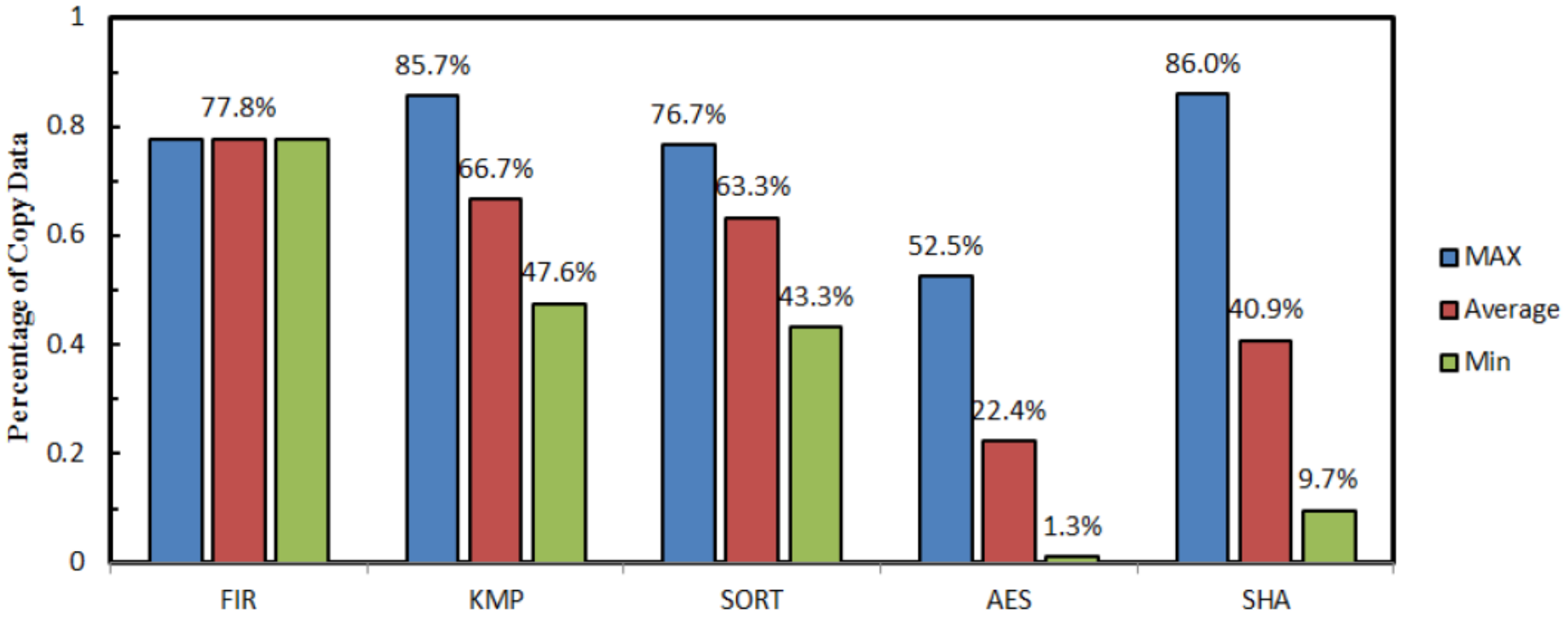
AES



Sort

Date Compression

– Compared to fully backup strategy

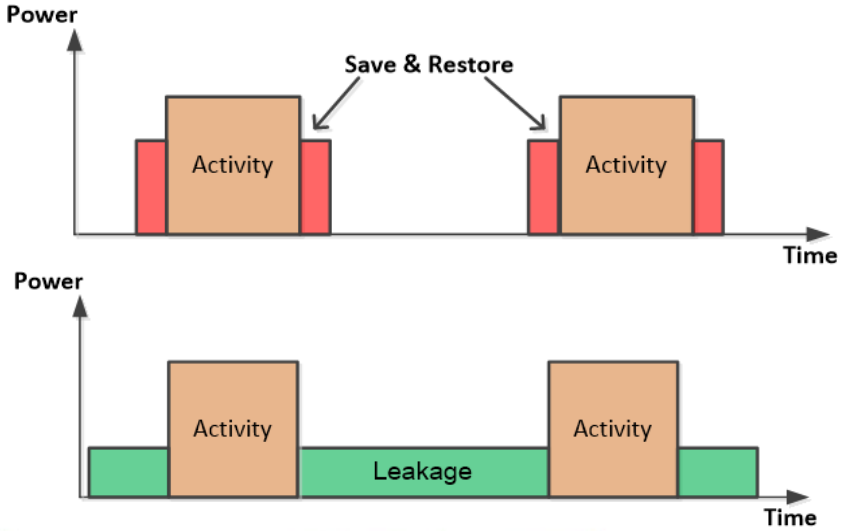


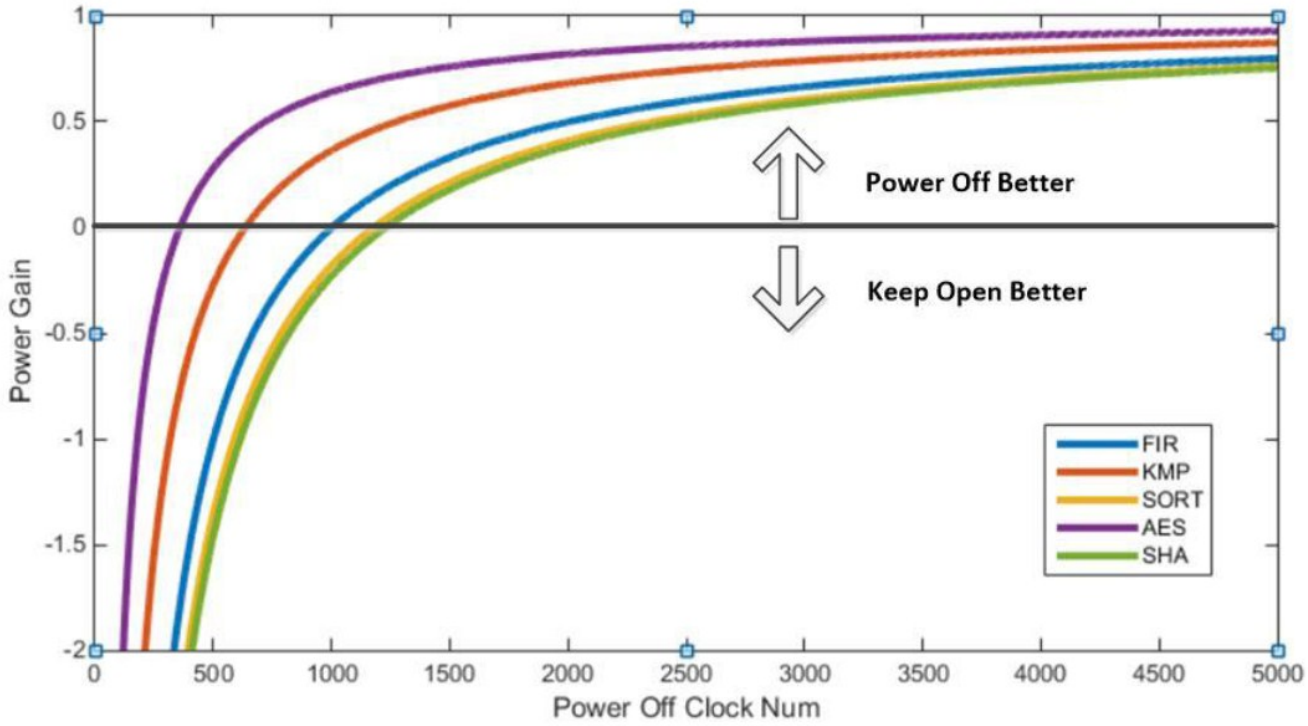
Worst Case： 24% Backup data is reduced.

Average Cases： 46% Backup data is reduced.

Power Management Strategy

- Breakeven time:
  - 1230 clock cycles
- Idle time>5000 clock cycles:
  - 60% power reduction





Outline

- Background
- Architecture Design
- Software Schemes
- System Evaluation
- Conclusion

Conclusion

Hardware

- New FPGA architecture based on checkpoint

Software

- Checkpoint schemes for proposed architecture

Results

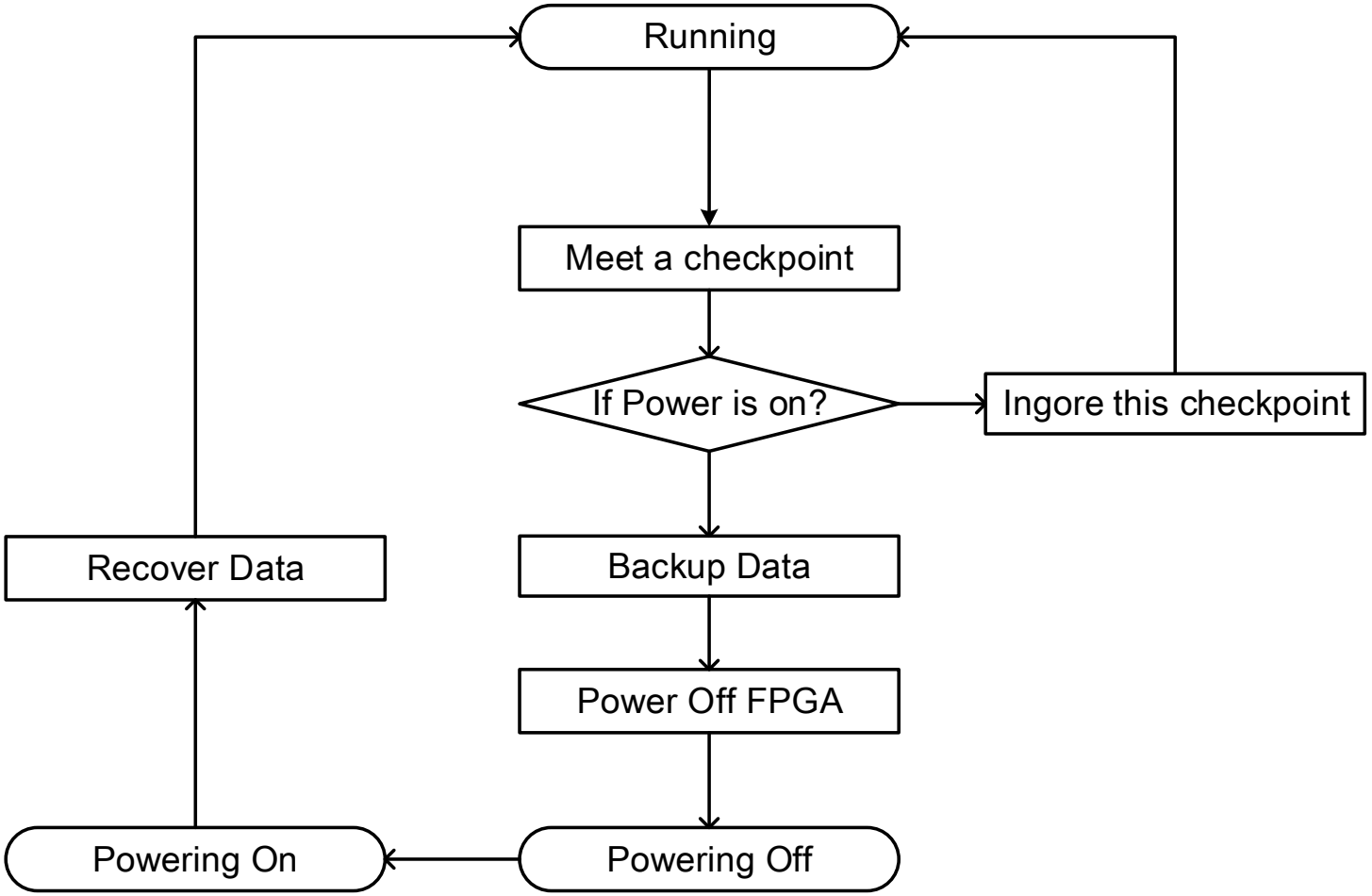
- 24%(worst) computation data reduction
- 46%(average) computation data reduction
- Power reduction under enough long idle time

Thank You !

Q&A

Appendix 1

- When to backup computation data into CBRAMs?



Appendix 2

- Sample Timeline of a benchmark