

Assessing CPA Resistance of AES with Different Fault Tolerance Mechanisms

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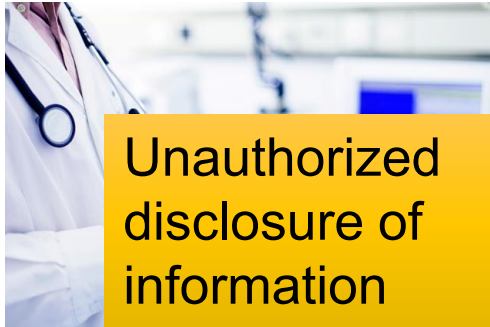
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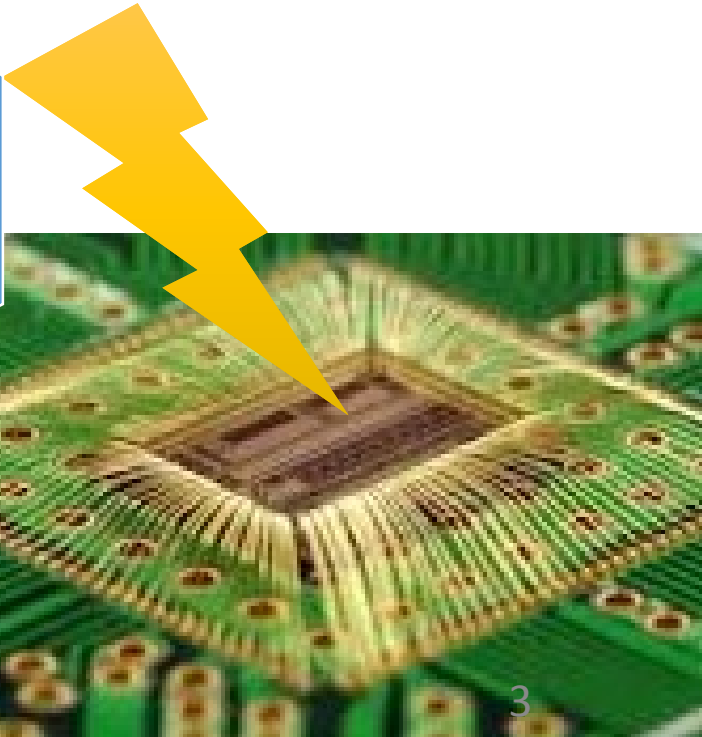
Outline

- Security threats on hardware
 - Fault attack
 - Side-channel attack (SCA)
 - Combined attack
- Impact of existing countermeasures for fault attack on cryptosystem against SCA
- Factors affect the efficiency of SCA

Security Challenges in IC



Unauthorized disclosure of information

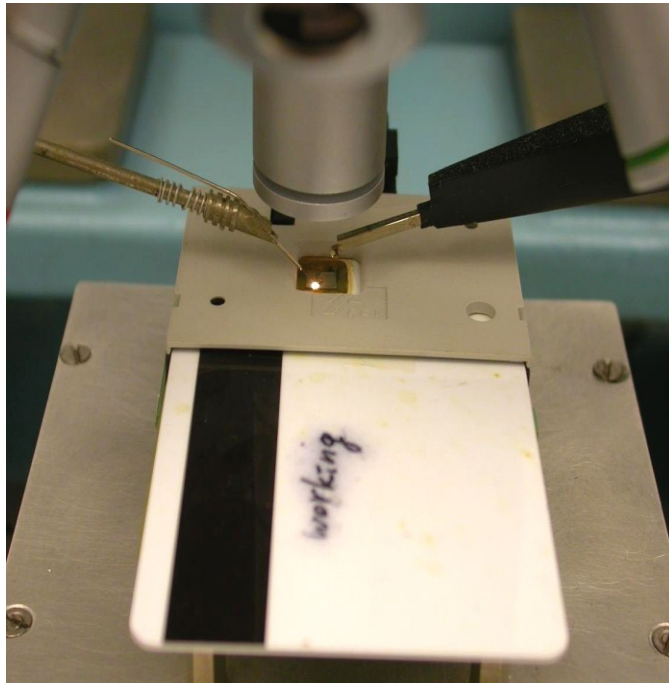


Unauthorized withholding of information

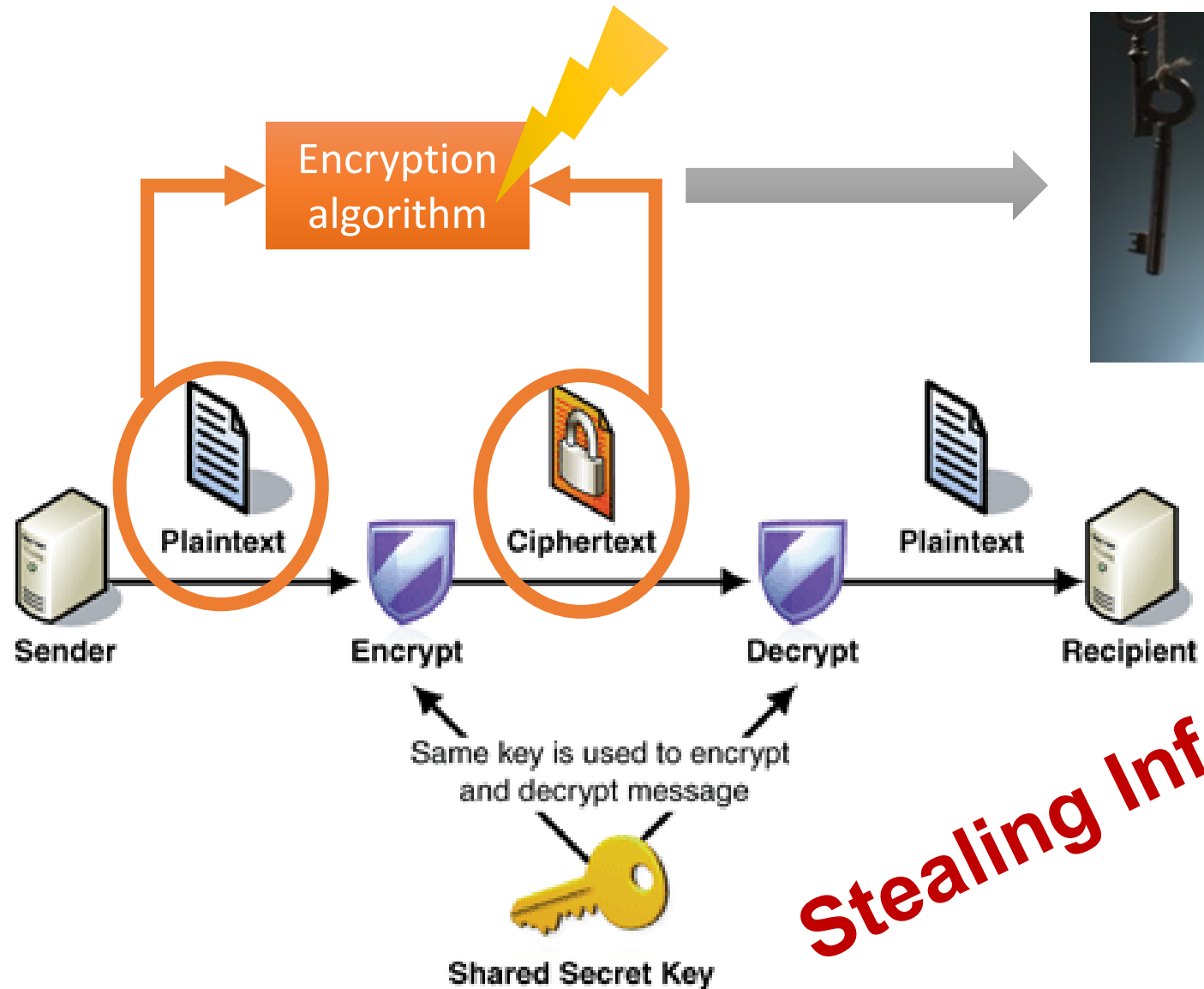


Unauthorized users access

IC Vulnerability to an Attack

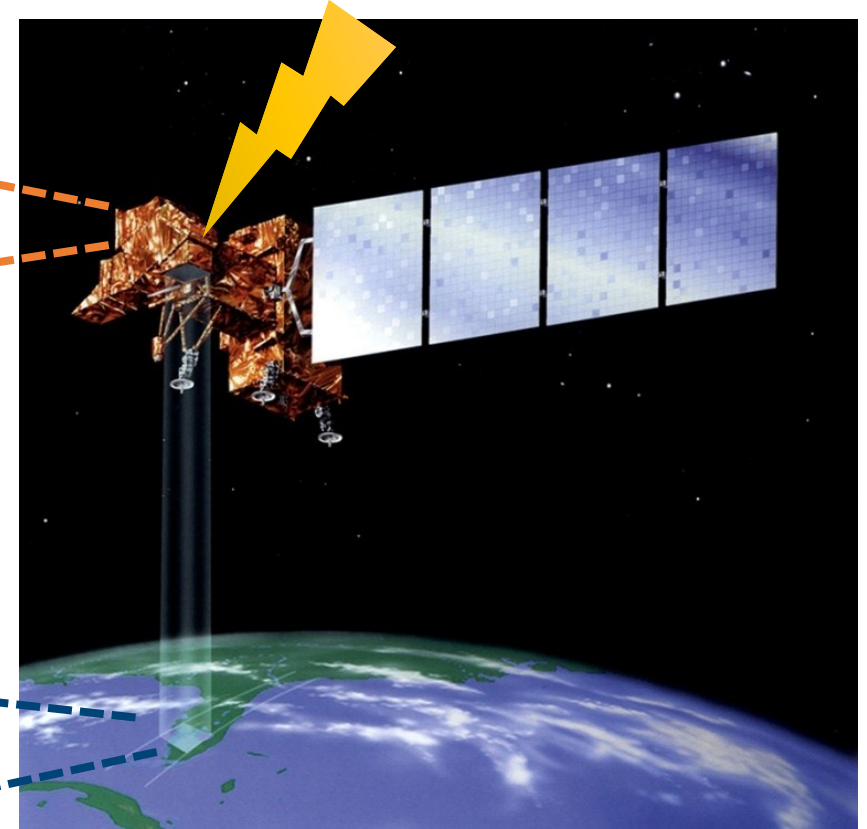
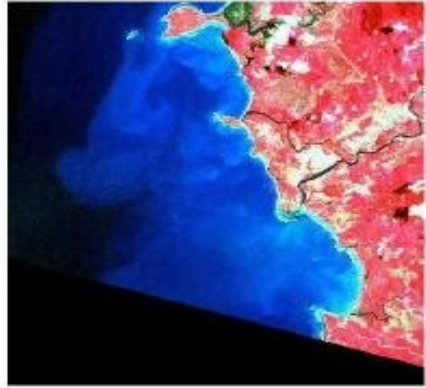


[1]



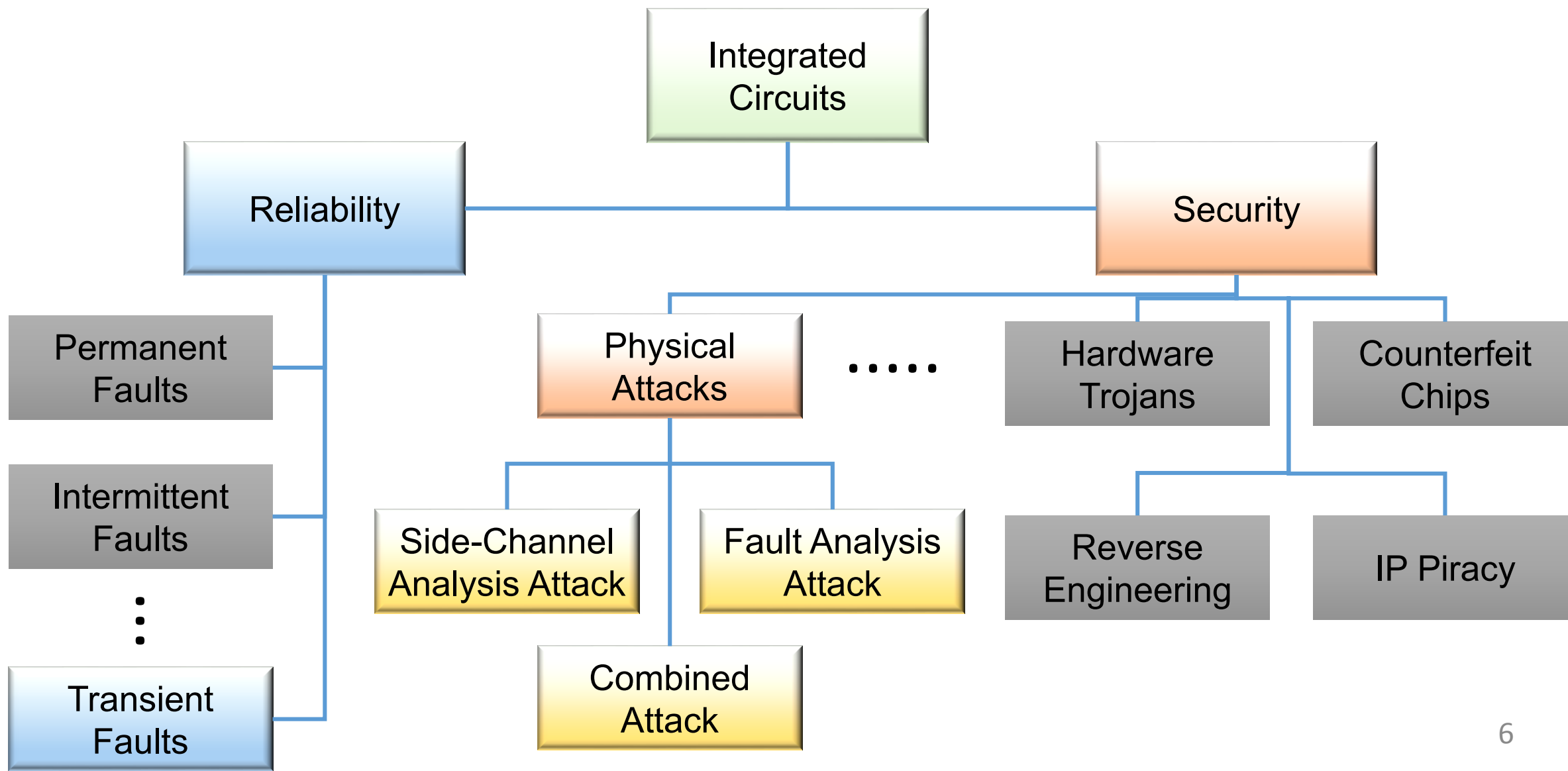
[1] S. Skorobogatov, ECRYPT II, 2011.

IC Vulnerability to Natural and Intentional Faults



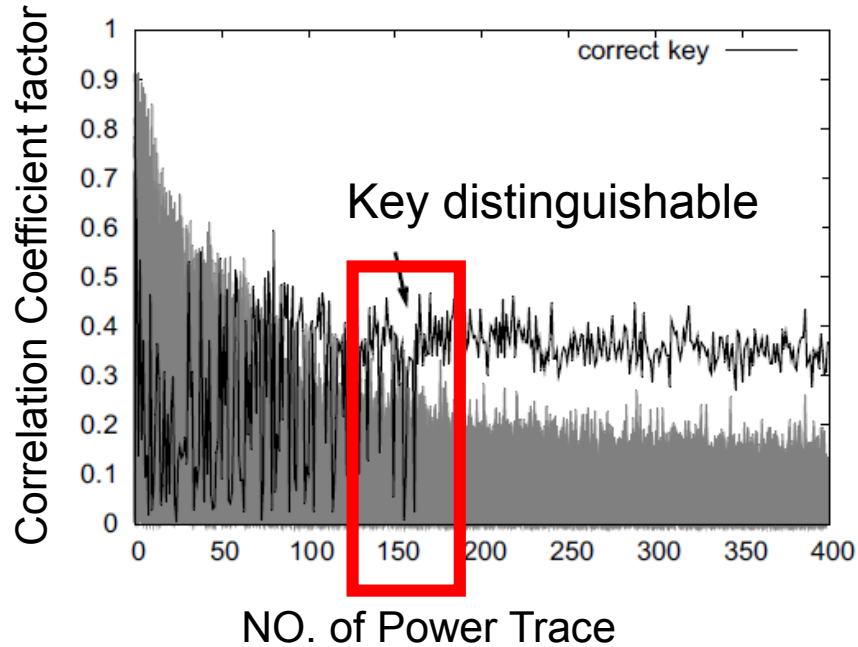
Denial of Service

Unified Framework for Reliability and Security of IC

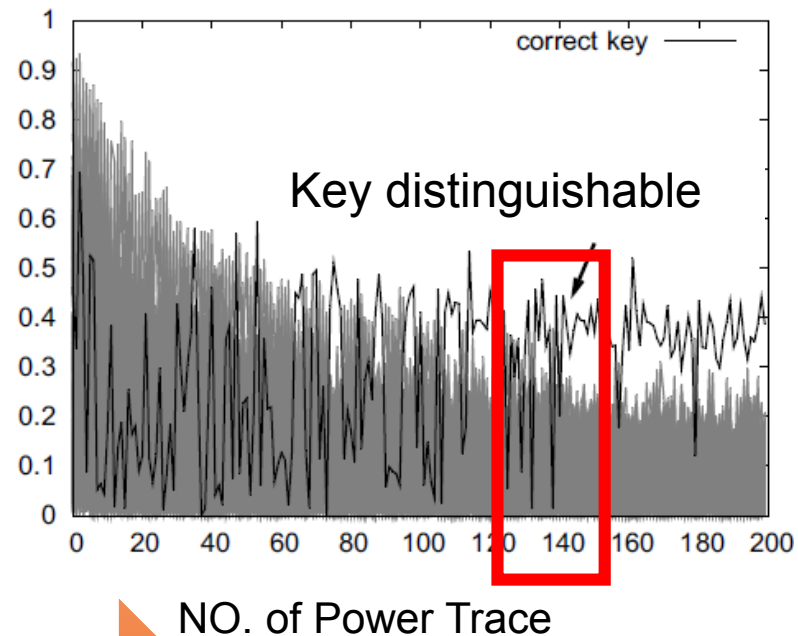


IC Security Vulnerability to Protection Circuits

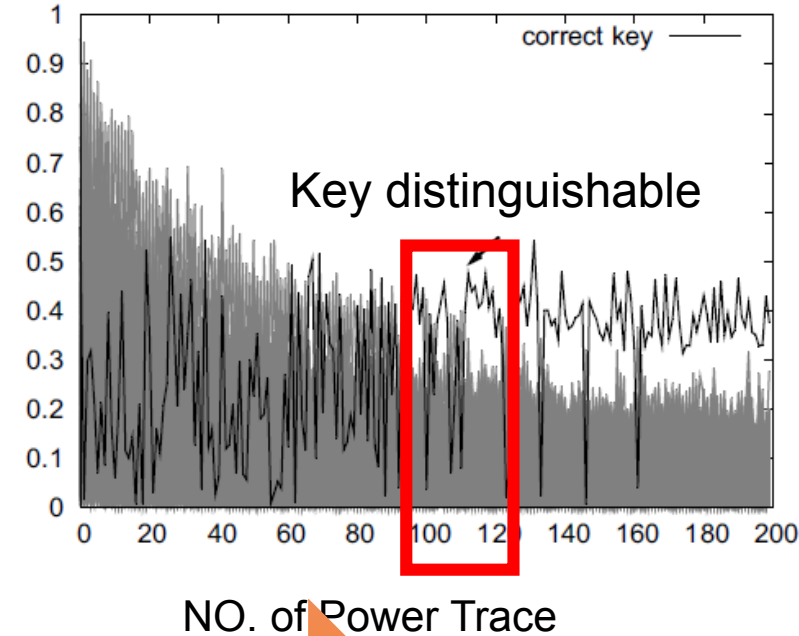
Attack on AES SBox, no fault detection method.



With parity based fault detection method.



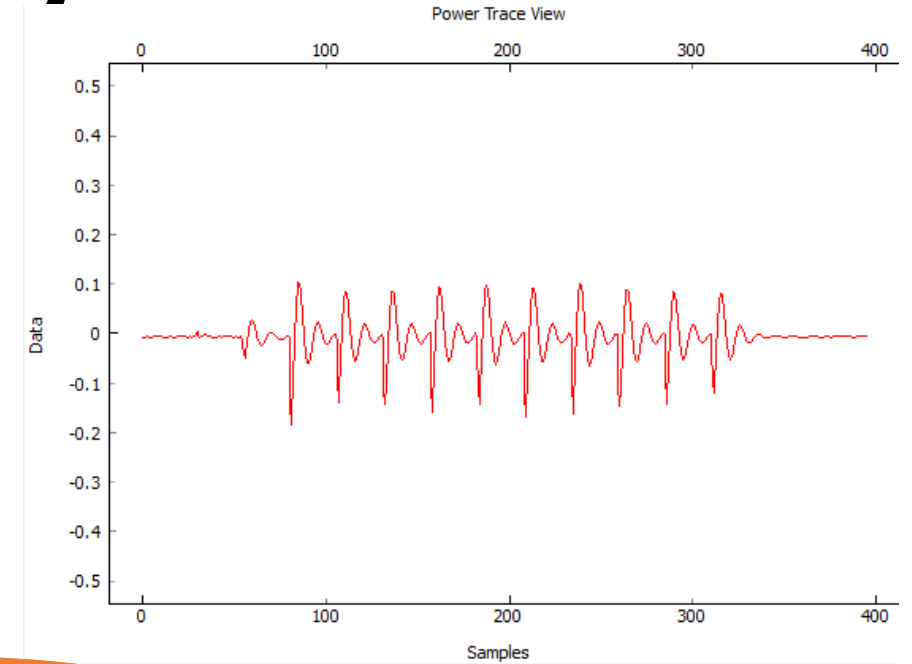
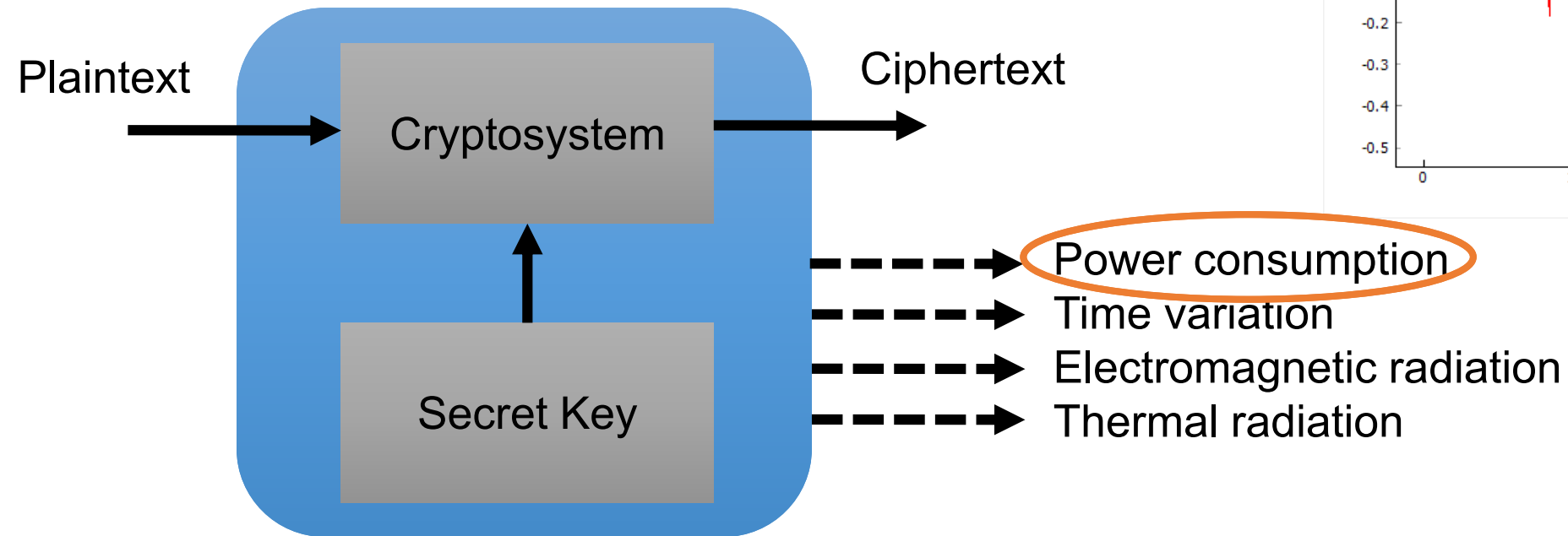
With residue code modulo 3 based fault detection method.



Adding Fault Detection Method

Stronger Fault Detection Method

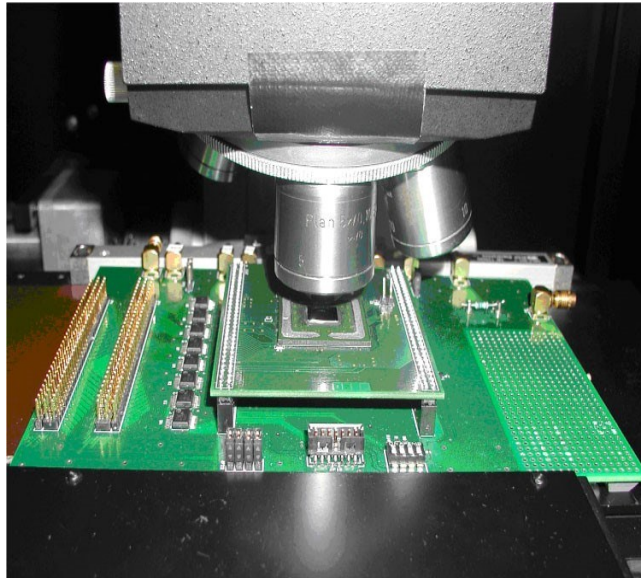
Side Channel Analysis Attack



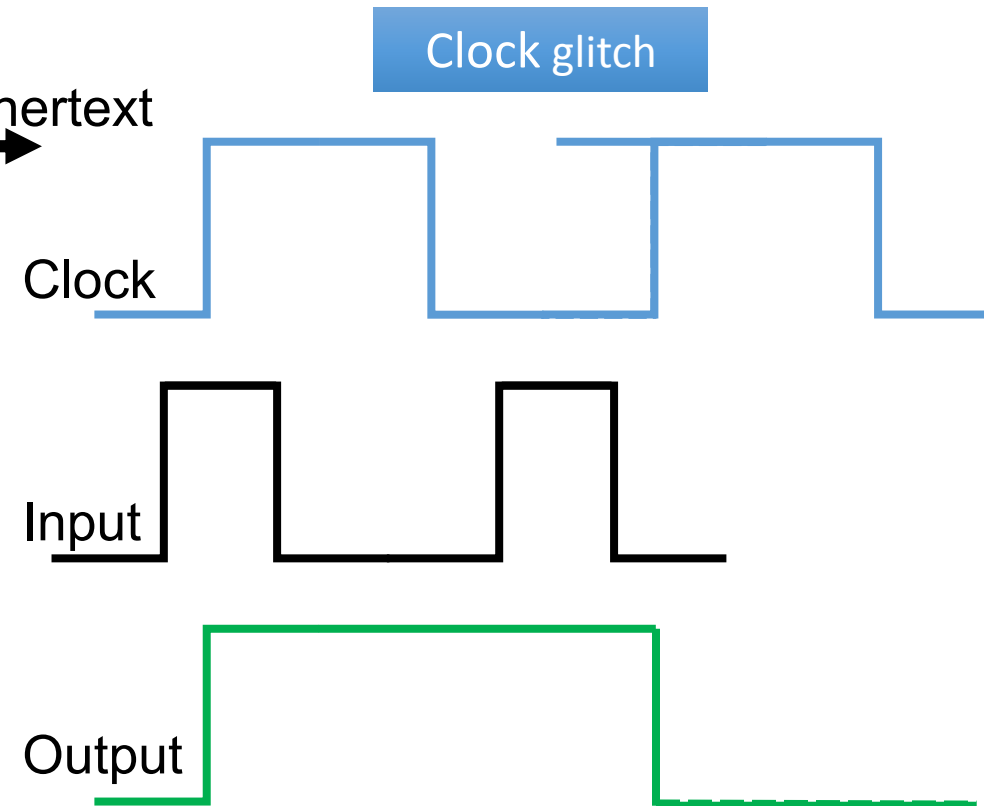
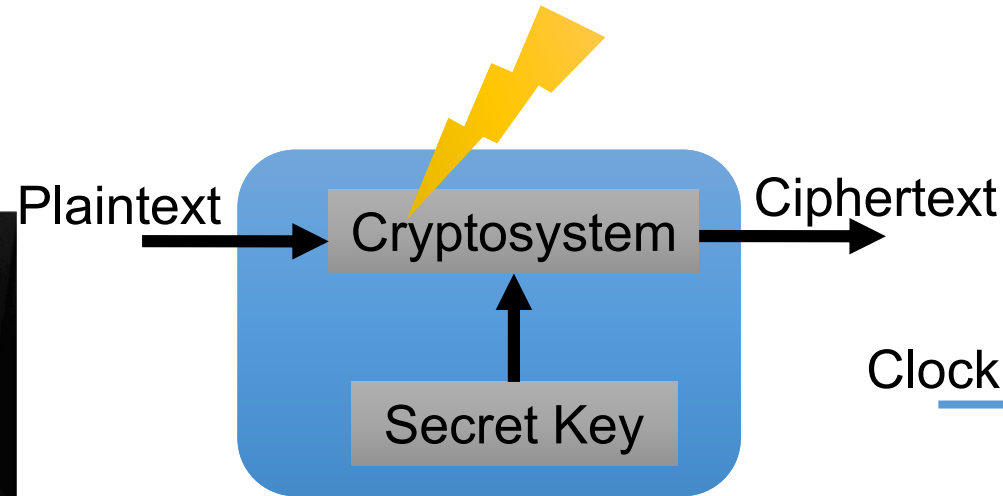
SCA Countermeasures

- Randomization (Masking)

Fault Analysis Attack



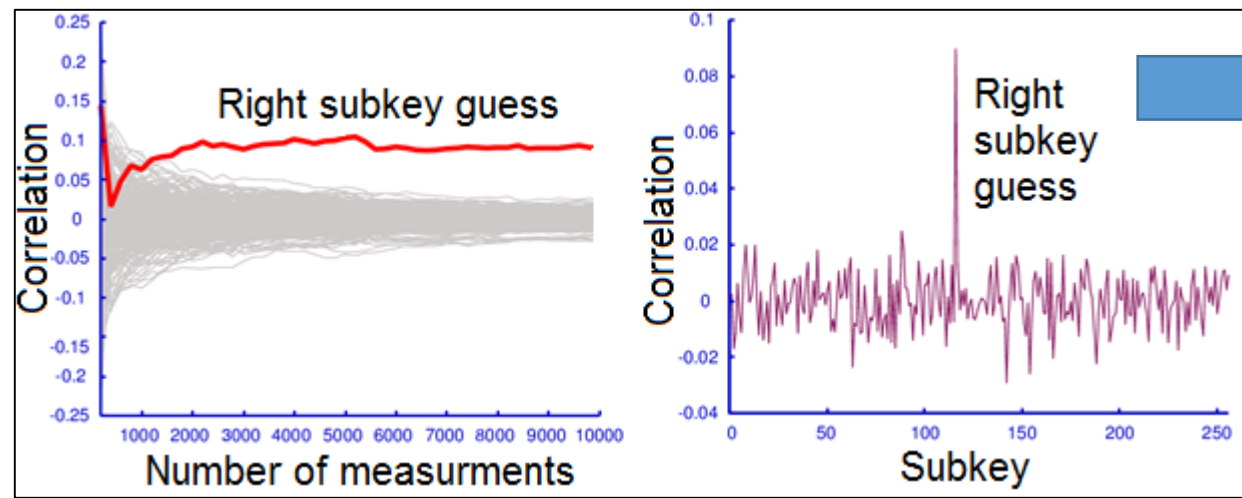
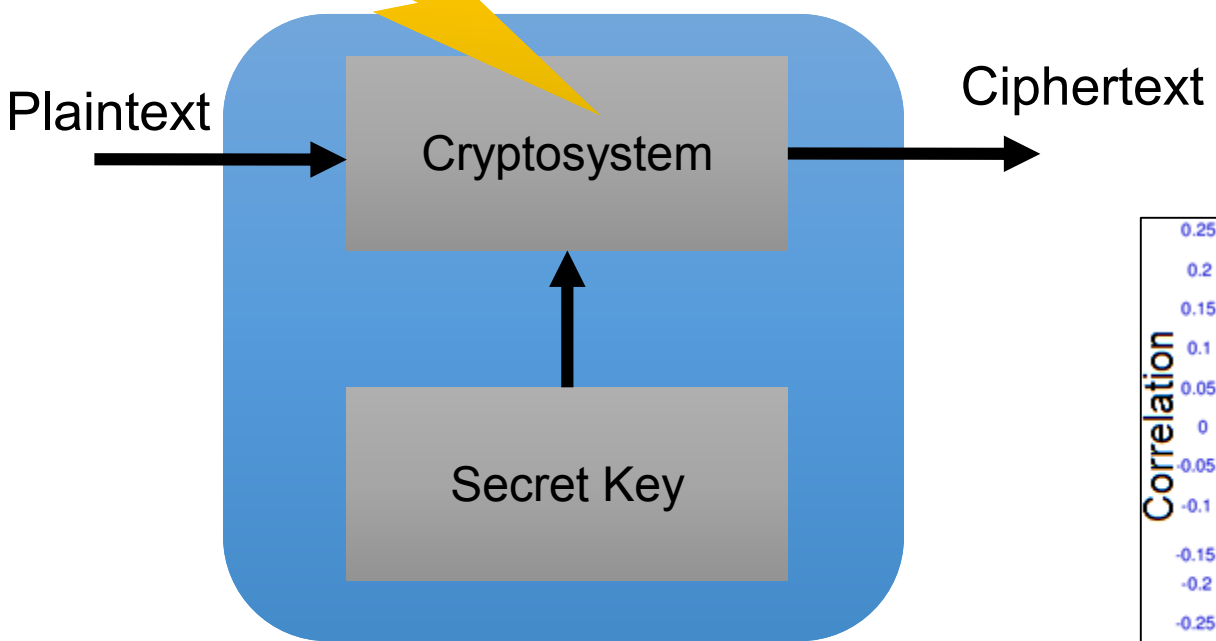
Laser fault injection equipment



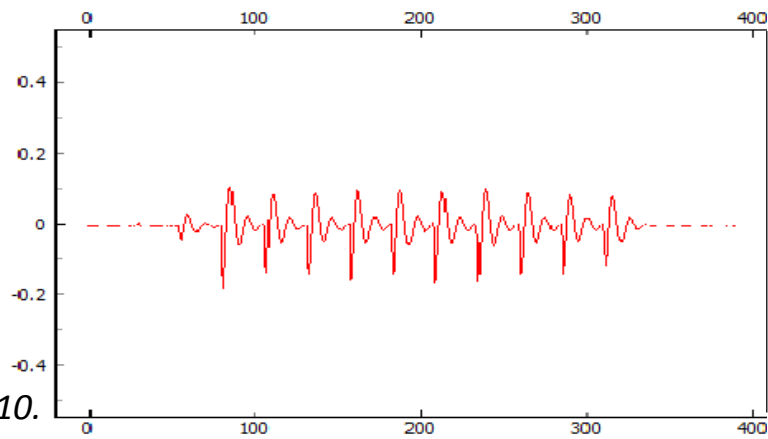
FA Countermeasures

- DMR
- Inverse function
- ECC

Combined Attack



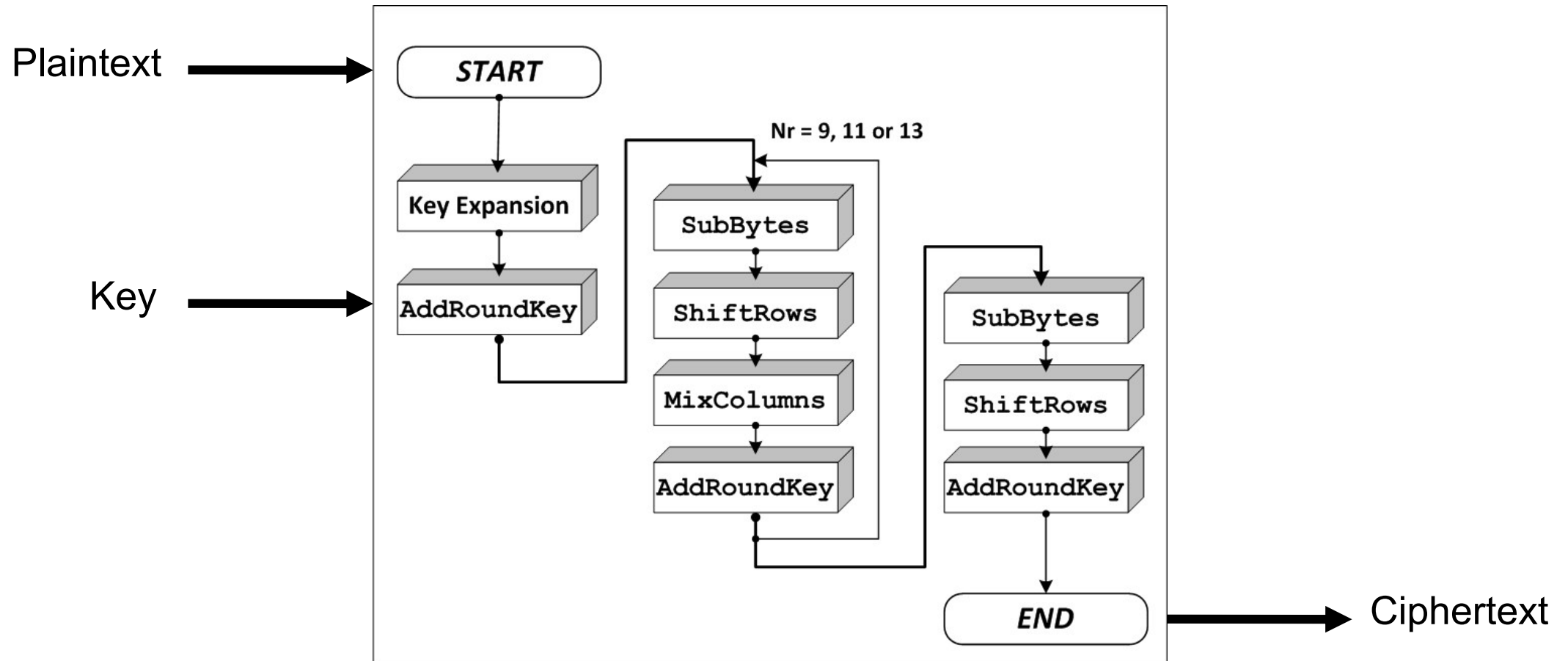
Power consumption



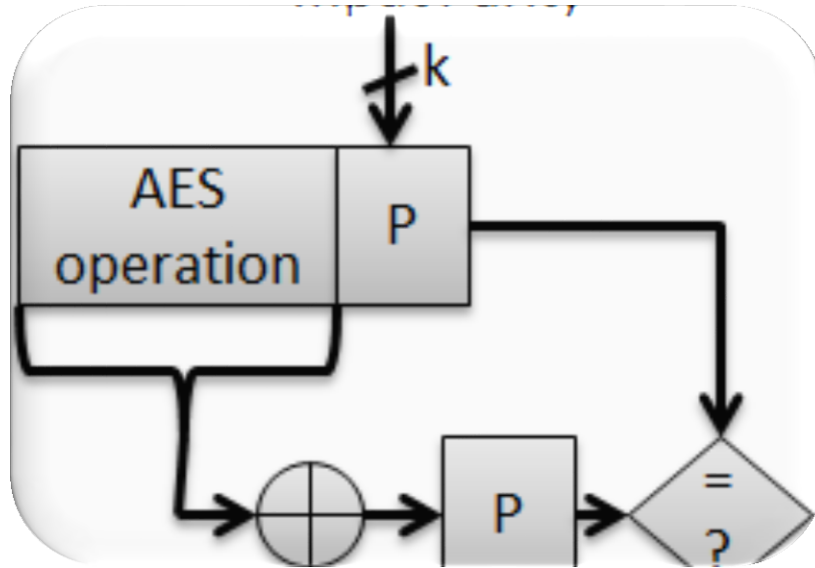
[REF]

[1] W. Hnath, J. Pettengill, *Major Qualifying Project*, 2010.

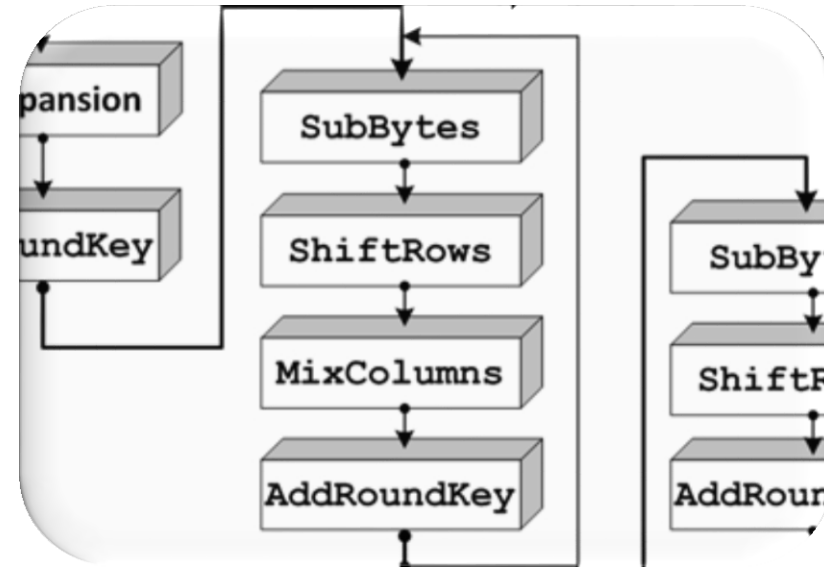
AES Cipher



Impact of existing countermeasures for fault attack on cryptosystem security



Different fault detection methods



Fault detection methods on different modules

Fault Detection Methods



[1]

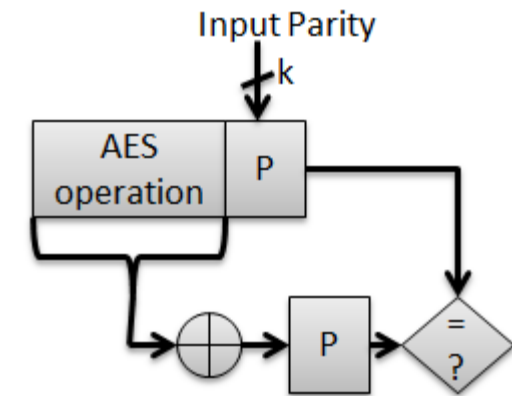
Double modular redundancy (DMR)

[1] G. Di Natale, et al., *JET*, 2009.

[2]

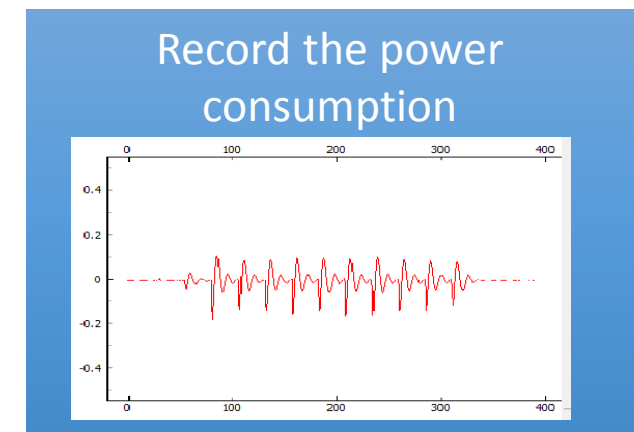
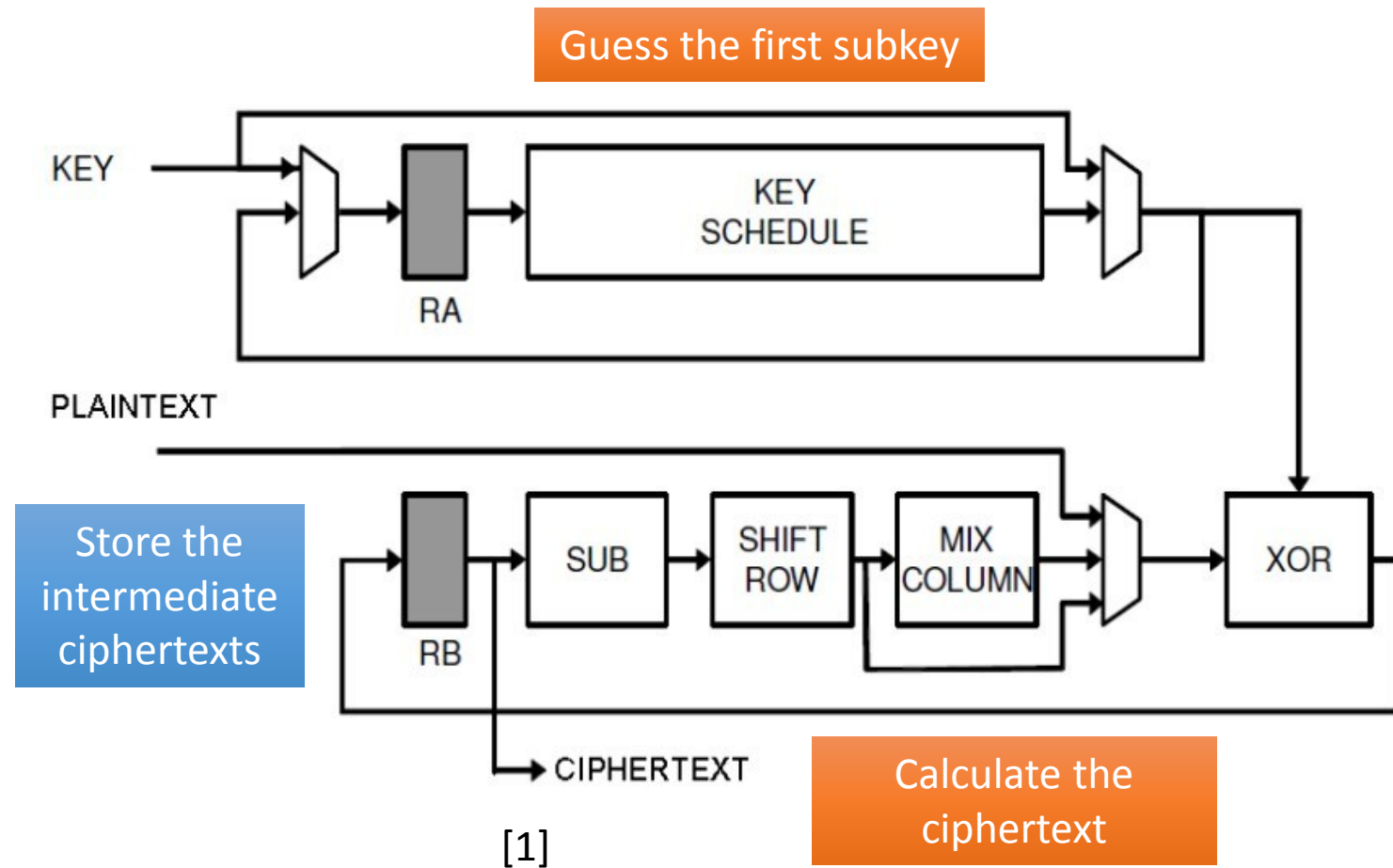
Inverse function

[2] R. Karri, et al., *DAC*, 2001.

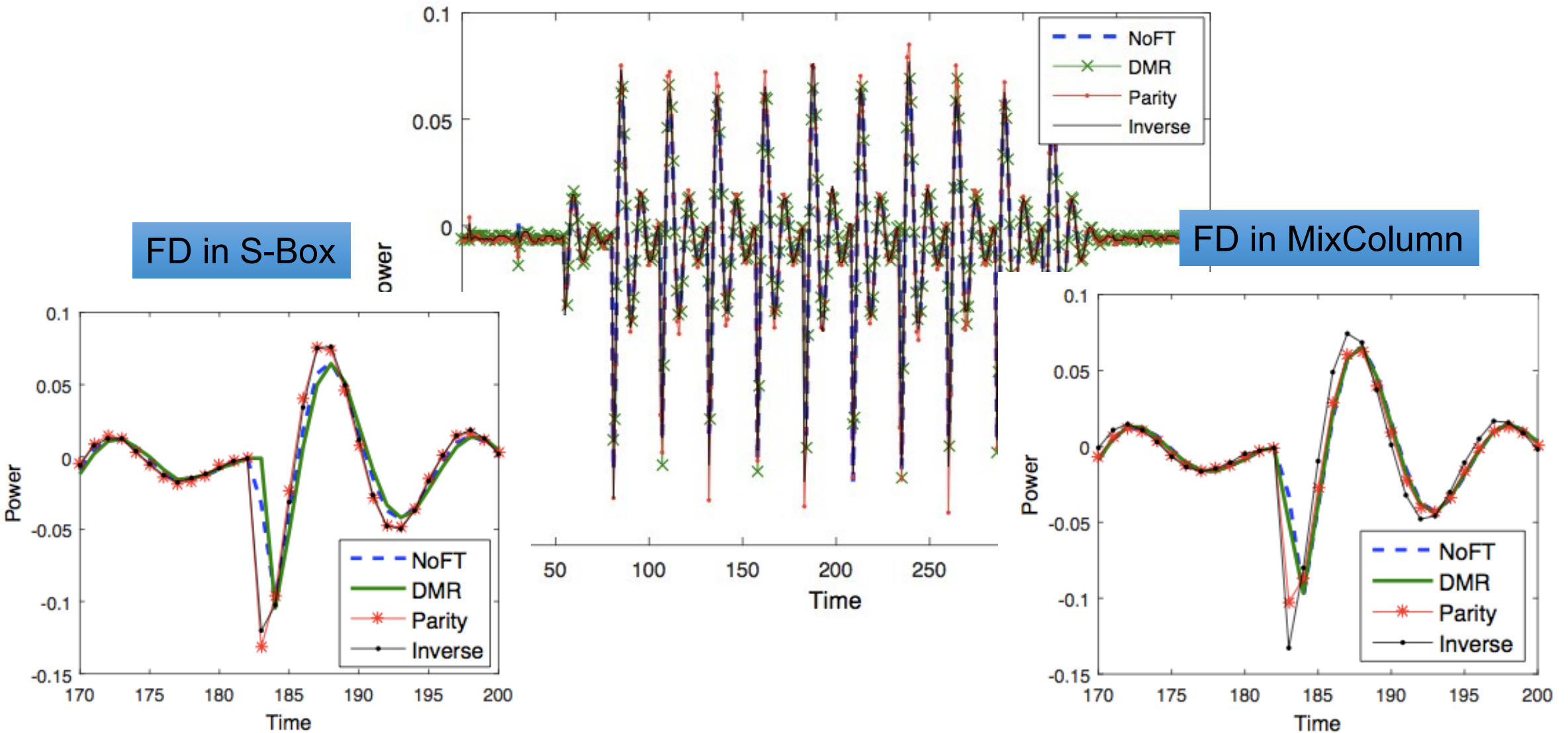


Parity check code

CPA Attack on AES



CPA Attack on AES

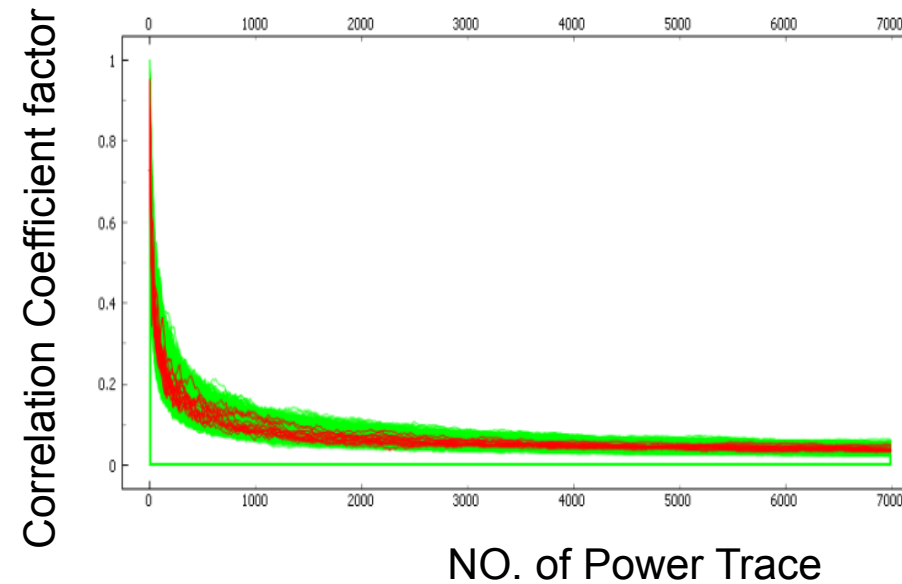
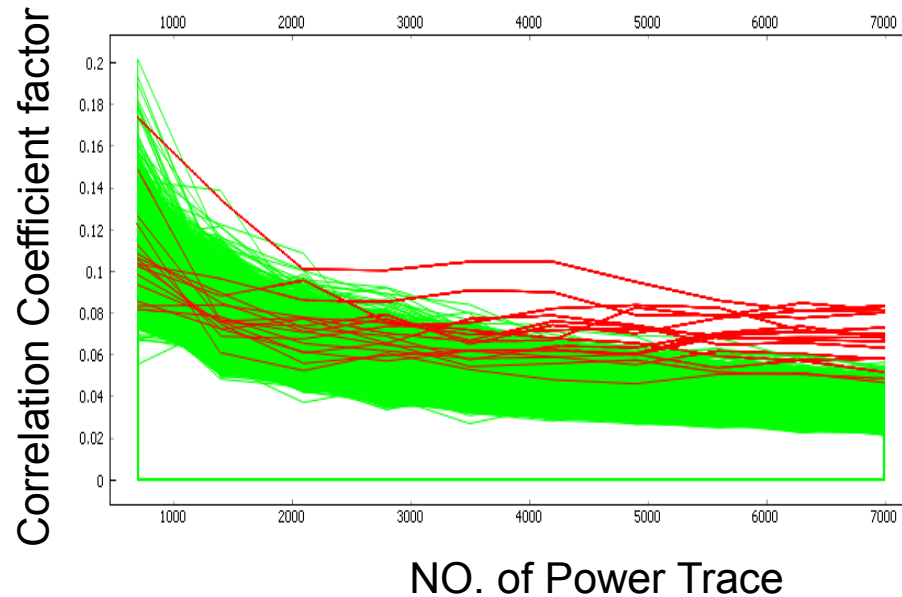


CPA Attack on AES

$$[1] \quad r_{i,j} = \frac{D \sum_{d=1}^D h_{d,i} t_{d,j} - \sum_{d=1}^D h_{d,i} \sum_{d=1}^D t_{d,j}}{\sqrt{\left(\left(\sum_{d=1}^D h_{d,i} \right)^2 - D \left(\sum_{d=1}^D h_{d,i}^2 \right) \right) \left(\left(\sum_{d=1}^D t_{d,j} \right)^2 - D \left(\sum_{d=1}^D t_{d,j}^2 \right) \right)}}$$

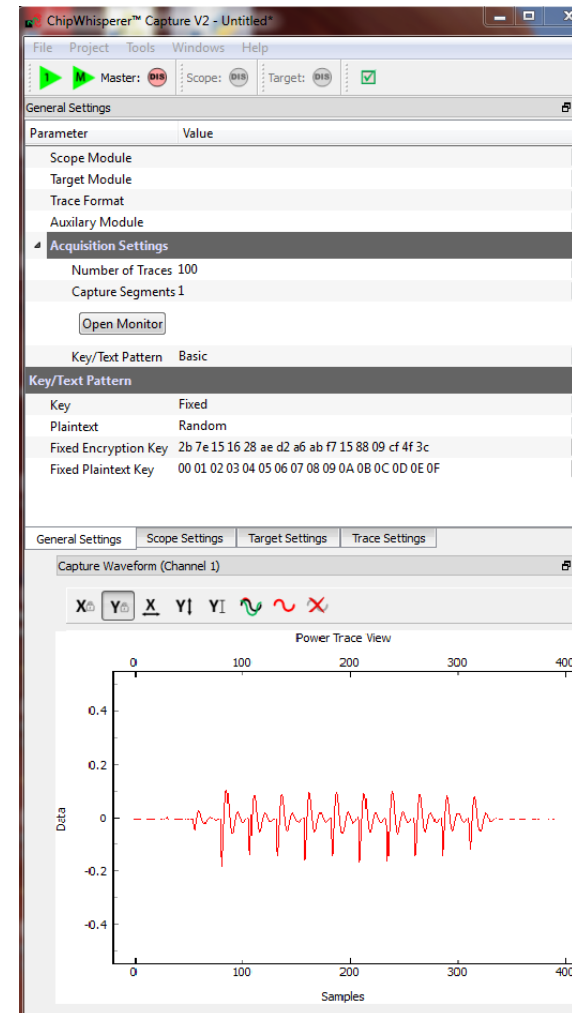
Convert the
ciphertext to
power trace

 $h = aH(D) + b$

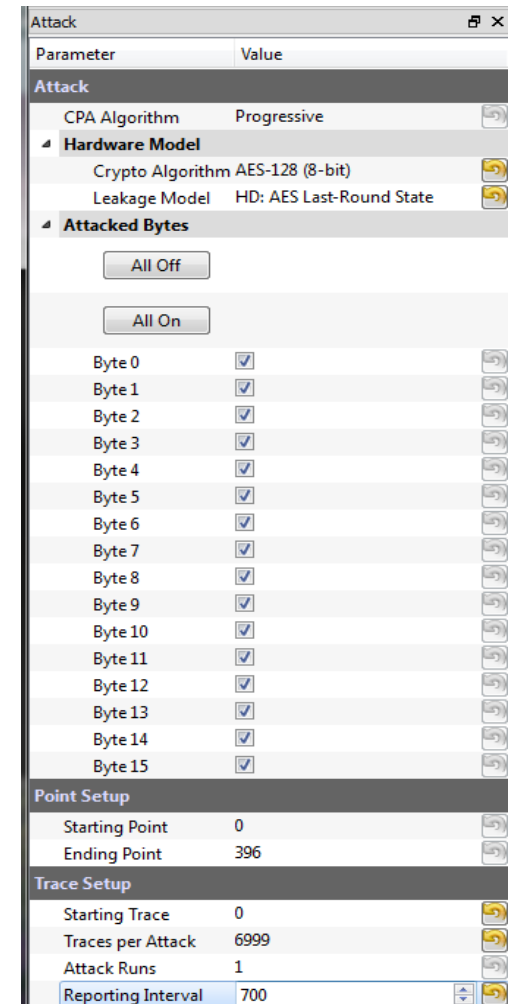


Experimental Setup

Capture



Analyzer



Analyzer

The screenshot displays the ChipWhisperer Analyzer interface. The main window is titled "Results Table" and shows a grid of data. The top row of the grid is highlighted in yellow and contains the following values: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15. Below this row, the first row of data is also highlighted in yellow and contains the following values: PGE, 0, 39, 0, 0, 54, 0, 0, 0, 0, 8, 12, 0, 0, 0, 16, 0. The second row of data contains the following values: 0, E6, 5B, D4, C4, ED, AD, 82, 9D, C0, 32, 51, ED, 36, 6D, 96, 3B. Below these values are correlation coefficient factors: 0.0634, 0.0472, 0.0596, 0.0937, 0.0494, 0.0661, 0.0675, 0.0531, 0.0579, 0.0542, 0.0515, 0.0663, 0.0626, 0.0823, 0.0544, 0.0541.

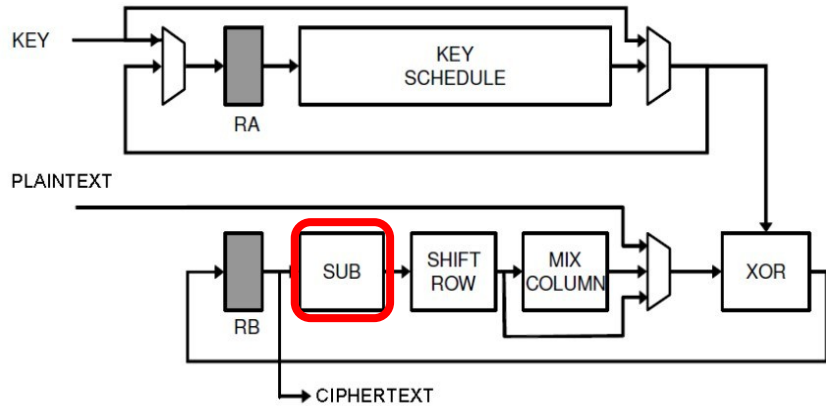
On the left side of the interface, there are several configuration panels. The "Attack" panel shows the CPA Algorithm set to "Progressive" and the Hardware Model set to "AES-128 (8-bit)". The "Attacked Bytes" panel shows "All Off" selected. The "Point Setup" panel shows the Starting Point set to 0 and the Ending Point set to 396. The "Trace Setup" panel shows the Starting Trace set to 0 and the Traces per Attack set to 6999. The "Reporting Interval" is set to 700. The "Progressive CPA" panel shows the Iteration Mode set to "Breadth-First" and the "Skip when PGE=0" checkbox unchecked.

Subkey NO.

Subkey Guess

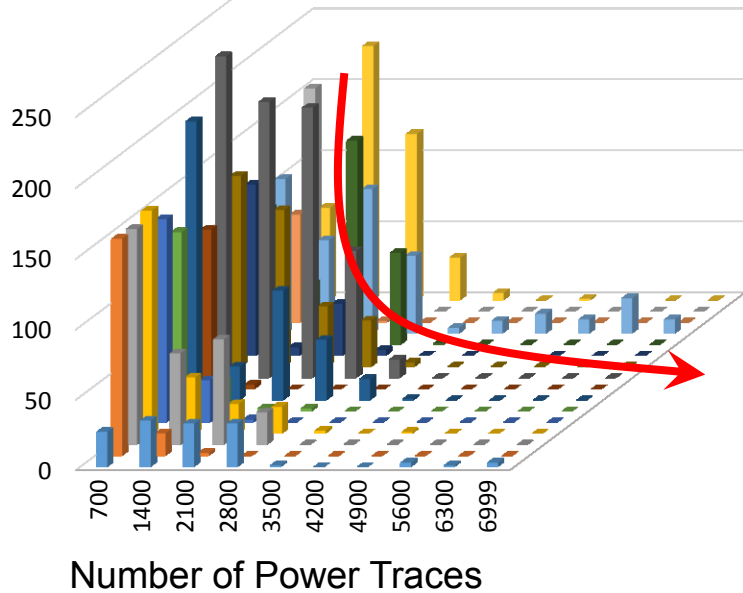
Correlation coefficient factor

Impact of FD on SCA Attack

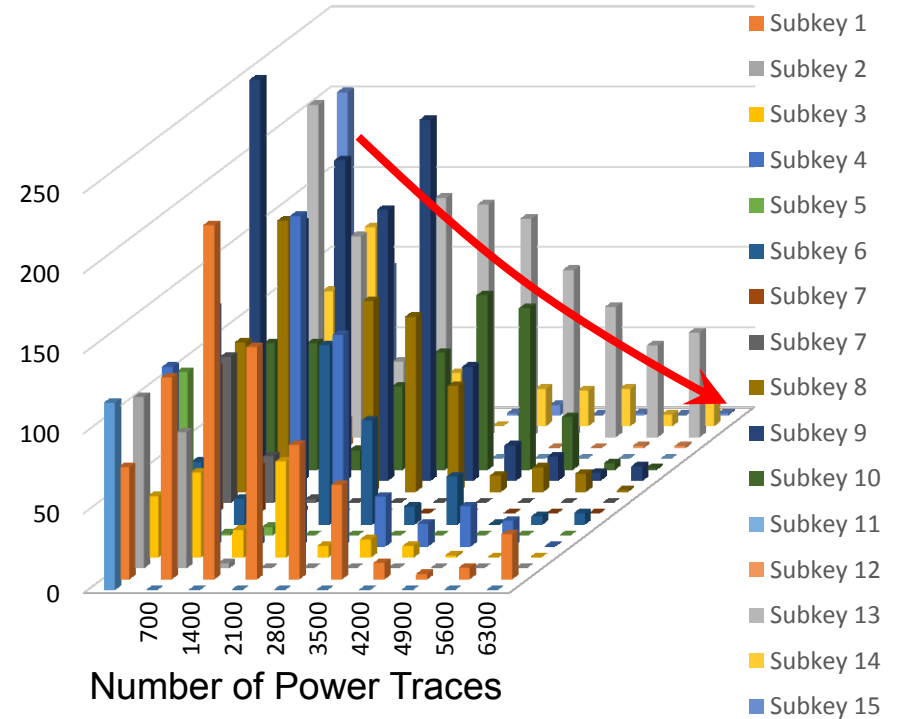


FD: Parity check code

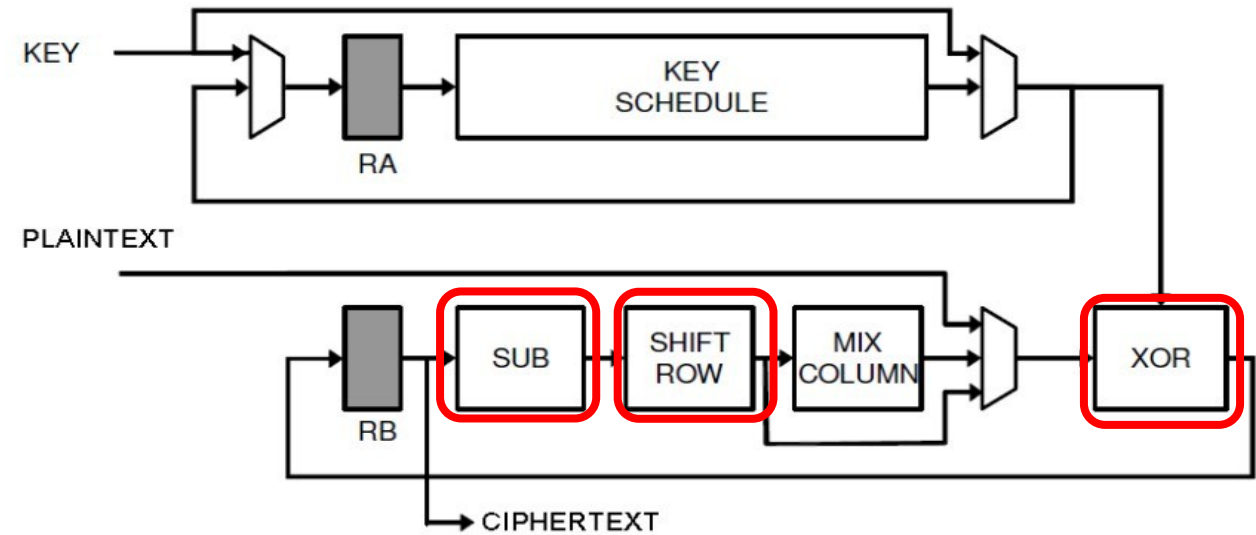
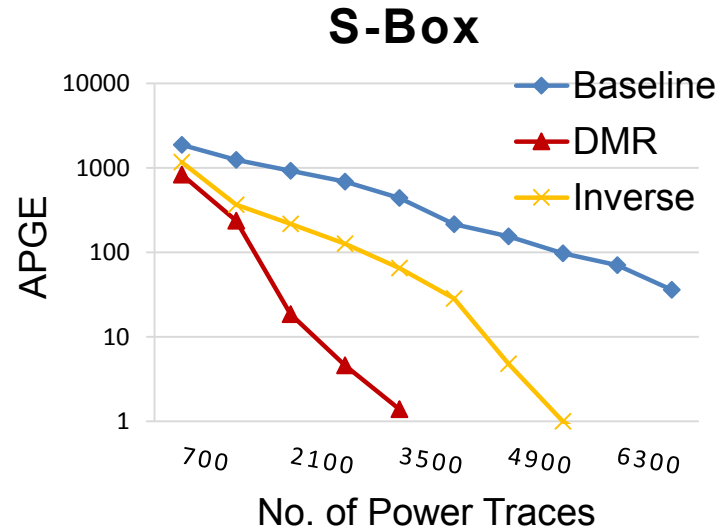
Partial Guessing Entropy



Partial Guessing Entropy



Impact of Different Hardware Redundancy-Based FD Methods on SCA Attack



Existence of hardware redundancy-based FD increase the efficiency of CPA

Use information redundancy-based FD

Impact of Different Power Models in CPA Attack

0 0 0 0 0 0 0 0

Ref. ciphertext

1 1 0 0 0 0 1 0

Real ciphertext

1 1 0 0 0 0 1 0

HW: 3

0 1 1 0 0 1 1 1

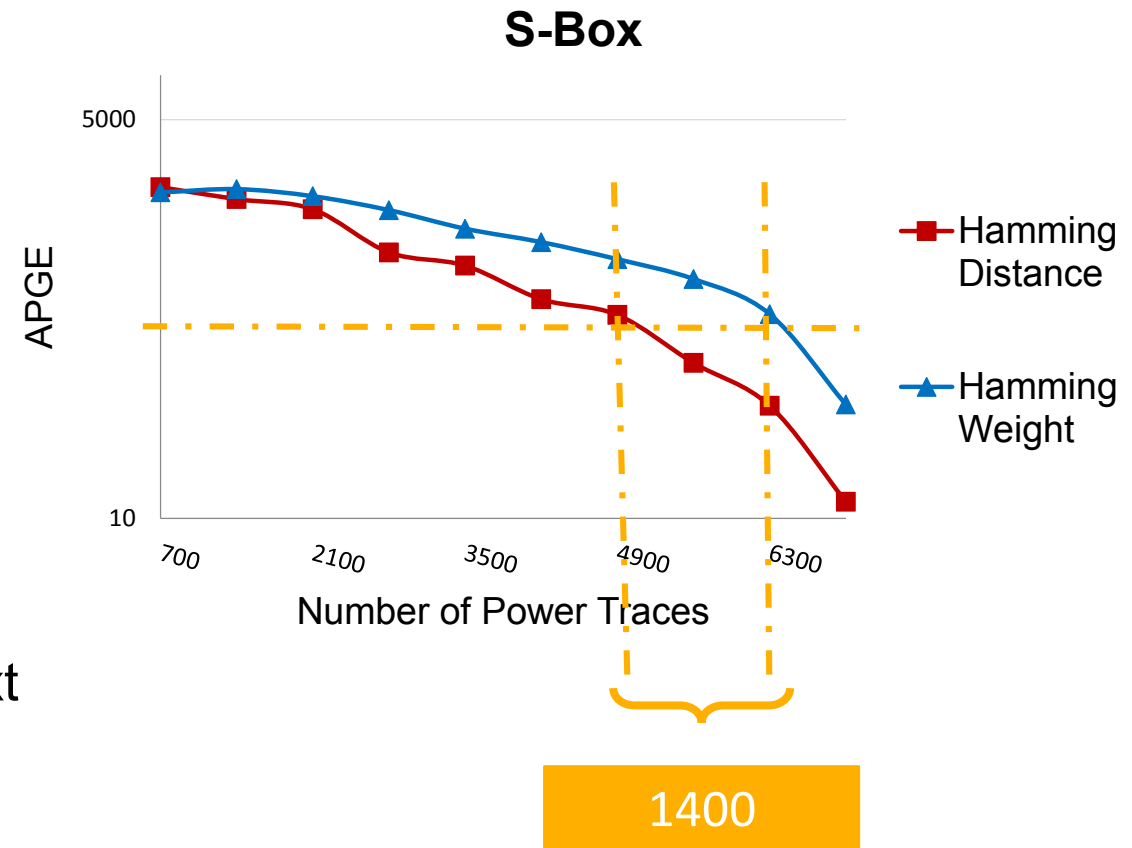
Previous ciphertext

1 1 0 1 1 0 1 0

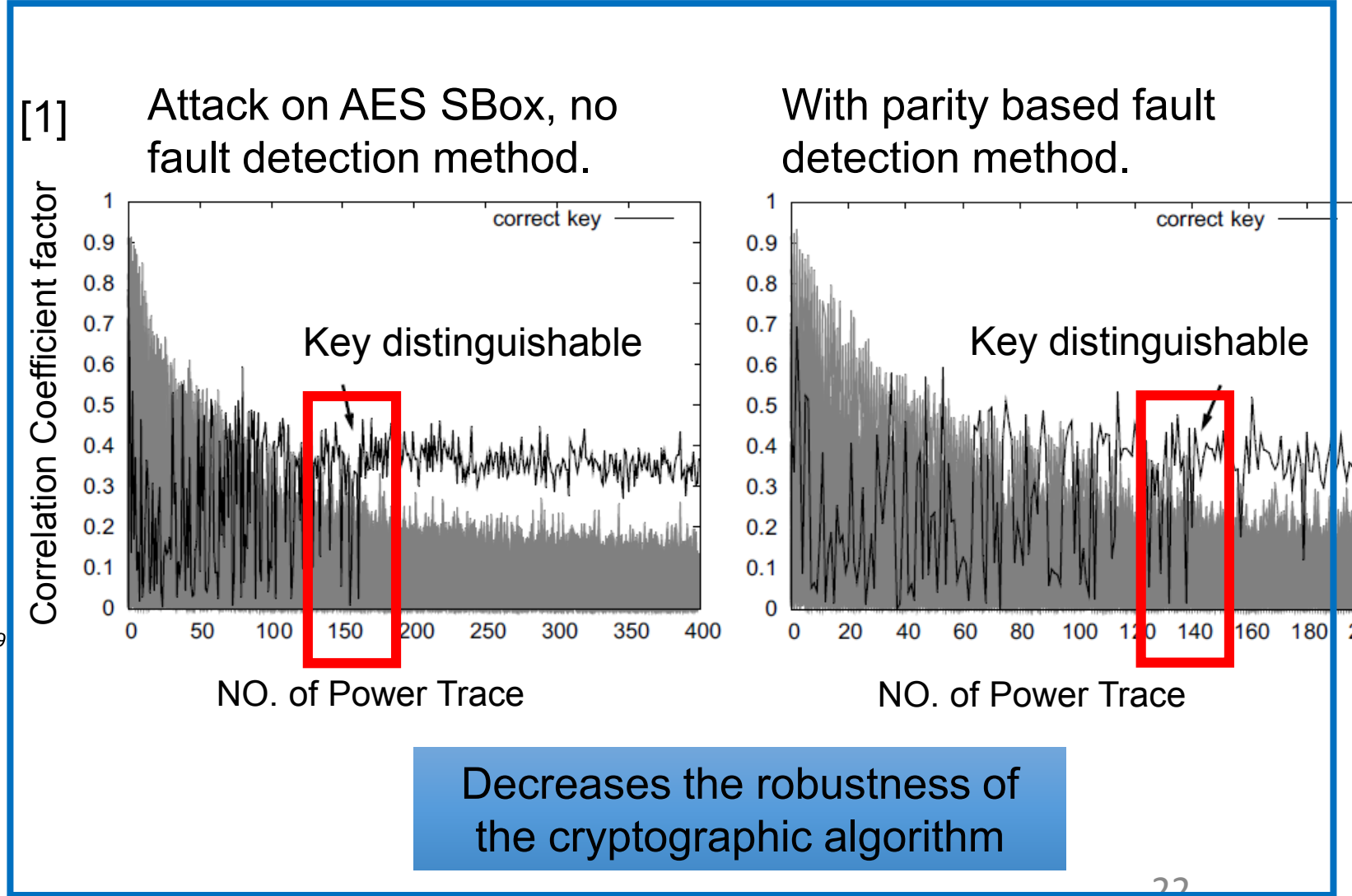
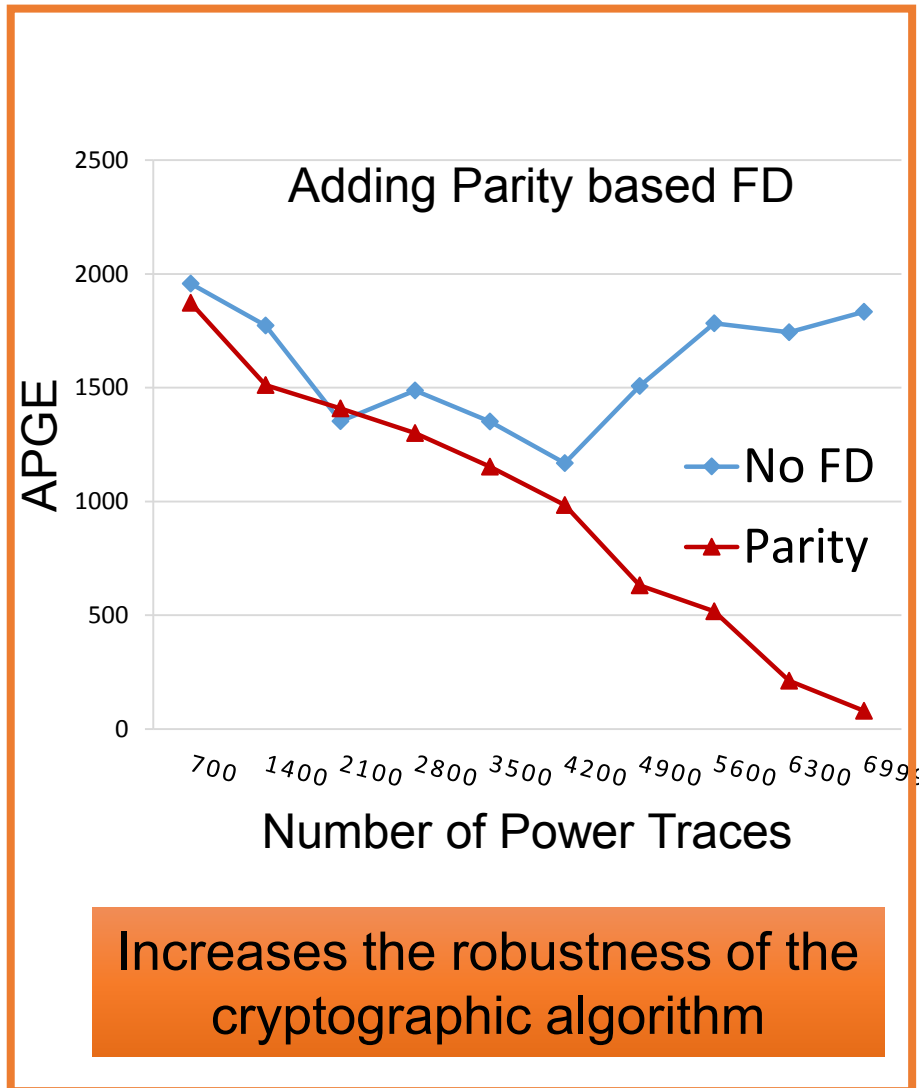
Real ciphertext

1 0 1 1 1 1 0 1

HD: 6

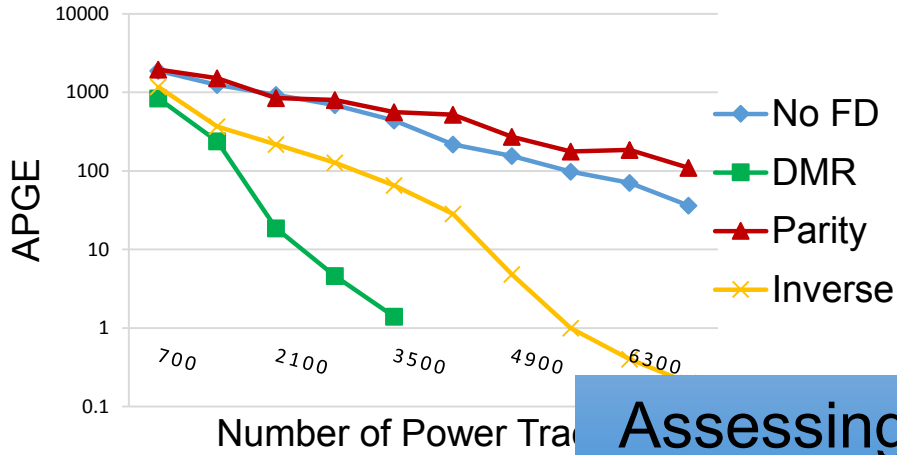


Impact of Different Power Models in CPA Attack

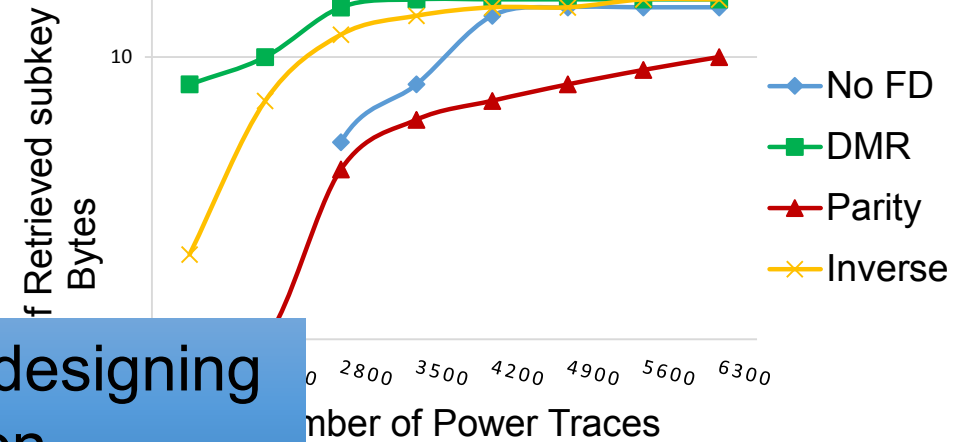


Two Approaches to Study the Impact of Different FDs

APGE for Different FDs on SBox

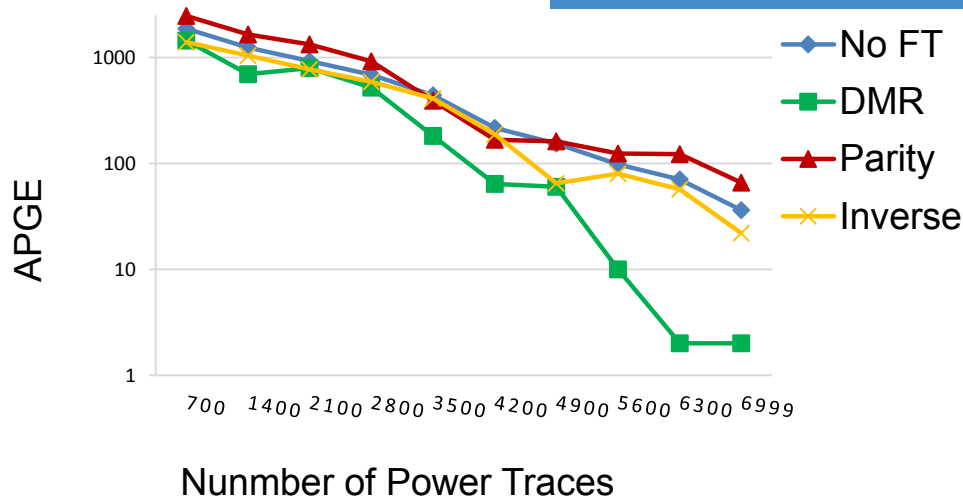


NO. of Retrieved Subkey Bytes for Different FDs on SBox

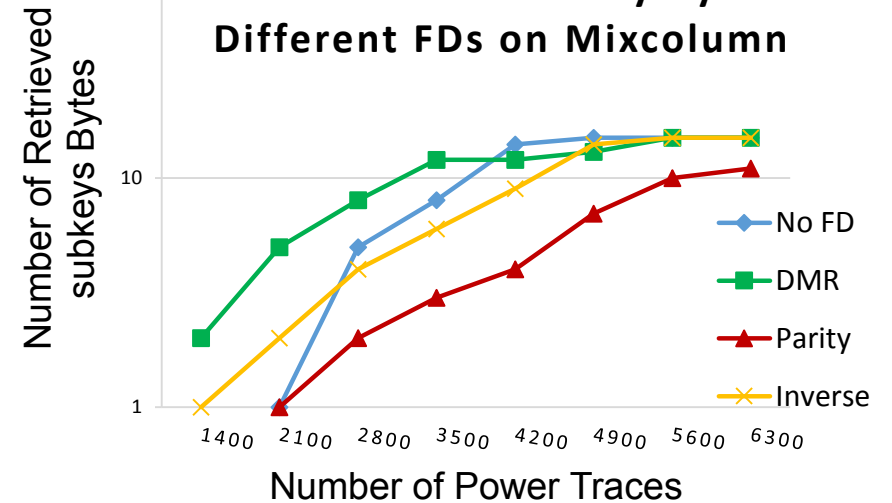


Assessing the process of designing a suitable protection

APGE For Different



NO. of Retrieved Subkey Bytes for Different FDs on Mixcolumn



Conclusion

- As the combination of FA and SCA attacks is emerging as an advanced attack, effective countermeasure for the combined attack is needed.
- One countermeasure for a particular attack can influence the other attack positively or negatively.
- Our experimental results indicate that the effective factors on CPA efficiency include
 - Type of redundancy
 - Module under protection
 - CPA attack power model

Thank you!

Any Questions?