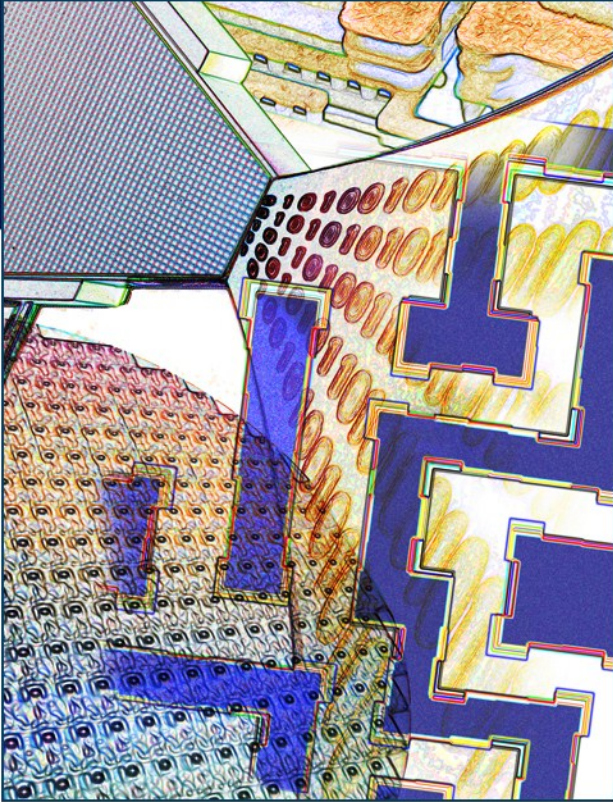


Advanced multi-patterning and hybrid lithography techniques

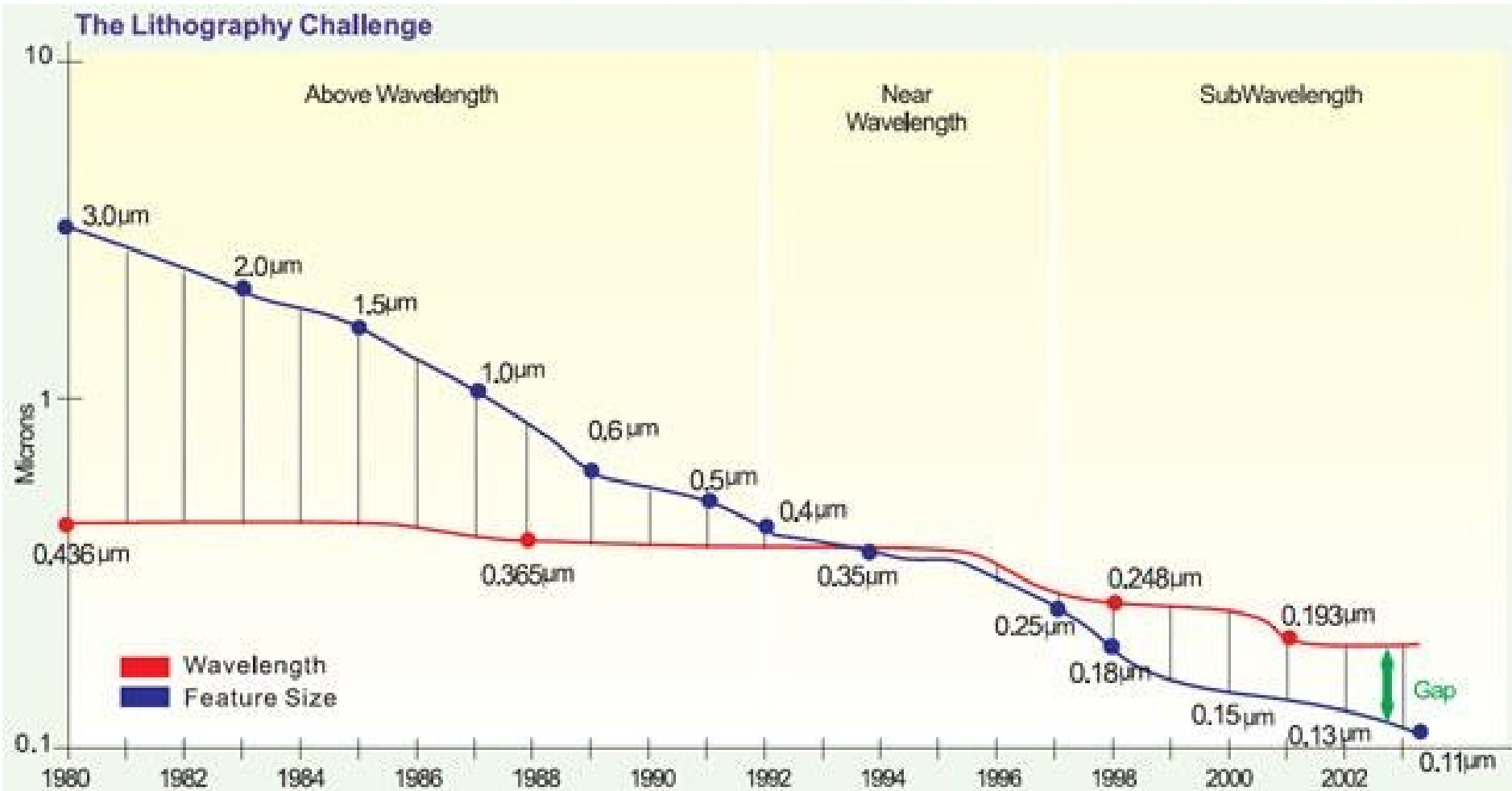
Fedor G Pikus, J. Andres Torres



Outline

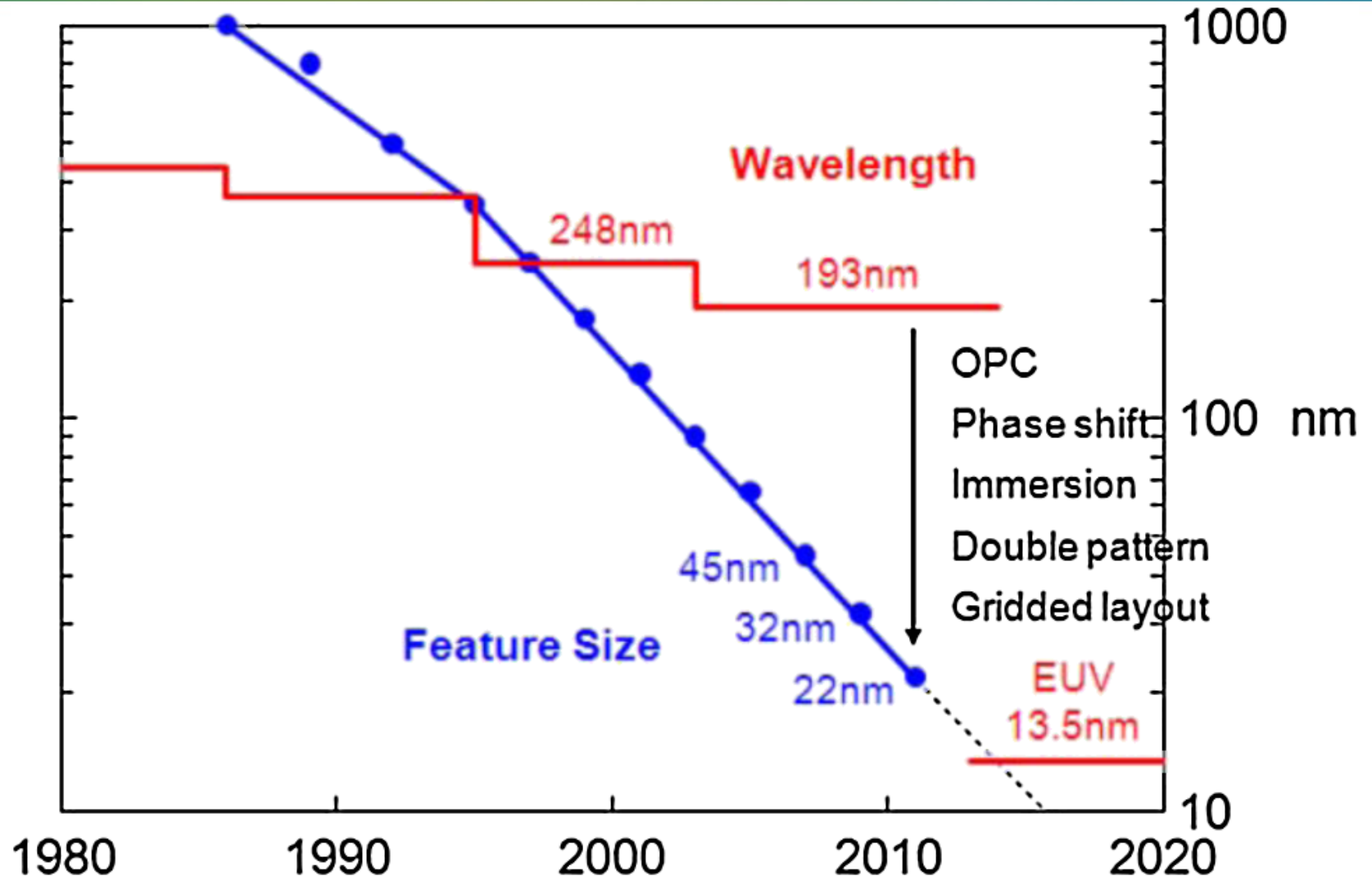
- Need for advanced patterning technologies
- Multipatterning (MP) technologies
 - What is multipatterning?
 - How does it work?
 - What problems does it create?
 - How does it change the way designers work?
 - Maturing technology – mostly engineering challenges
- Direct self-assembly (DSA)
 - What is direct self-assembly?
 - How does it work?
 - How does it interact with multipatterning?
 - What are the challenges?
 - New technology – many unknowns

The Lithography Challenge



Source – ITRS roadmap, 2005

The REAL Lithography Challenge



Source – Bohr M., "Moore's law in the innovation era," Proc. SPIE . 7974, , 797402 (2011). 0277-786XI

How Progress is Made

	N28		N20		N14		N10		N7	
Fin / Active	I93i SP		I93i SP		SADP + cut	48	SADP + cut	36-42	SAQP + LELE cut	24-27
Gate	I93i SP	I10	LELE + cut	82-90	LELE + cut	82-90	LELE + cut	64	LELE + cut	48
M0A	n/a		LELE		LELE	82-90	LELELE	64	LELELE	48
M0G	n/a		LELE		LELE	82-90	LELE	64	LELE	48
V0	I93i SP		I93i SP		LELE	90 (SV)	LELE	72(SV)	LELELE	60 (SV)
MI	I93i SP	90	LELE	64	LELE	64	LELELE	48	SADP + LELE block	48
Vx	I93i SP		I93i SP		LELE	90	LELE	68	LELELE	51
Mx	I93i SP	90	LELE	64	LELE	64	SADP + block	48	SAQP + LELE block	36

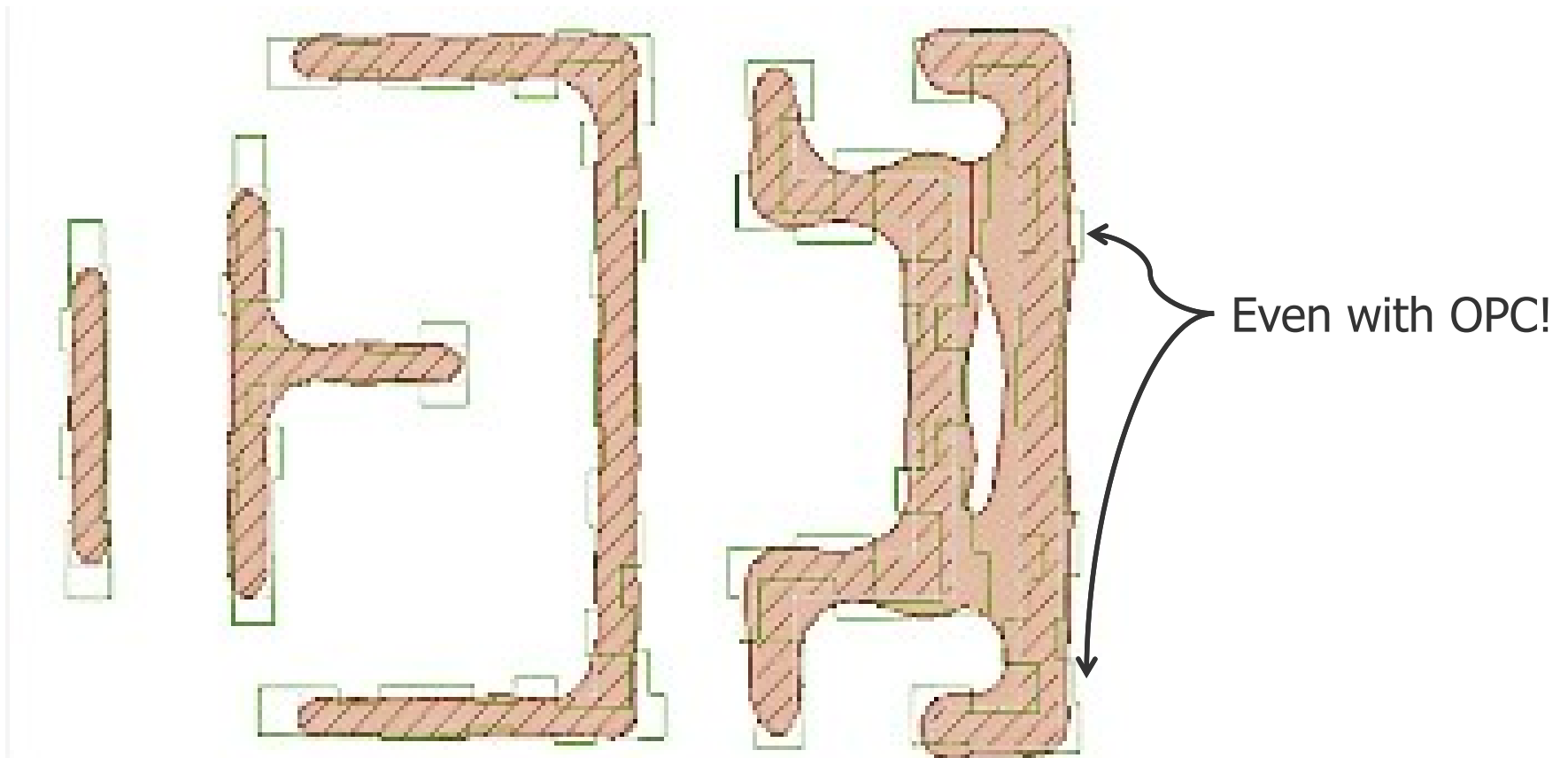
Source – Arindam Mallik et al, “The economic impact of EUV lithography on critical process modules,” Proc. of SPIE 9048, 2014

Outline – MultiPatterning (MP)

- Why do we need multipatterning?
- What is multipatterning?
- Different multipatterning technologies
 - Multiple exposures
 - Self-aligned patterning
 - Multi-patterning and fill
 - Stitches
- Multipatterning impacts cost, yield, and performance
- Multipatterning flows and tools
 - Colorless flow
 - Colored flow

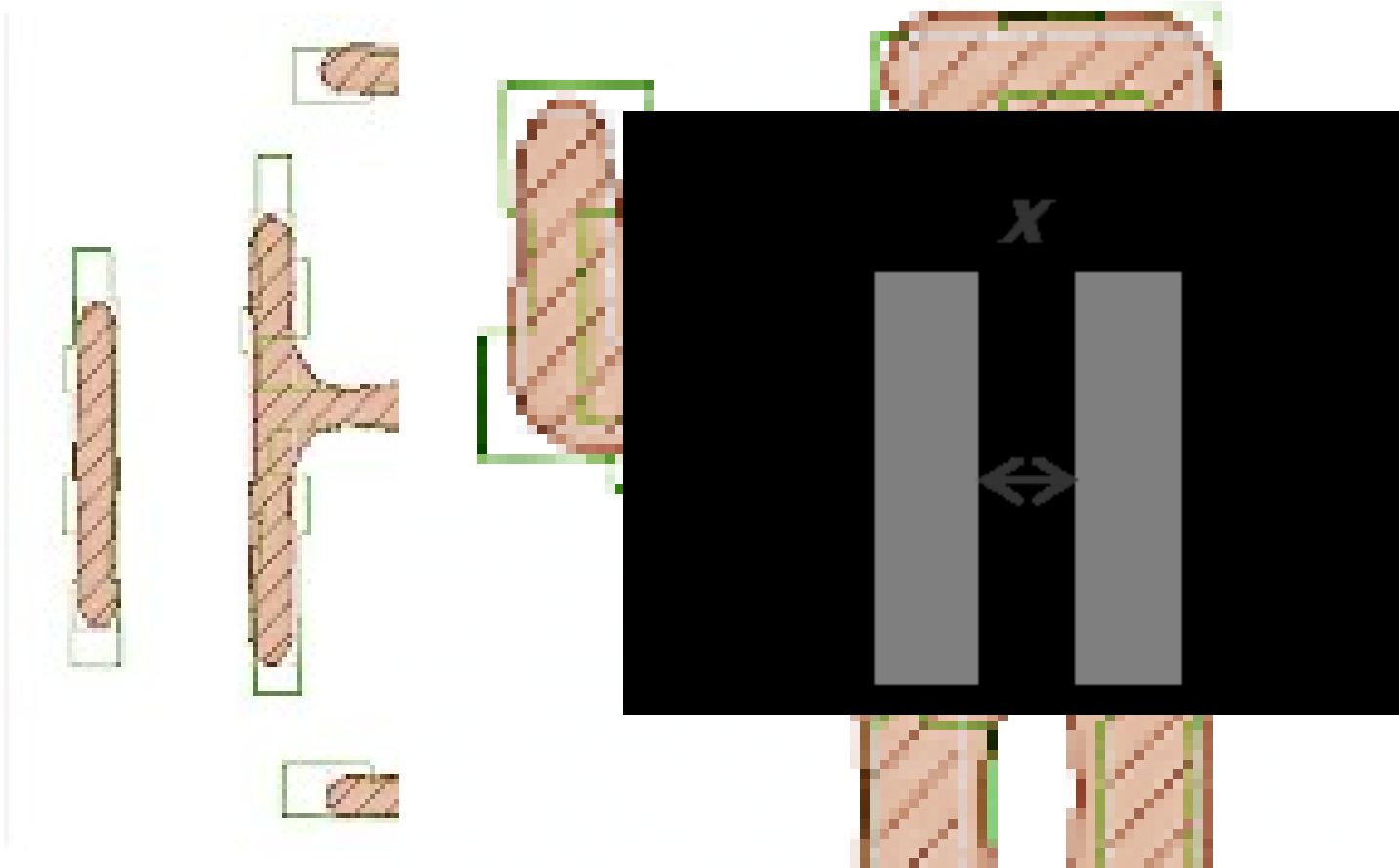
MultiPatterning in a Nutshell

- Layout is too dense to print



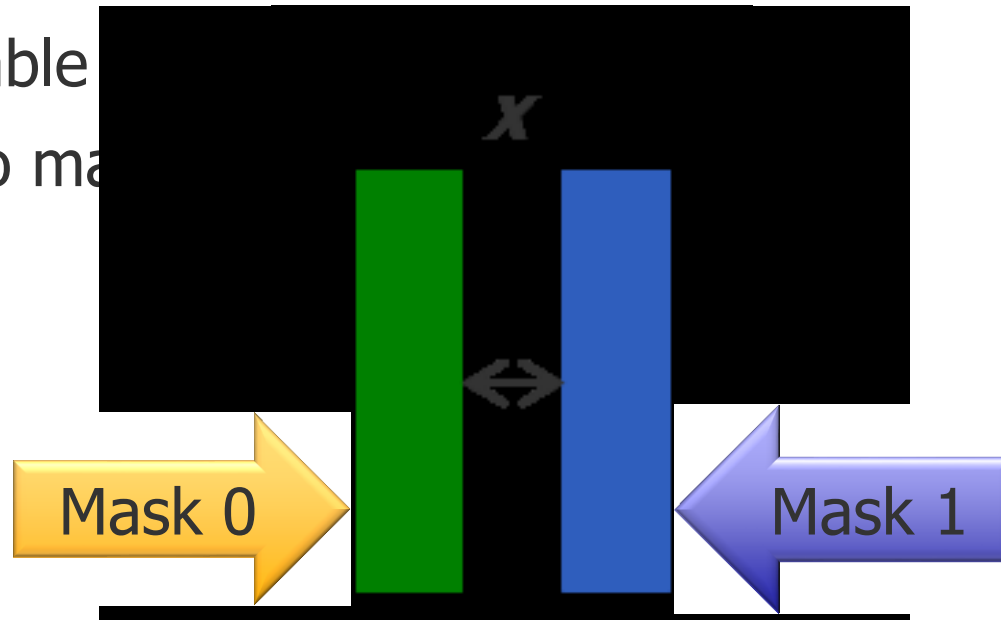
MultiPatterning in a Nutshell

- Layout is too dense to print
- DRC violations are detected



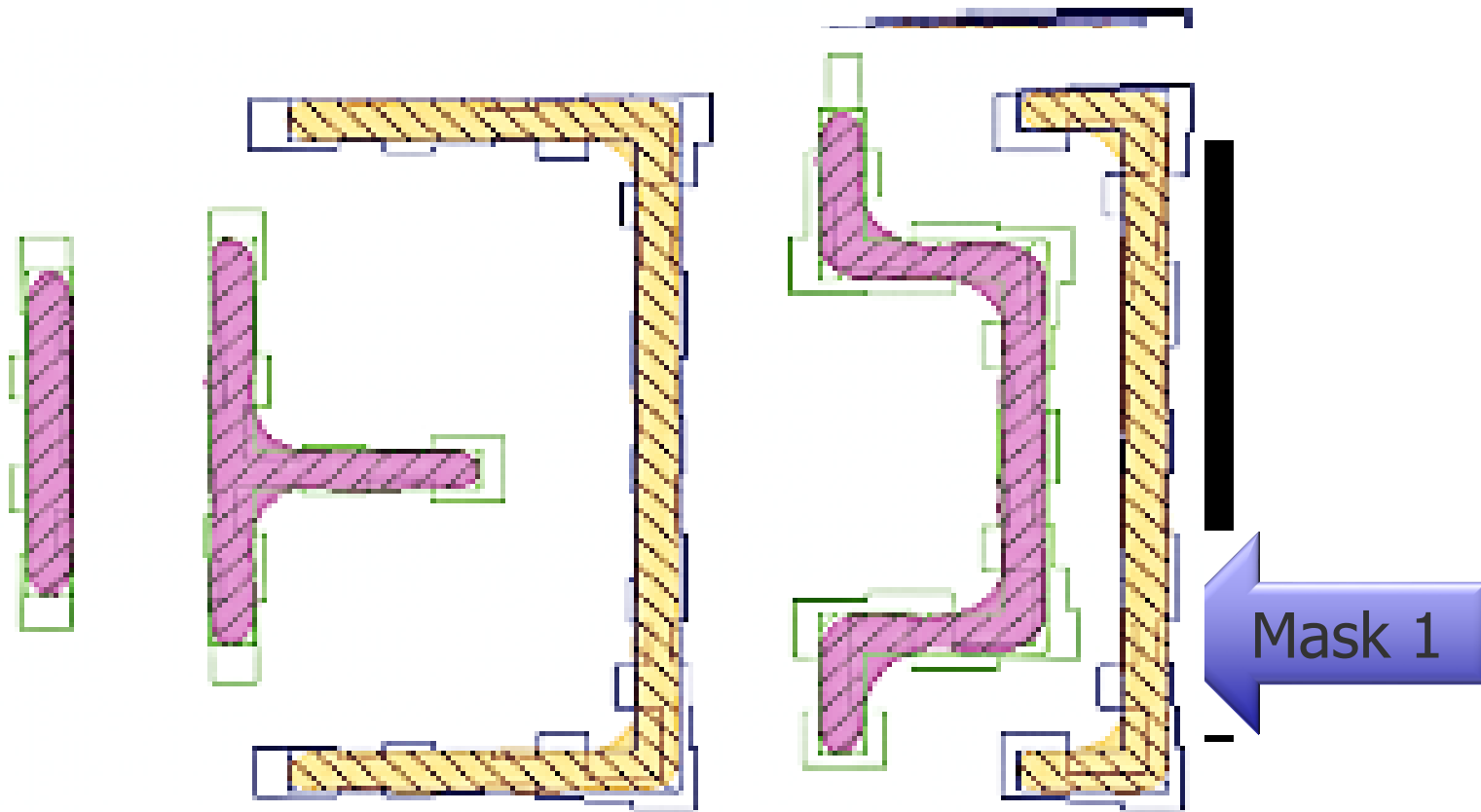
MultiPatterning in a Nutshell

- Layout is too dense to print
- DRC violations are detected
- We cannot print all features using one mask
- But we may be able
- We will need two masks

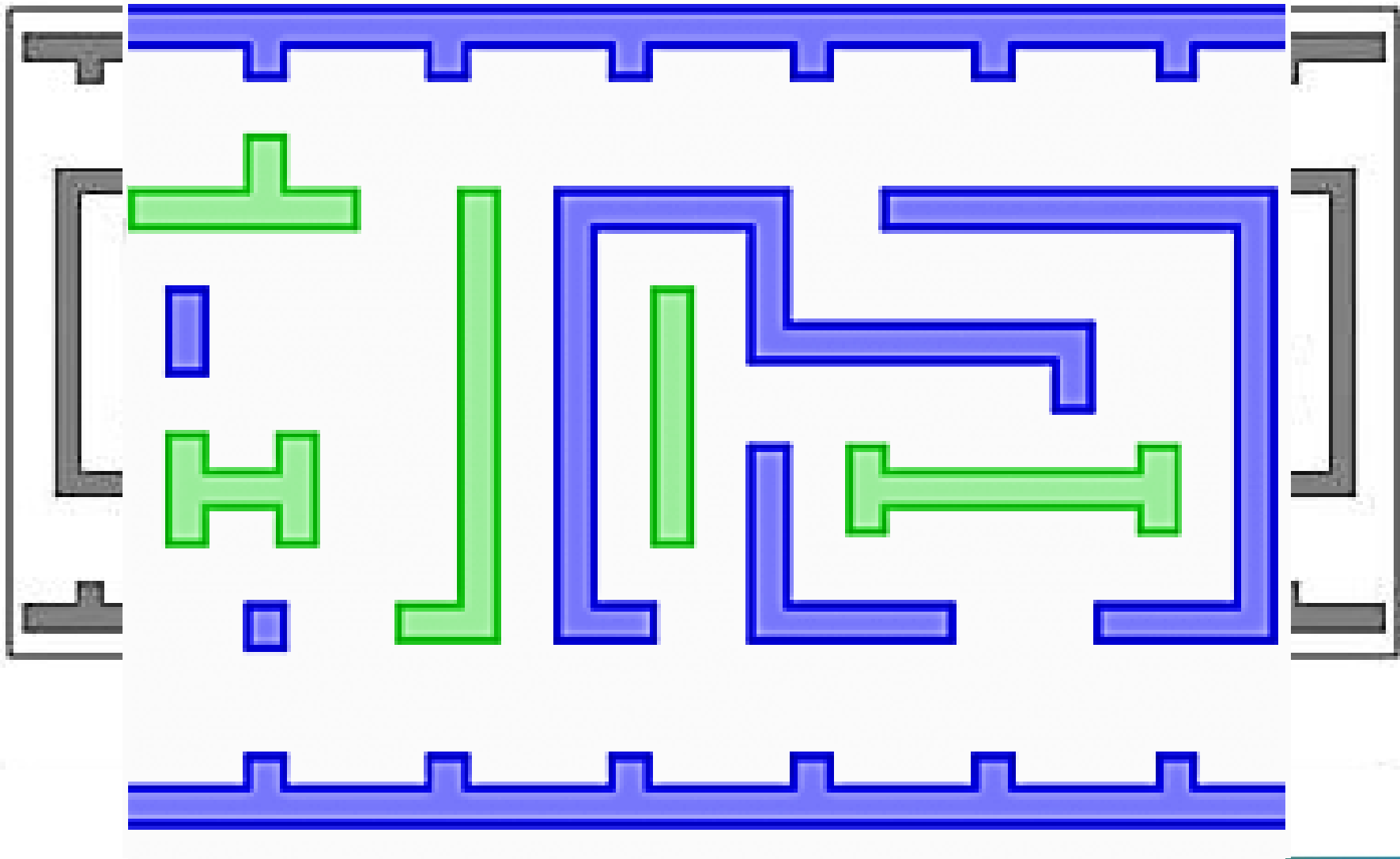


MultiPatterning in a Nutshell

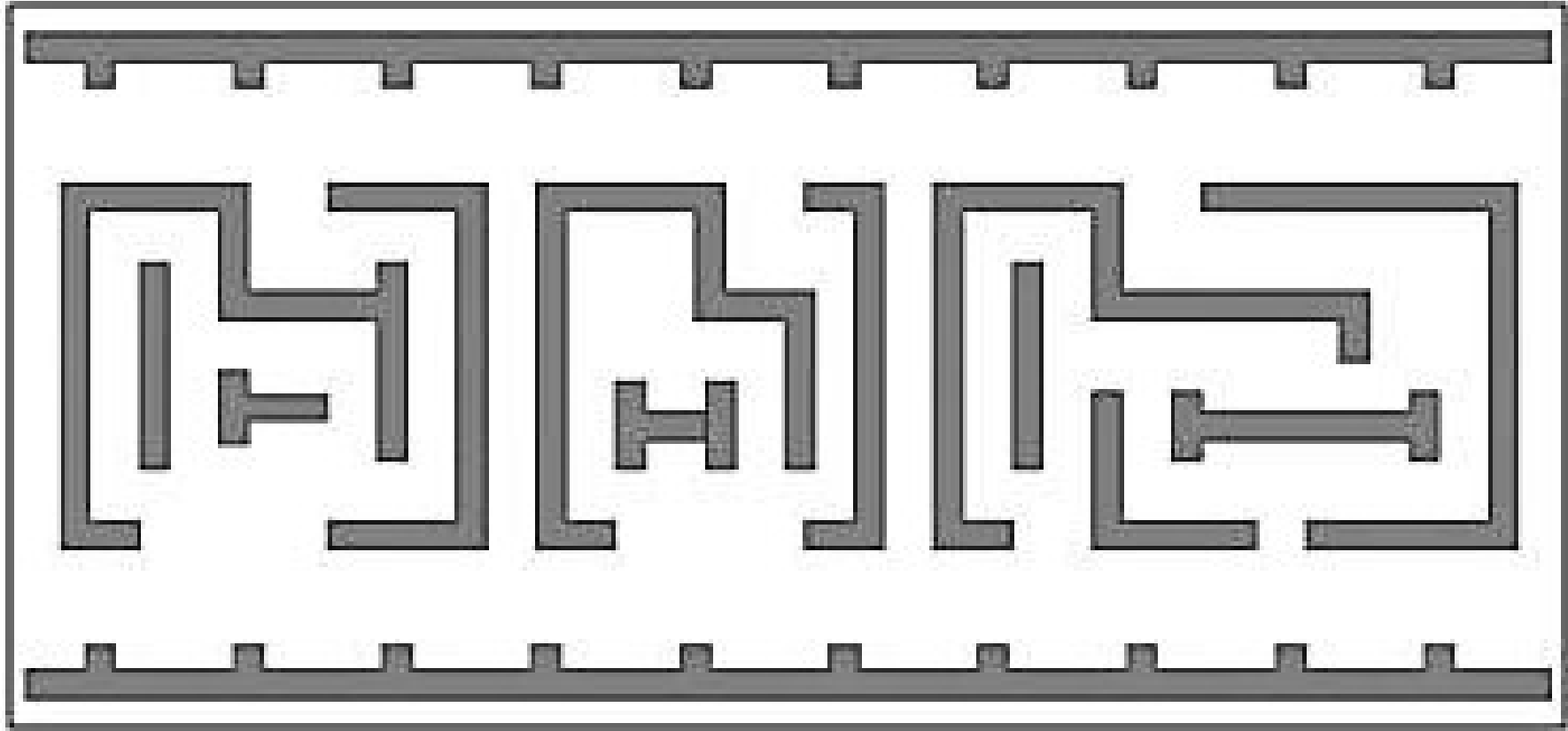
- We will need two masks



Multiple Patterning by Multiple Exposures

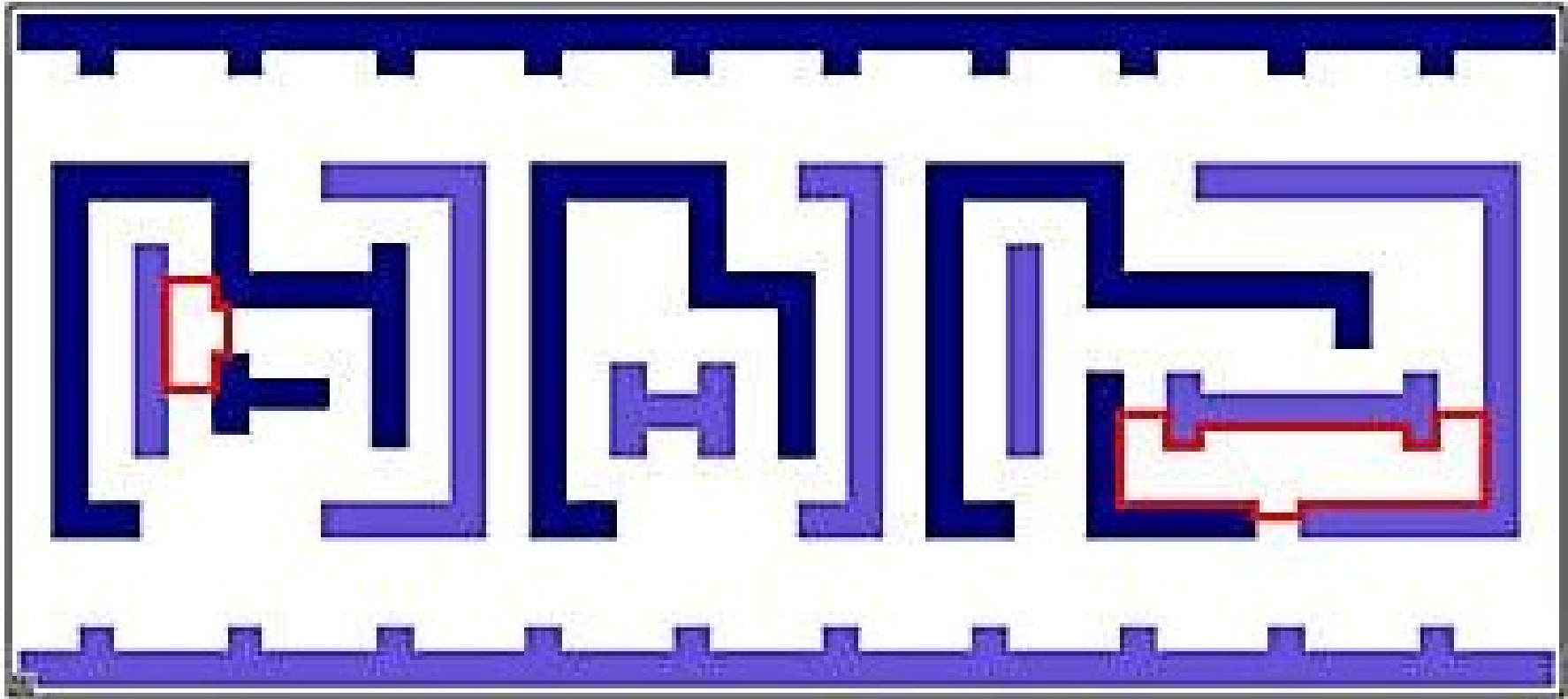


Multiple Patterning by Multiple Exposures



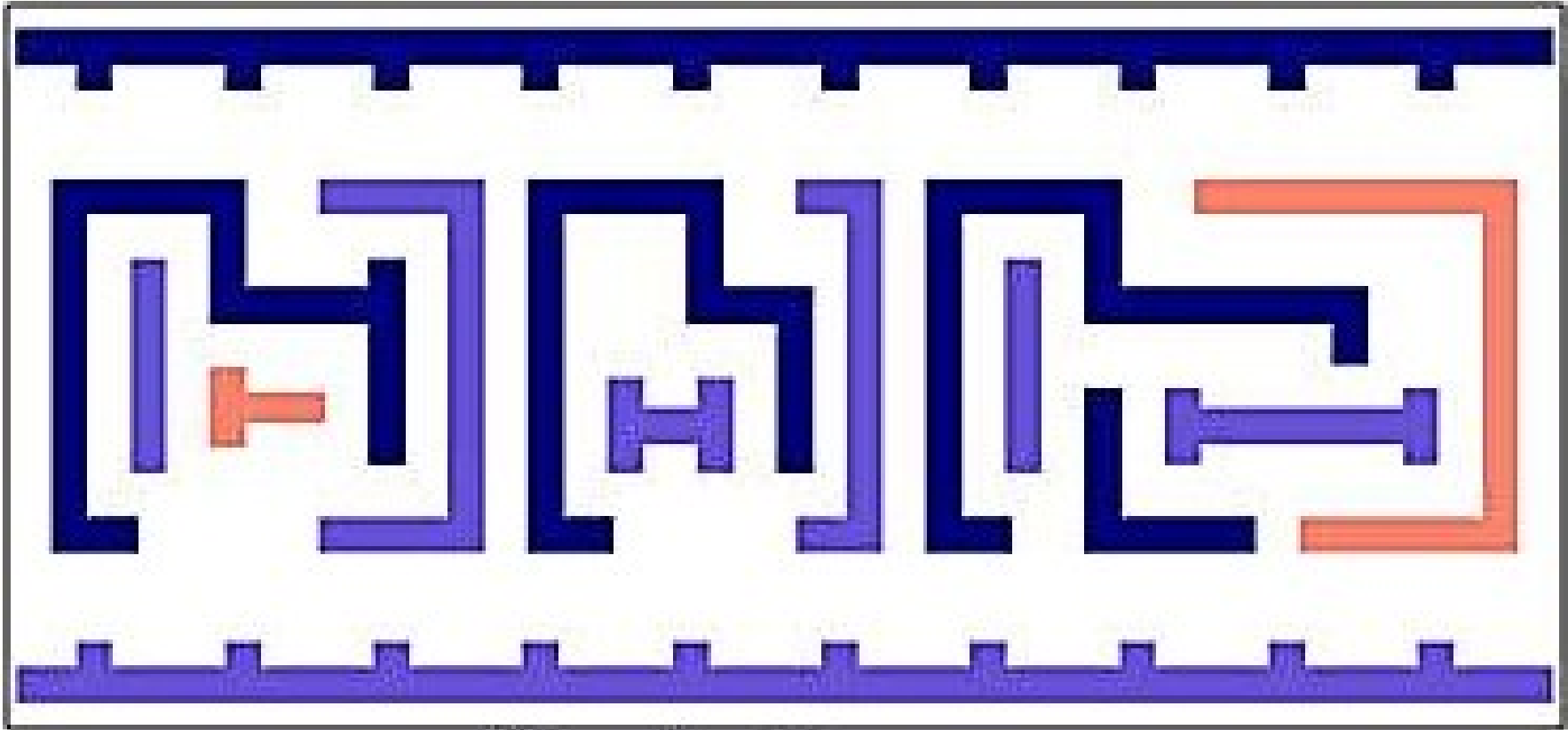
- Exposures are processed sequentially:
 - Litho-etch-litho-etch (**LELE**, double patterning)

Multiple Patterning by Multiple Exposures



- Exposures are processed sequentially: LELE
- What if the layout is too dense even for two masks?

Multiple Patterning by Multiple Exposures

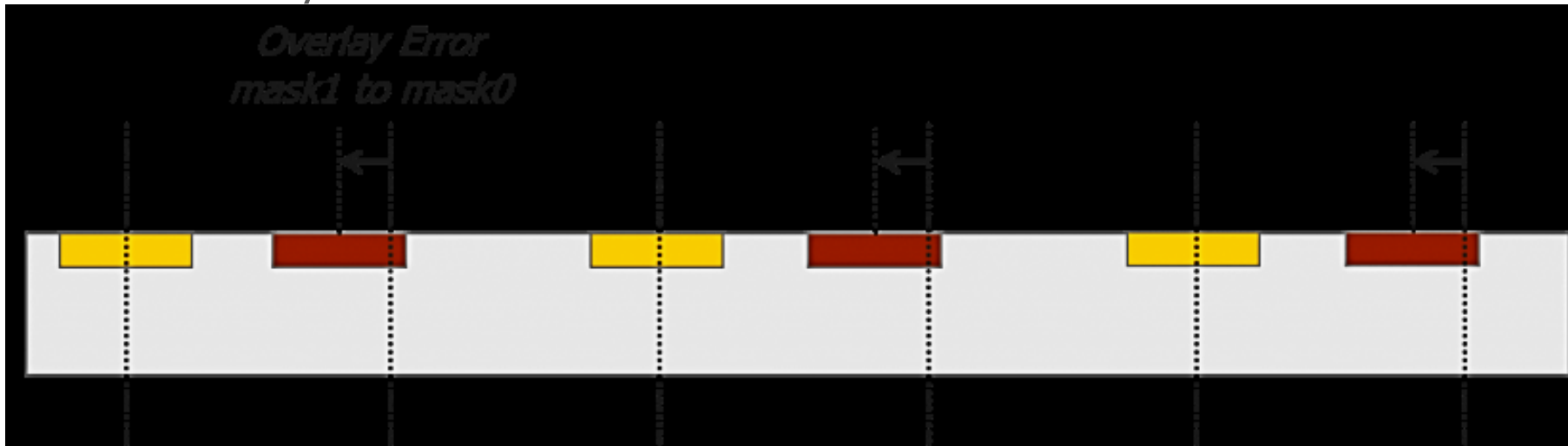


- Exposures are processed sequentially: LELE
- What if the layout is too dense even for two masks?
 - LELELE (triple patterning)

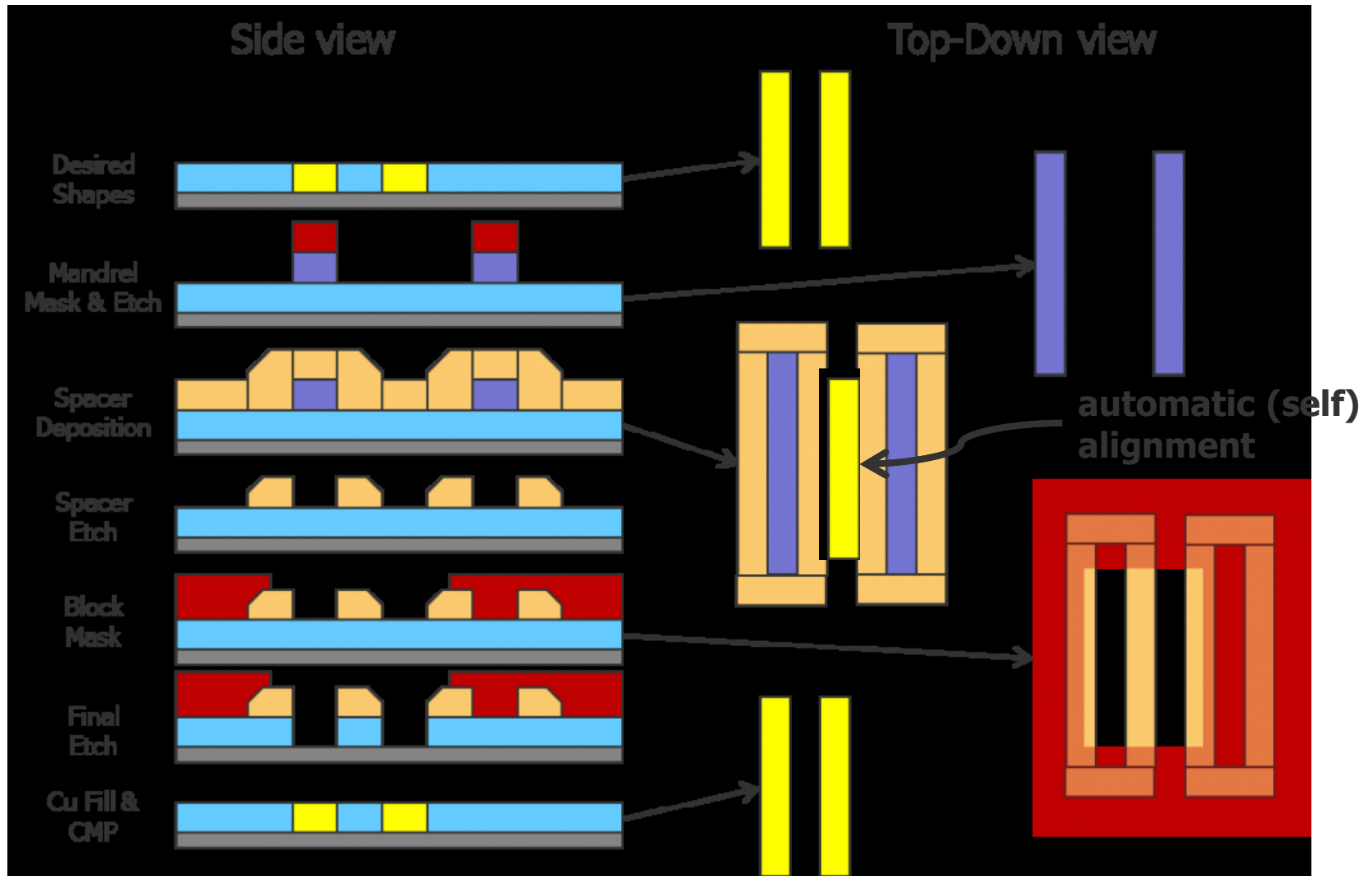
Why not LELELELELELE?

(3nm, here we come!)

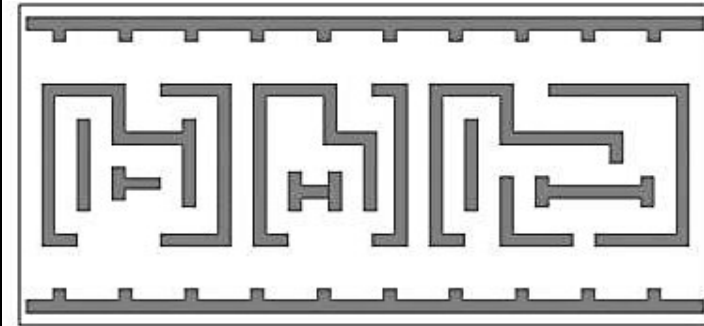
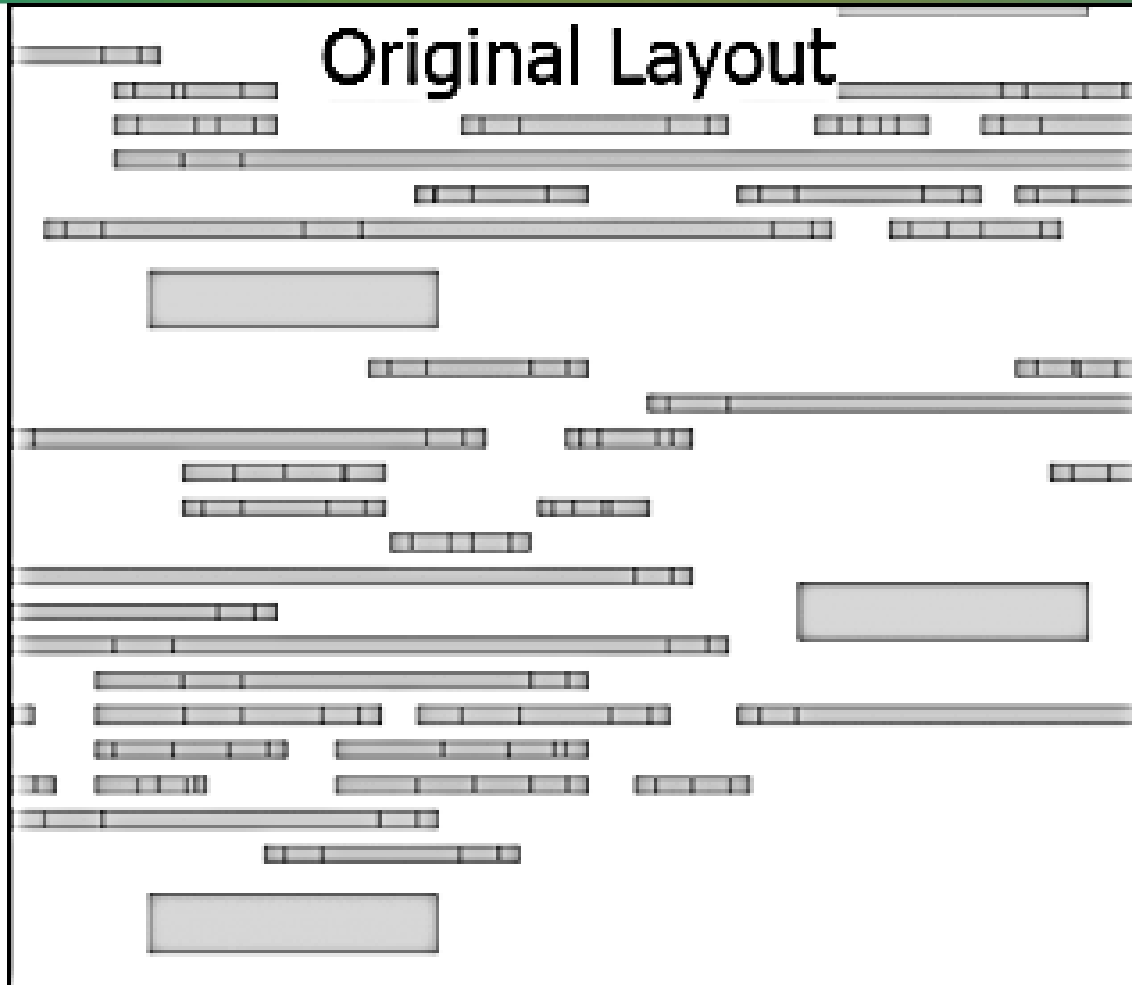
- Each exposure requires a new mask
 - Masks are expensive
- What happens to the first exposure (LE) when it's etched again (LELE)?
 - Different masks usually require different bias
- Combining separate masks is never perfect
 - Overlay error



Self-Aligned Double Patterning (SADP)

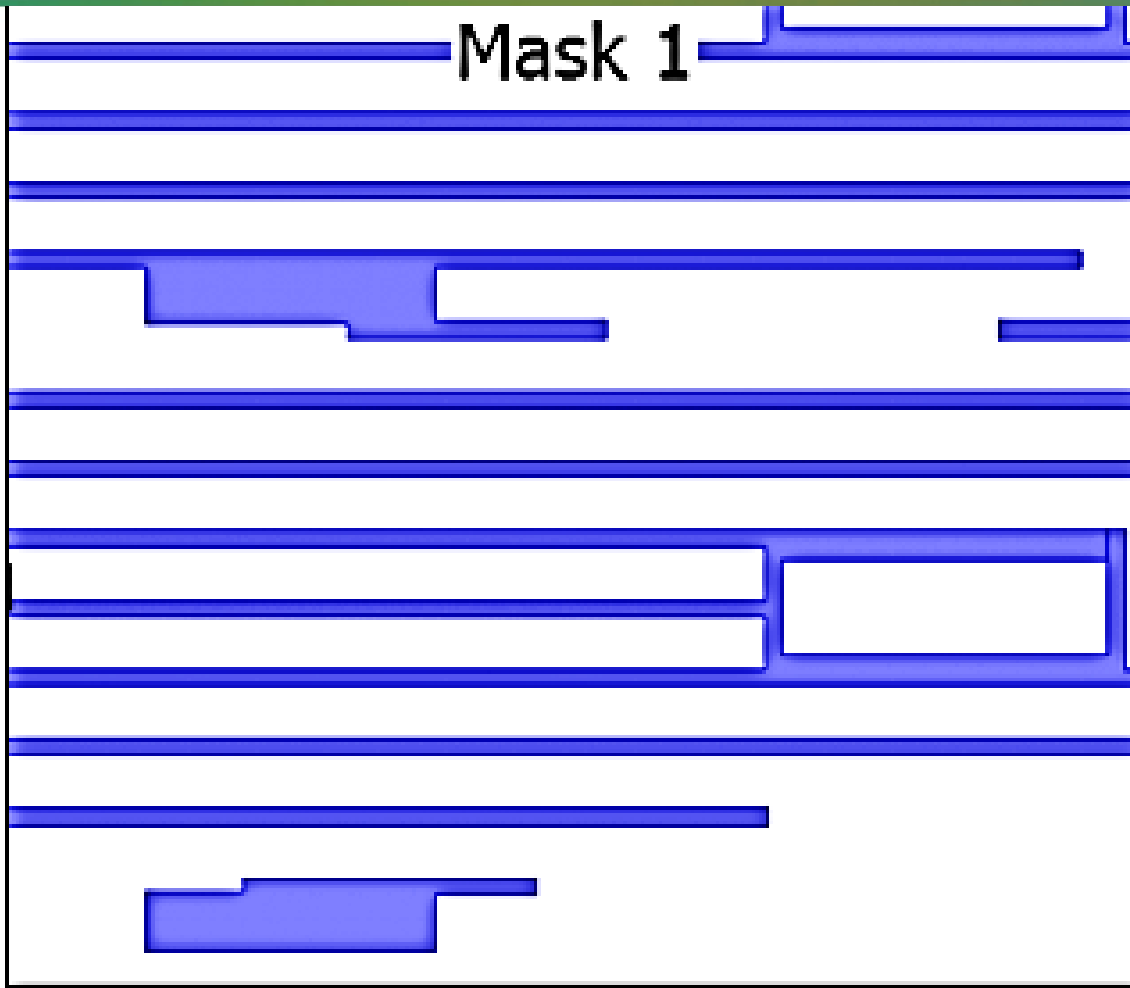


Self-Aligned Double Patterning



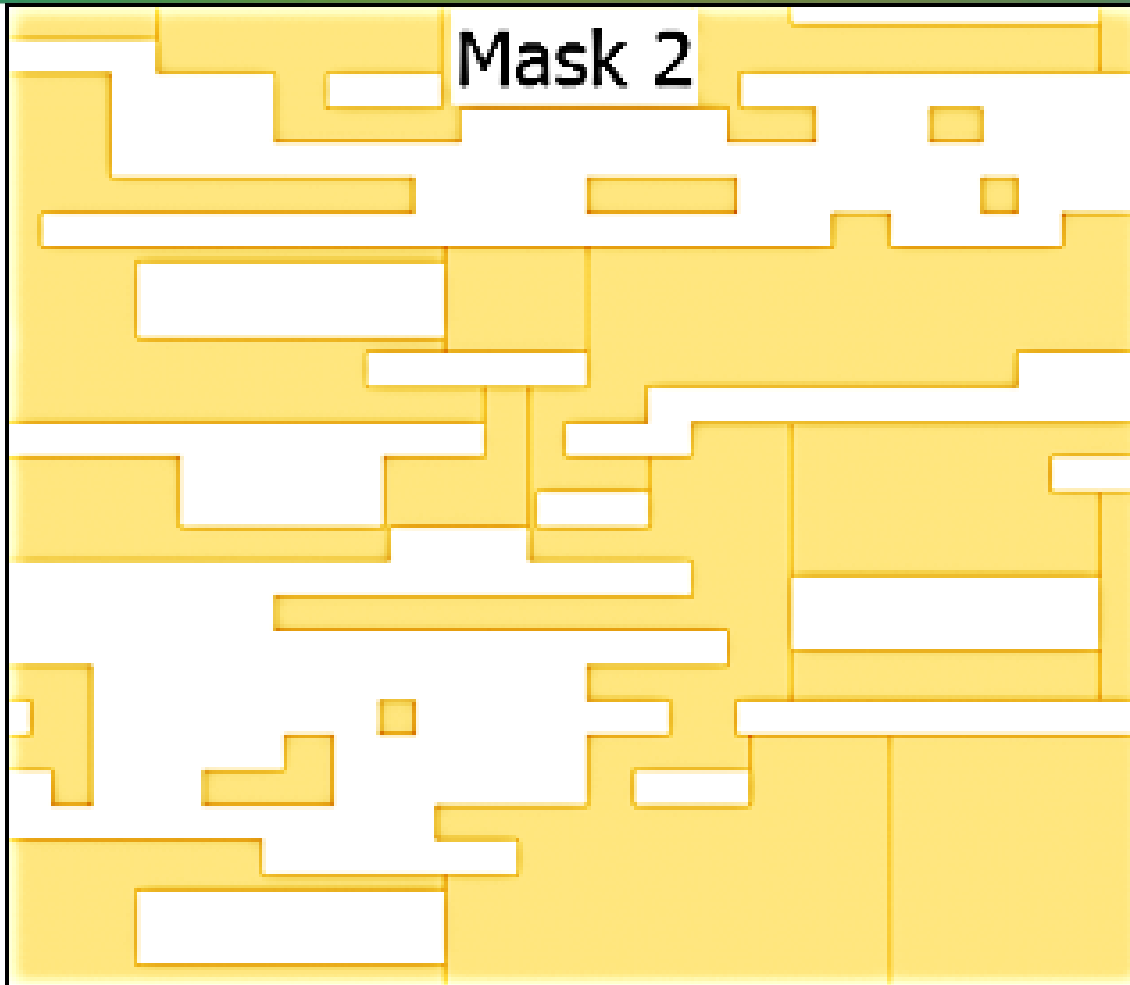
- Different layout style – nearly one-dimensional

Self-Aligned Double Patterning



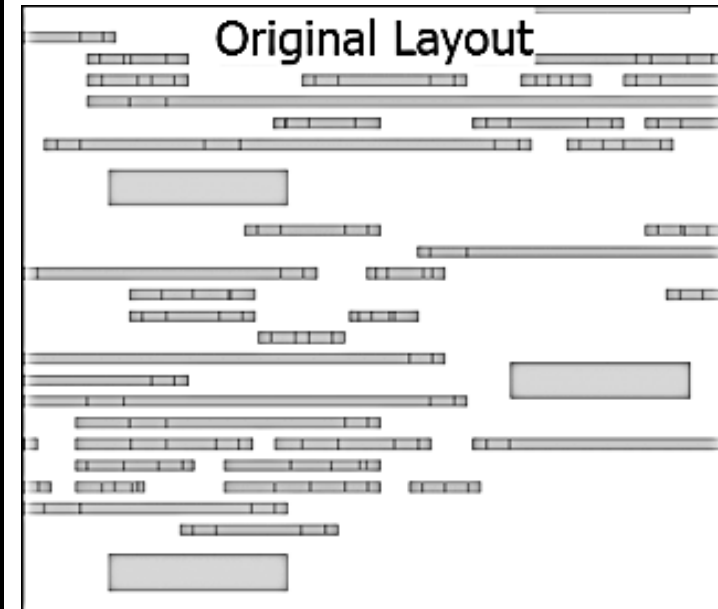
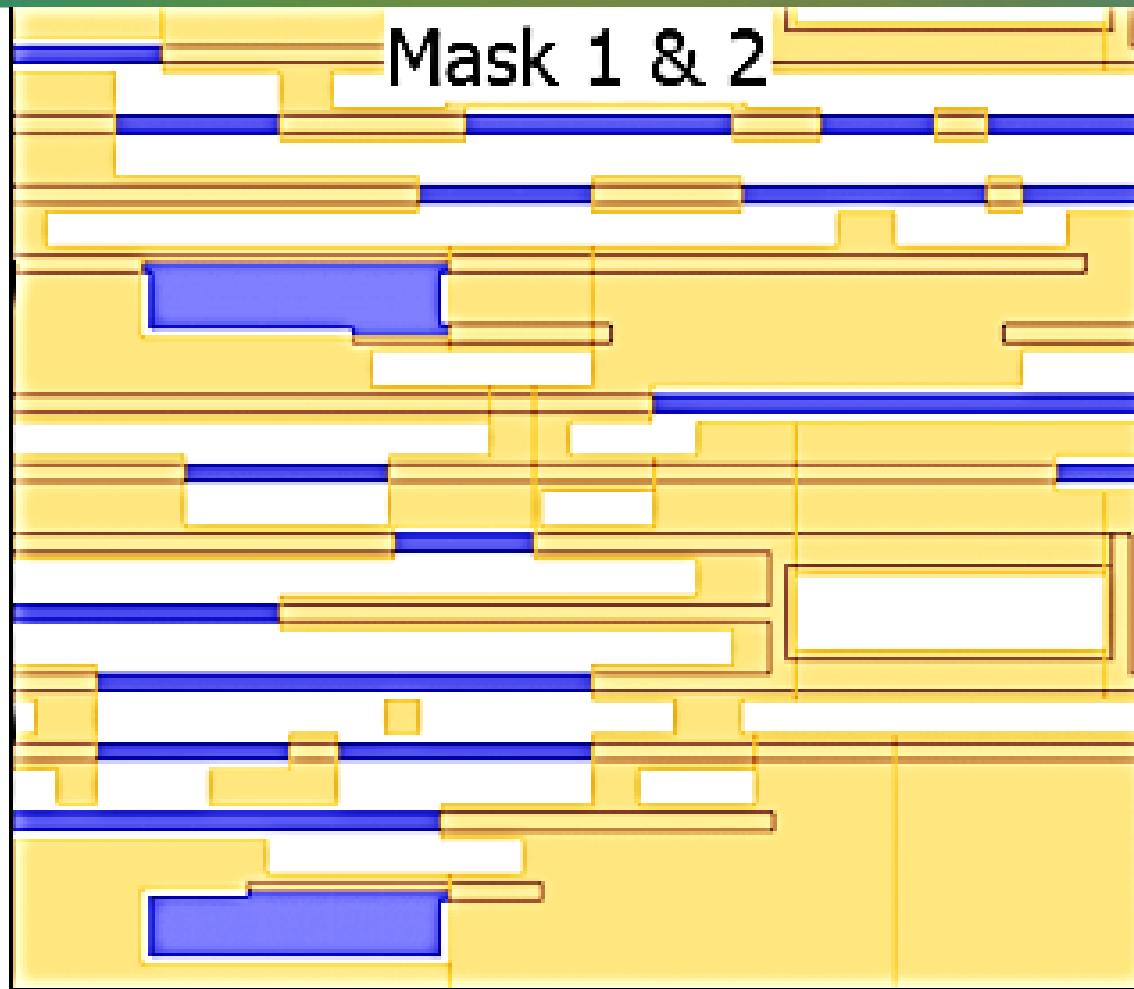
- Mandrel mask looks (sort of) like half of the layout

Self-Aligned Double Patterning



- Block mask looks weird (and costs a lot)

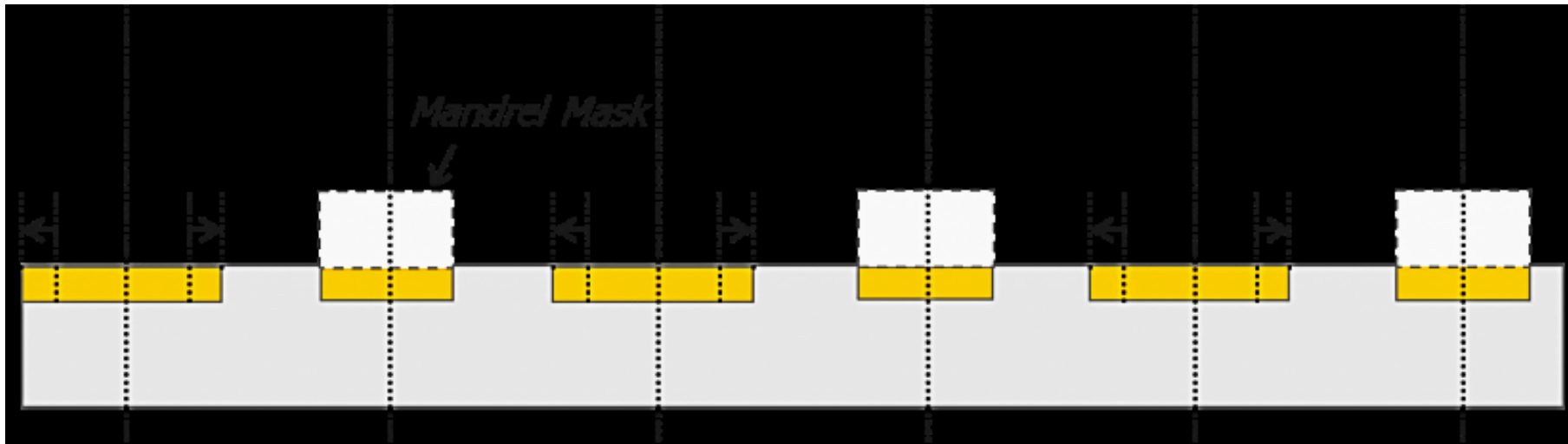
Self-Aligned Double Patterning



- Half of all features are “replicated” by self-aligned process

Limitations and Drawbacks of SADP

- Double patterning still needs two masks
 - Masks are expensive, block mask more so
 - There are additional process steps
- Half of all features are created by a very different process
 - No overlay errors due to self-alignment
 - Non-mandrel shapes are not perfect replicas
 - Mandrel and non-mandrel shapes have different variations



Cut, don't Block

- SADP block mask needs to remove many features

Original Drawn Shapes

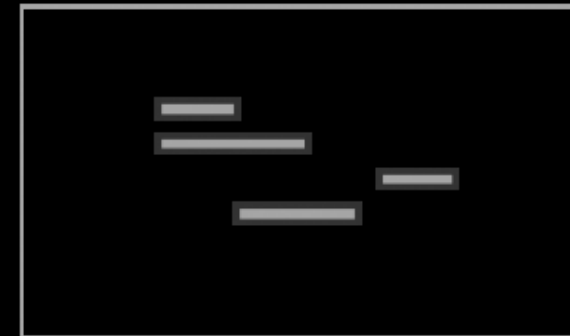
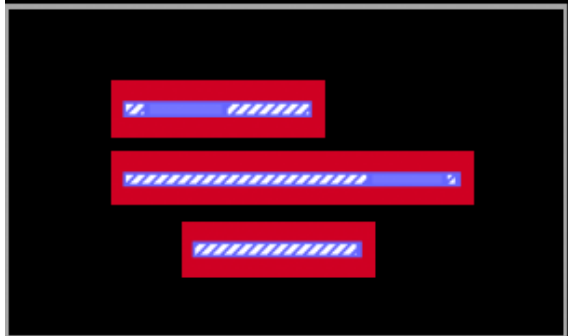
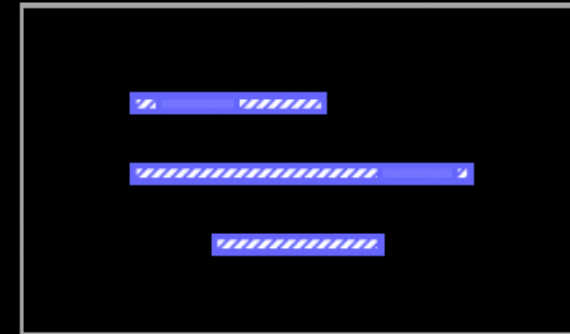
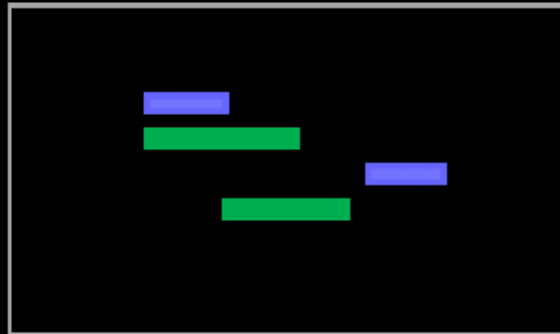
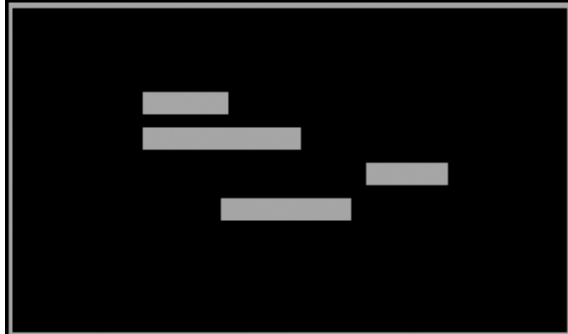
Mandrel/Non-Mandrel Assigned

Mandrel Mask

Spacers That Will Form

Block Mask Over Spacers

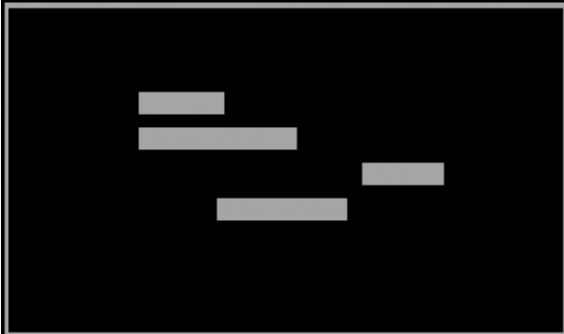
Final Trenches on Wafer



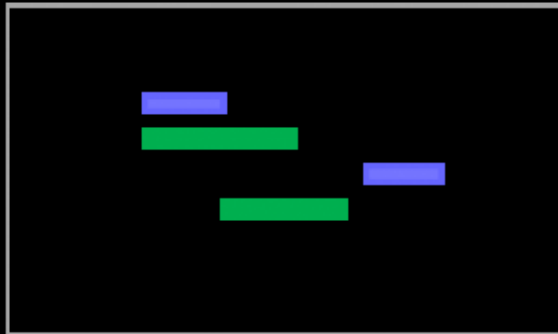
Cut, don't Block

- SADP block mask needs to remove many features
- Can we remove less?

Original Drawn Shapes



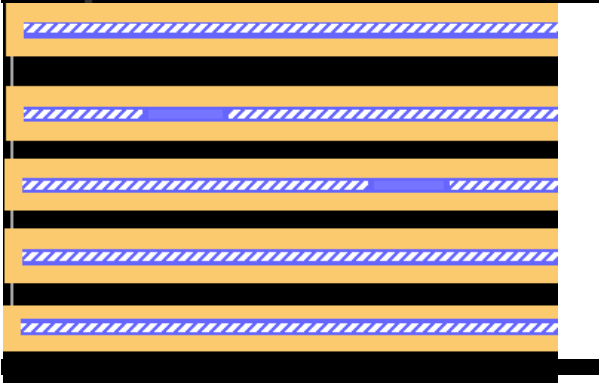
Mandrel/Non-Mandrel Assigned



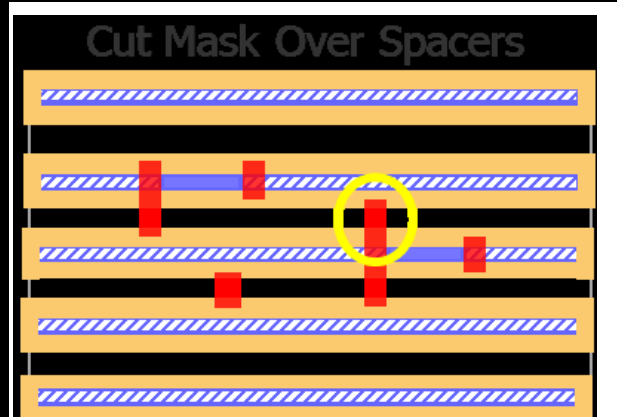
Mandrel Mask



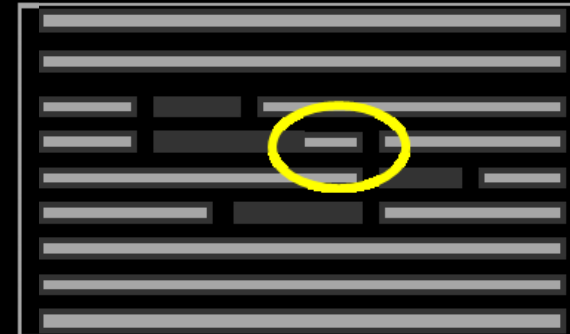
Spacers That Will Form



Cut Mask Over Spacers



Final Trenches on Wafer

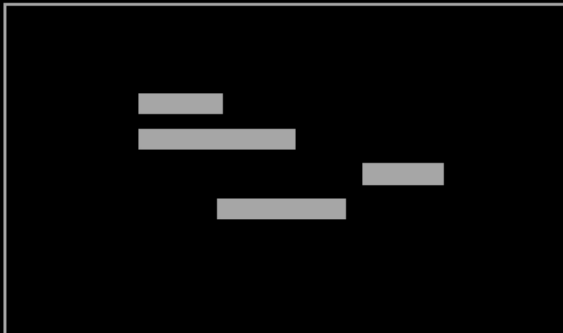


Cut, don't Block

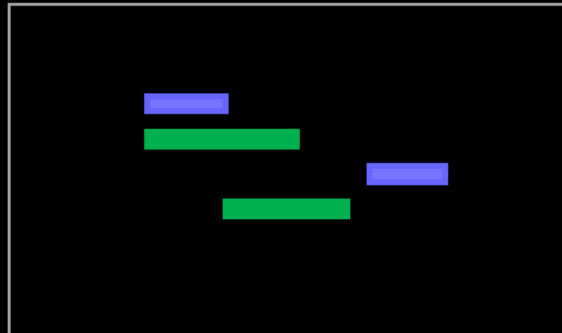
- Cuts ensure correct electrical connectivity
- Cut mask is much simpler but leaves extra meta



Original Drawn Shapes



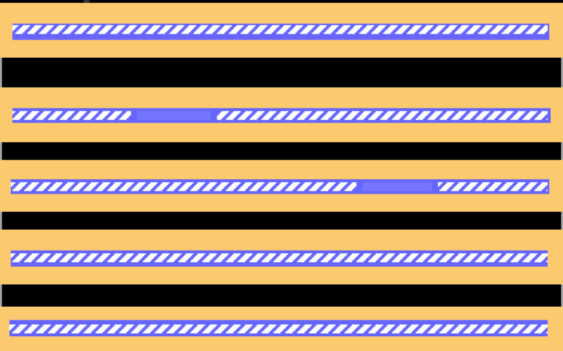
Mandrel/Non-Mandrel Assigned



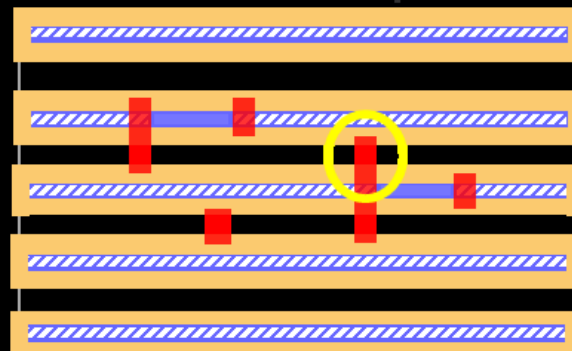
Mandrel Mask



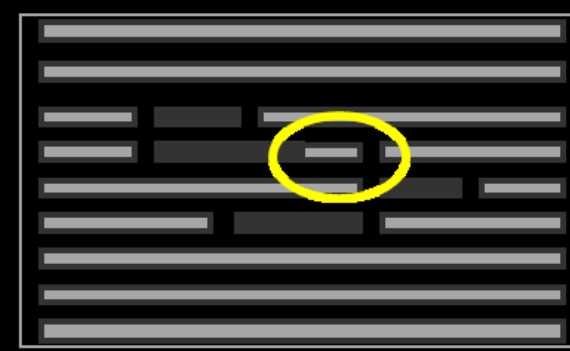
Spacers That Will Form



Cut Mask Over Spacers

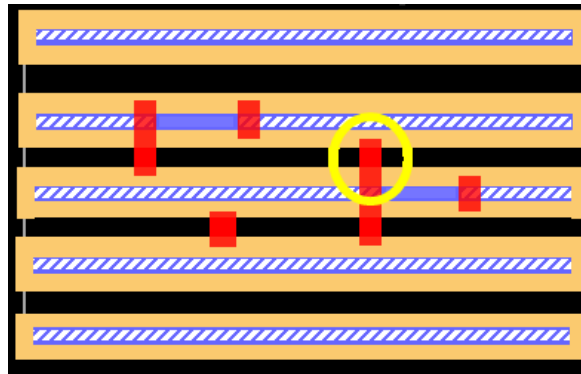


Final Trenches on Wafer



If Two Patterns are Good, Four are Better?

- Self-aligned replication can be repeated to get two more copies of the mandrel shape (SAQP)
 - Works only for 1D layouts – ok for cut masks



- SAQP lets us print very dense grid
 - Too dense to put all cuts on one mask!
- We will need up to 4 cut masks
 - Less if cut rules are very restrictive

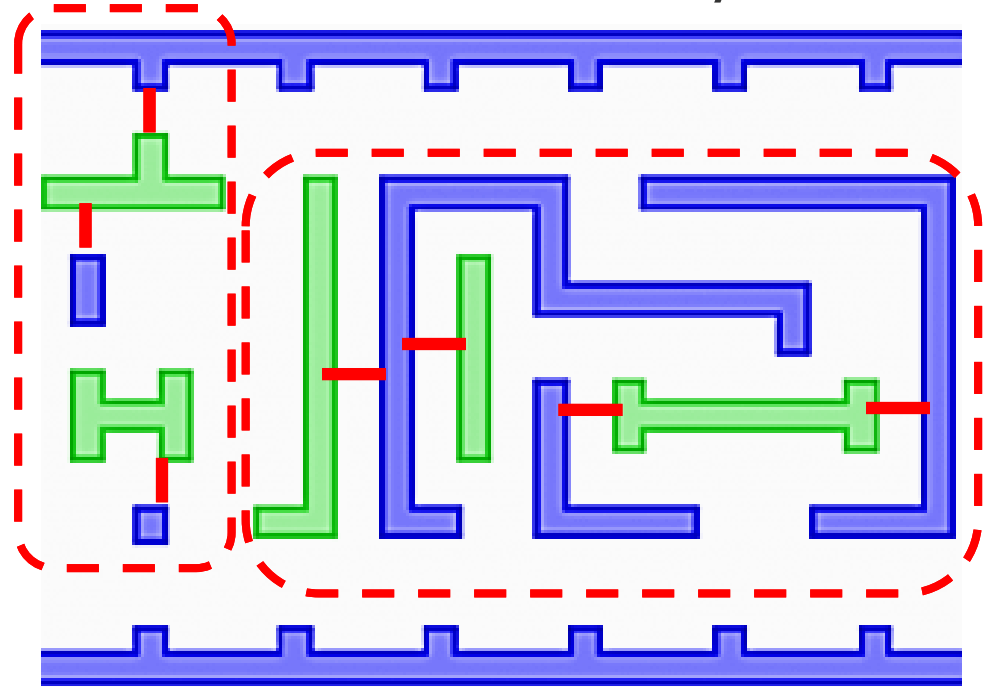
Stitches

- So far we assigned the whole shape to one mask
- Breaking up a shape can reduce mask count



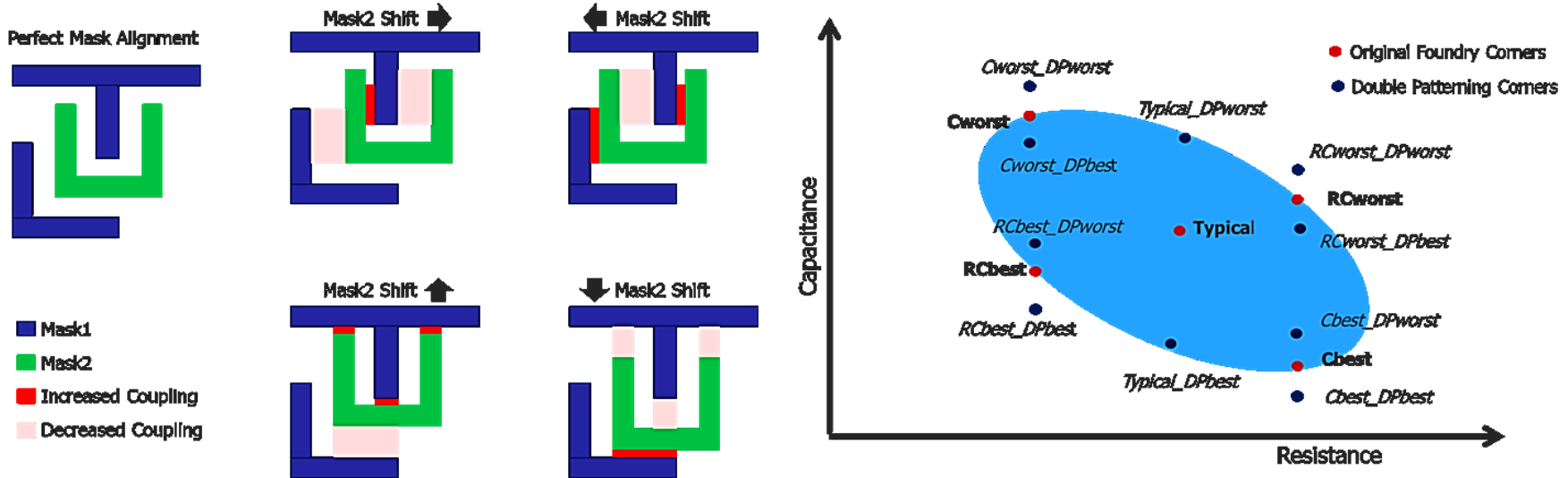
What Makes a Good Decomposition?

- Decomposition has many valid solutions for one layout
 - We can exchange mask 0 and mask 1
 - We can exchange masks separately in each group of independent shapes
 - Triple and quadruple patterning have even more solutions
- Not all solutions are equally good
- Many quality metrics: yield impact, variability, hierarchy preservation, density balancing



MultiPatterning vs Yield and Variability

- No process is perfect – multipatterning leads to variability
 - Example – mask misalignment in LELE

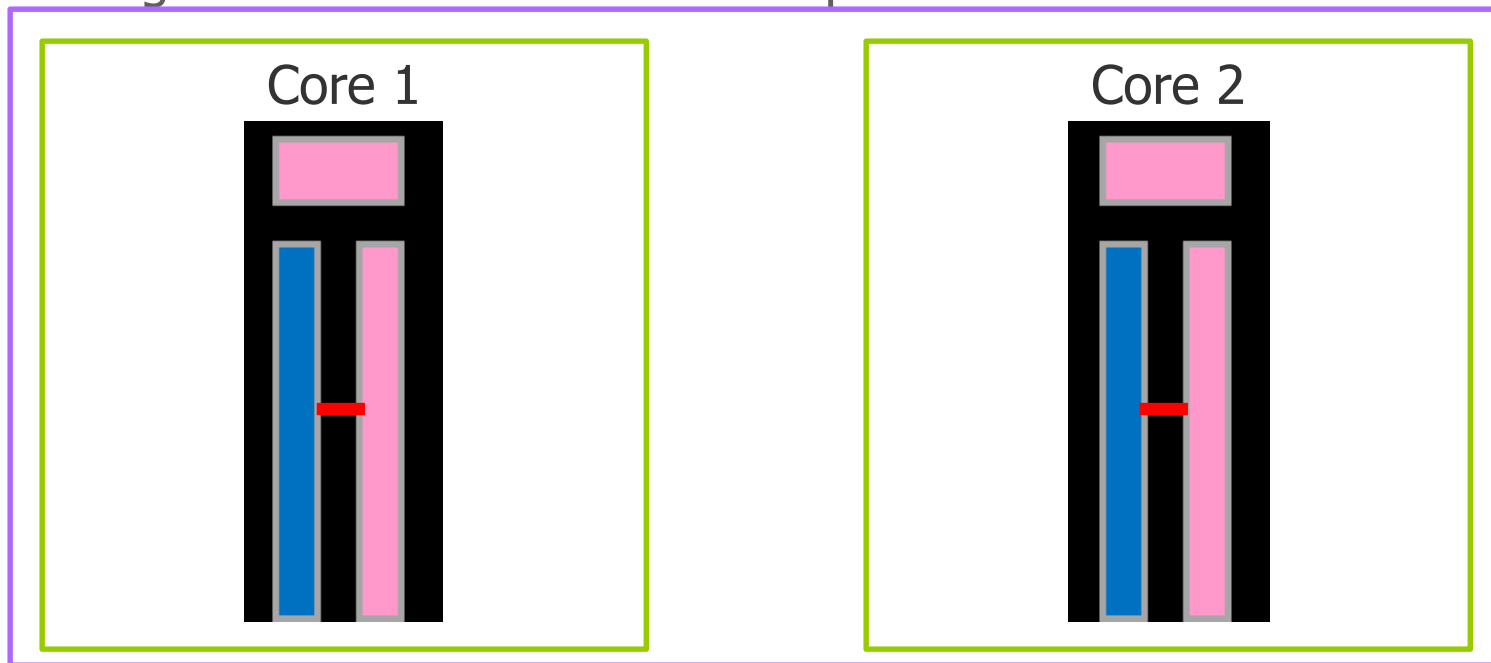


- Extra metal means extra capacitance in SADP with cuts
- Non-mandrel shapes have more width variations
- Stitches are never perfect, wire distortion means extra resistance

- Some parts of the design are more sensitive than others
- Good decomposition minimizes impact of MP on yield

MultiPatterning vs Hierarchy

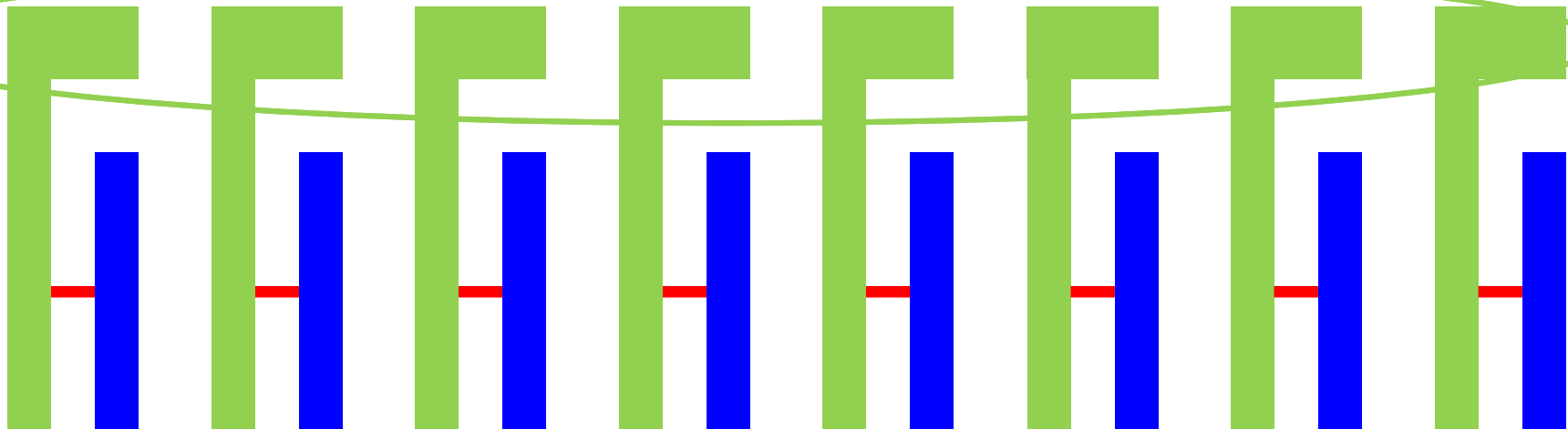
- Most chips today have multiple identical blocks or cores
- Identical blocks should be identically manufactured
 - Less variability between cores, faster OPC and mask processing
 - No guarantee of identical decomposition



- Good decomposition preserves hierarchy

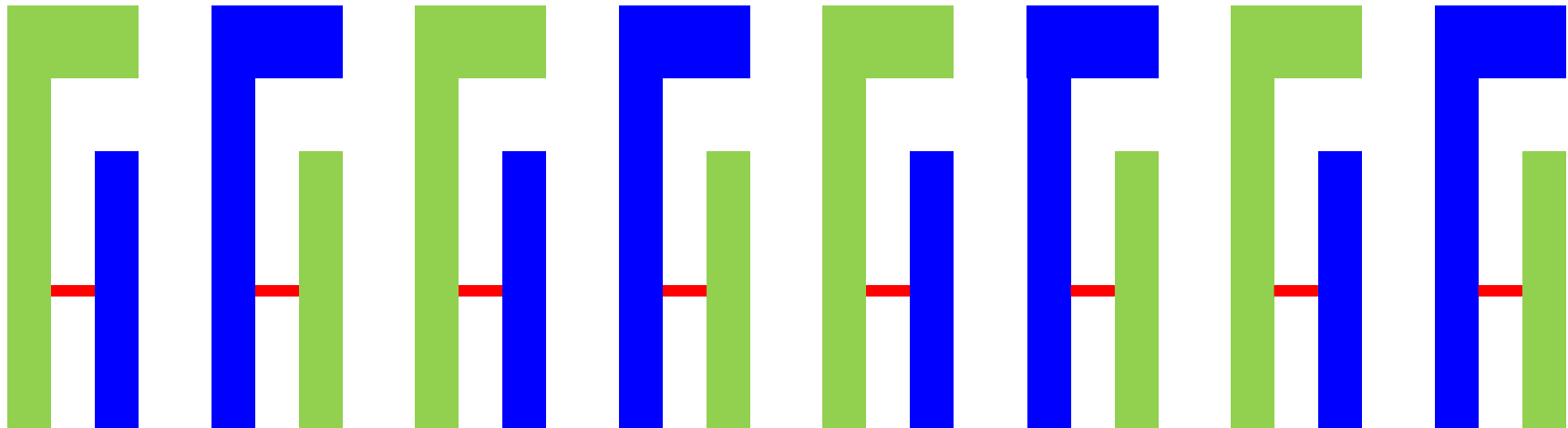
MultiPatterning vs Density Balancing

- Traditional density balancing: density must be sufficiently uniform across the die (no large empty spaces on the die)
- New density balancing for multipatterning: all masks must have similar and uniform density



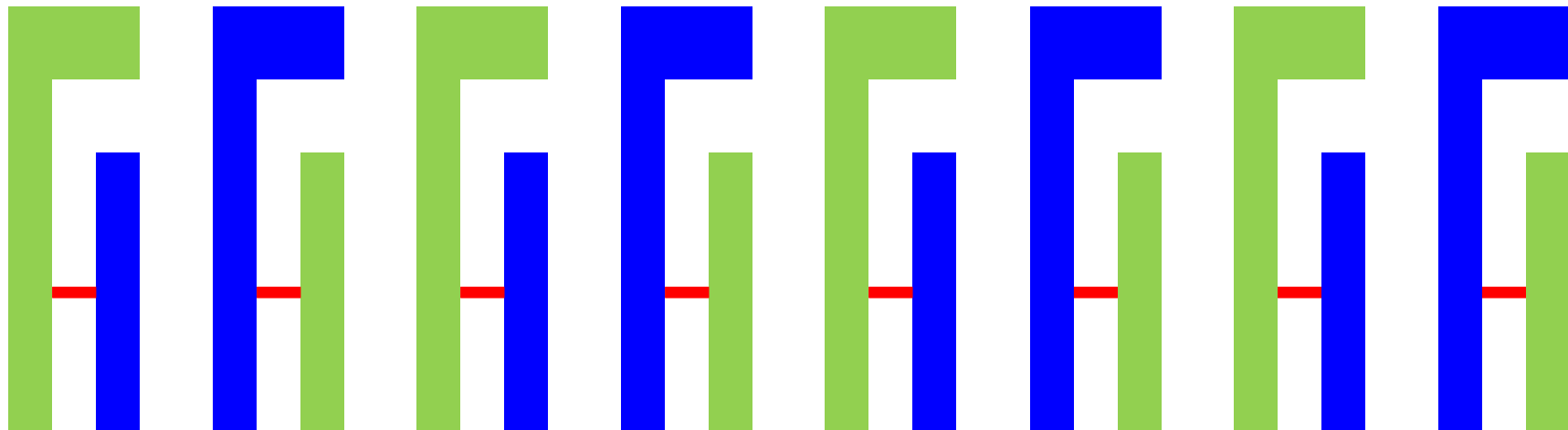
MultiPatterning vs Density Balancing

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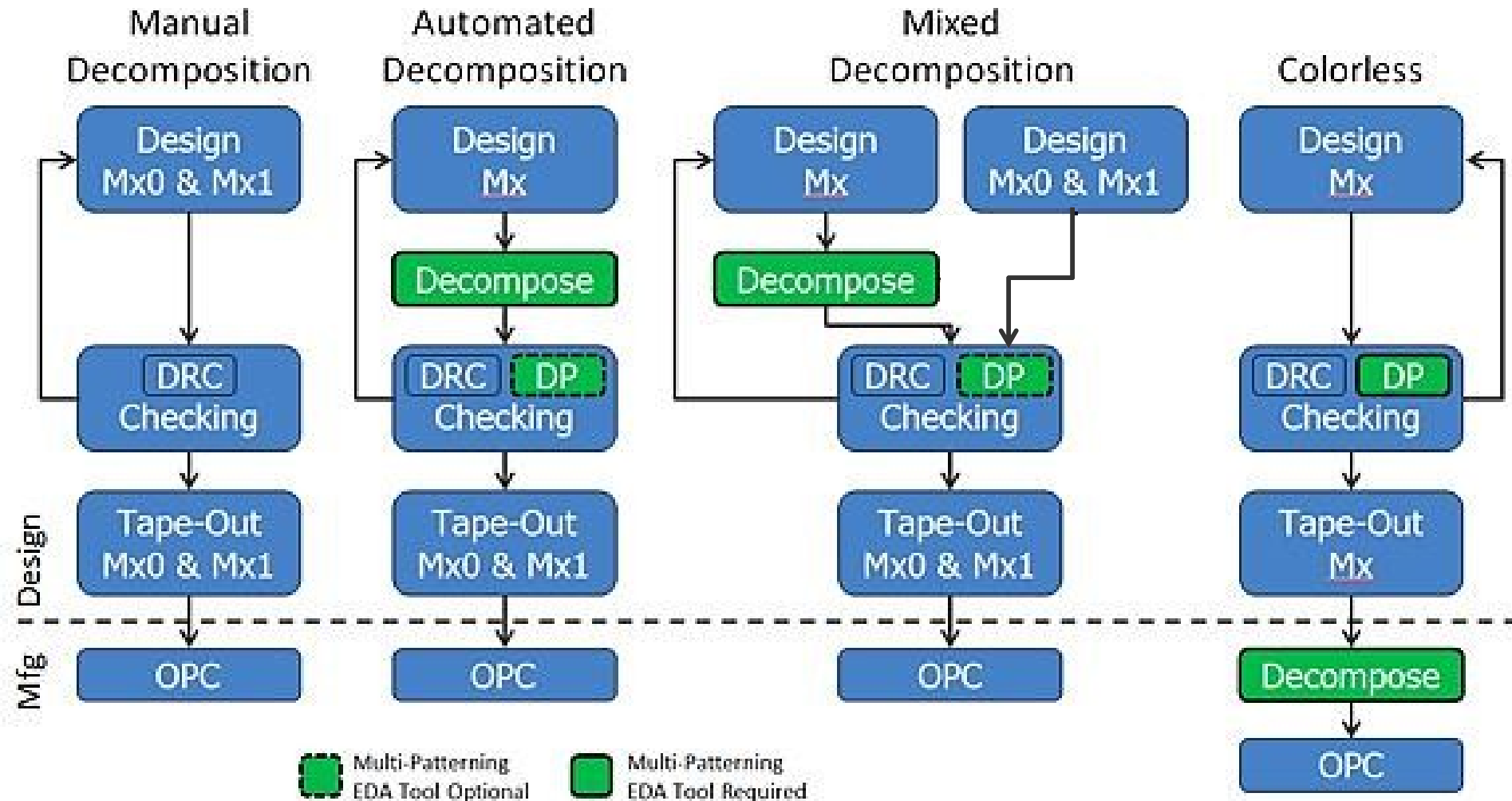
Hierarchy Preservation vs Density Balancing

- Preserving a block means decomposing it the same way in every placement
- This preserves and magnifies any density imbalance within the block

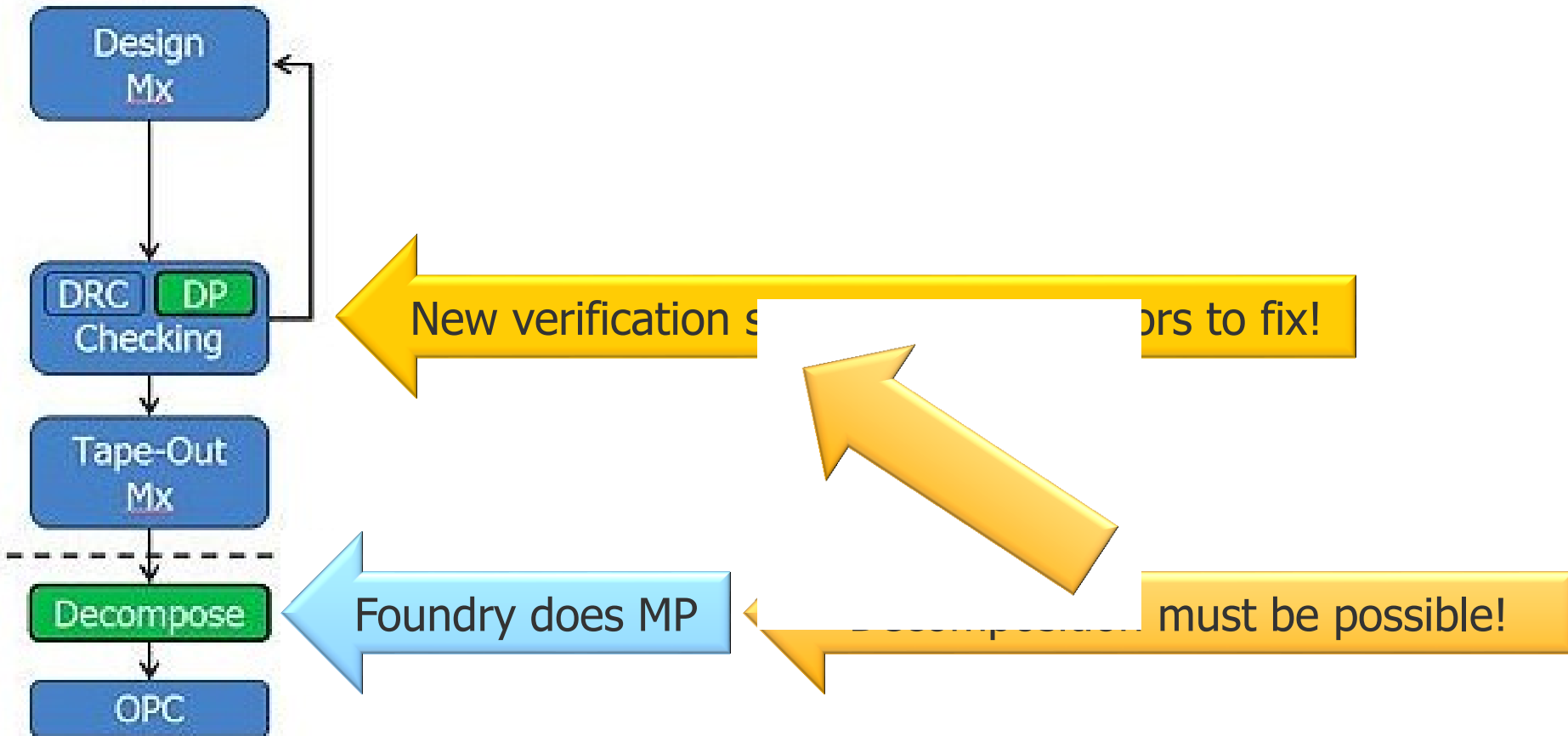


- Decomposition quality metrics sometimes conflict with each other

Multi-Patterning in Real World

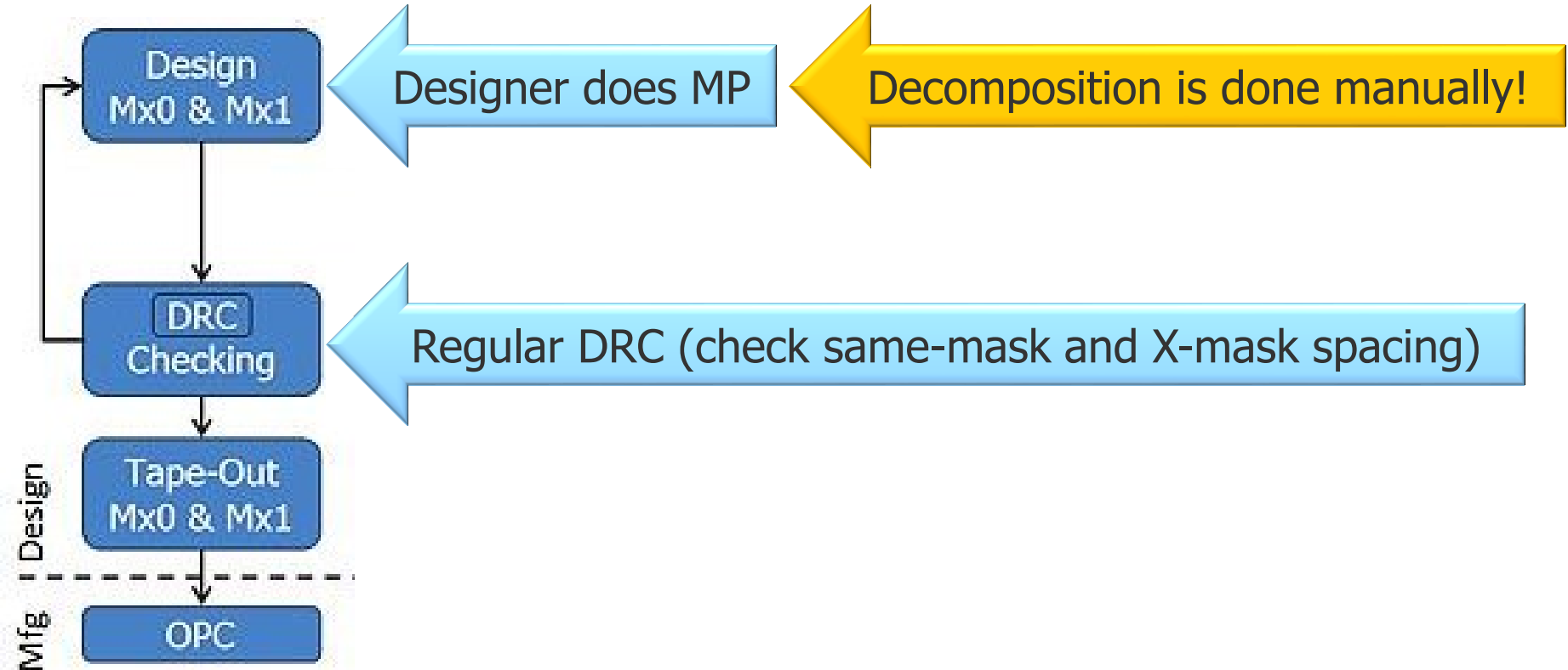


MultiPatterning and EDA Tools – “Colorless”



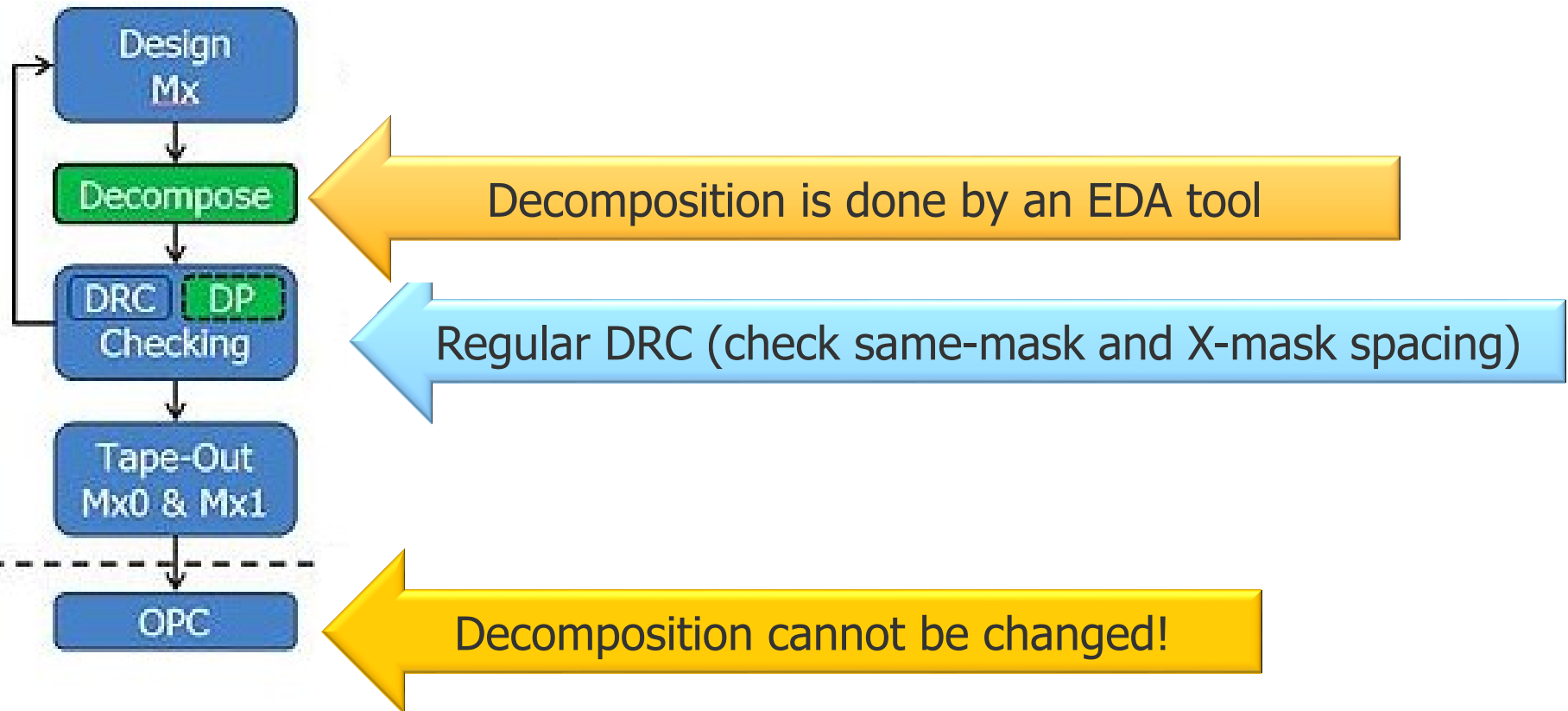
- “Colorless” flow – designers verify that decomposition (coloring) is possible but do not assign masks

MultiPatterning and EDA Tools – “Colored”



- “Colored” flow – designers must decompose the layout, mask assignment is part of the tapeout

MultiPatterning and EDA Tools – “Colored”



- “Colored” flow – designers decompose the layout using EDA tools, mask assignment is part of the tapeout

Colored vs Colorless Flow

- Colored flow – tape out with colors (mask assignments)
 - + What you see is what you get
 - Designers have to learn (more) about multipatterning
 - Foundry has to share detailed process information
 - Foundry cannot alter decomposition to improve yield, fine-tune process, etc
- Colorless flow – tape out as one layer, foundry does decomposition
 - DRC verification must ensure that decomposition is possible
 - Different tools used by designer and foundry give different results
 - Tool used by the foundry may fail to find a solution or find one of poor quality; designer found good solution and passed DRC
 - + Foundry is free to improve the process, including MP technology
 - + Designer does not need to know process details and complex interactions between MP and lithography

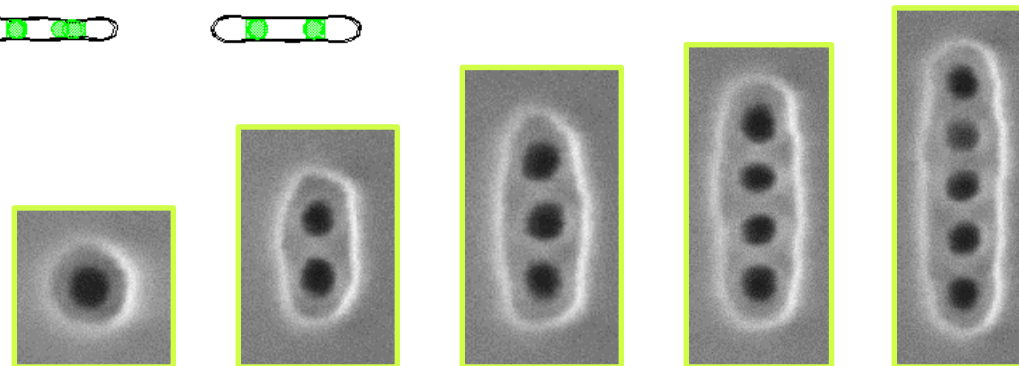
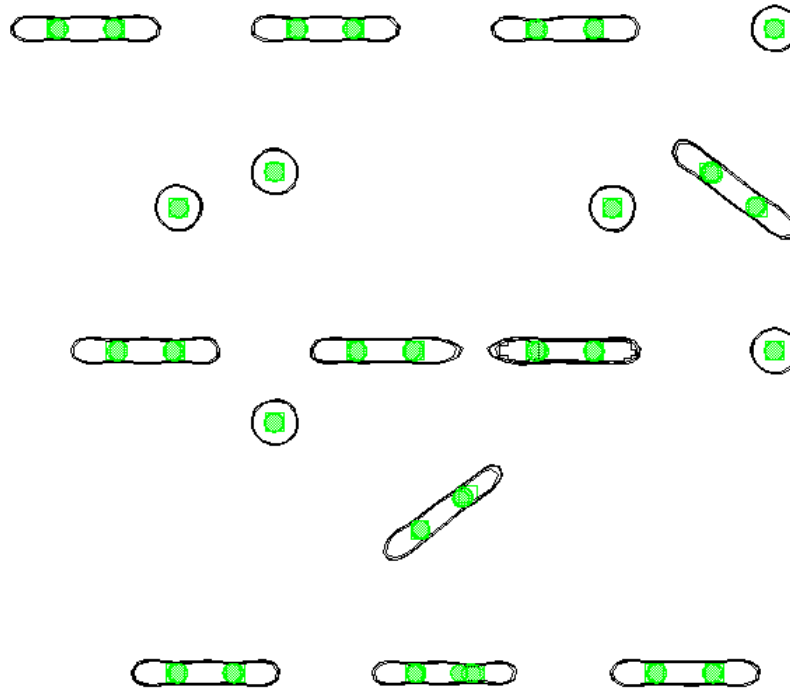
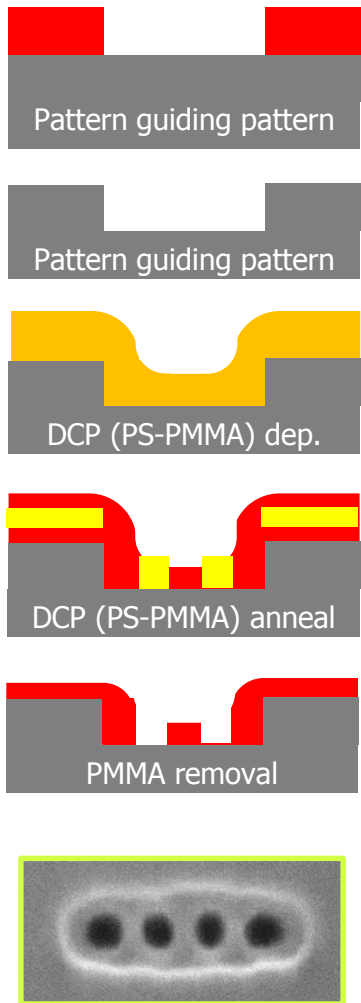
Conclusions

- Multipatterning is necessary to enable IC manufacturing progress without significant progress in lithography technologies
- Several multipatterning techniques are available, the best option must be selected for each process and each layer
- Best multipatterning approach is determined by cost and strengths/weaknesses of each technique
- Multiple quality metrics exist for a decomposition solution, the best solution is often a compromise
- Multipatterning impacts both design and manufacturing

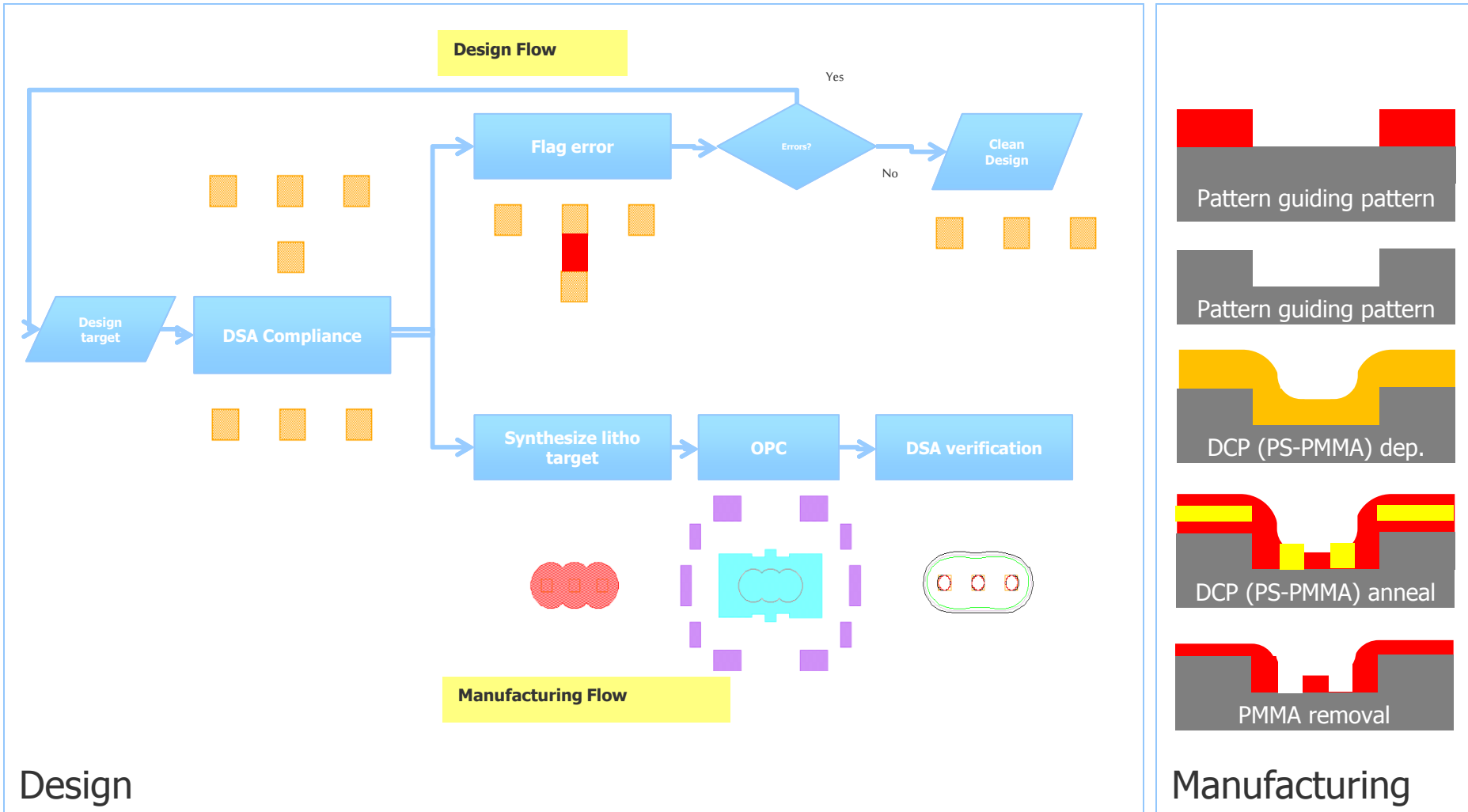
Outline – Direct Self-Assembly (DSA)

- What is DSA?
- Why use DSA?
- Combining DSA and multi-patterning
- DSA-aware coloring
- DSA Compact models
- DSA and design restrictions

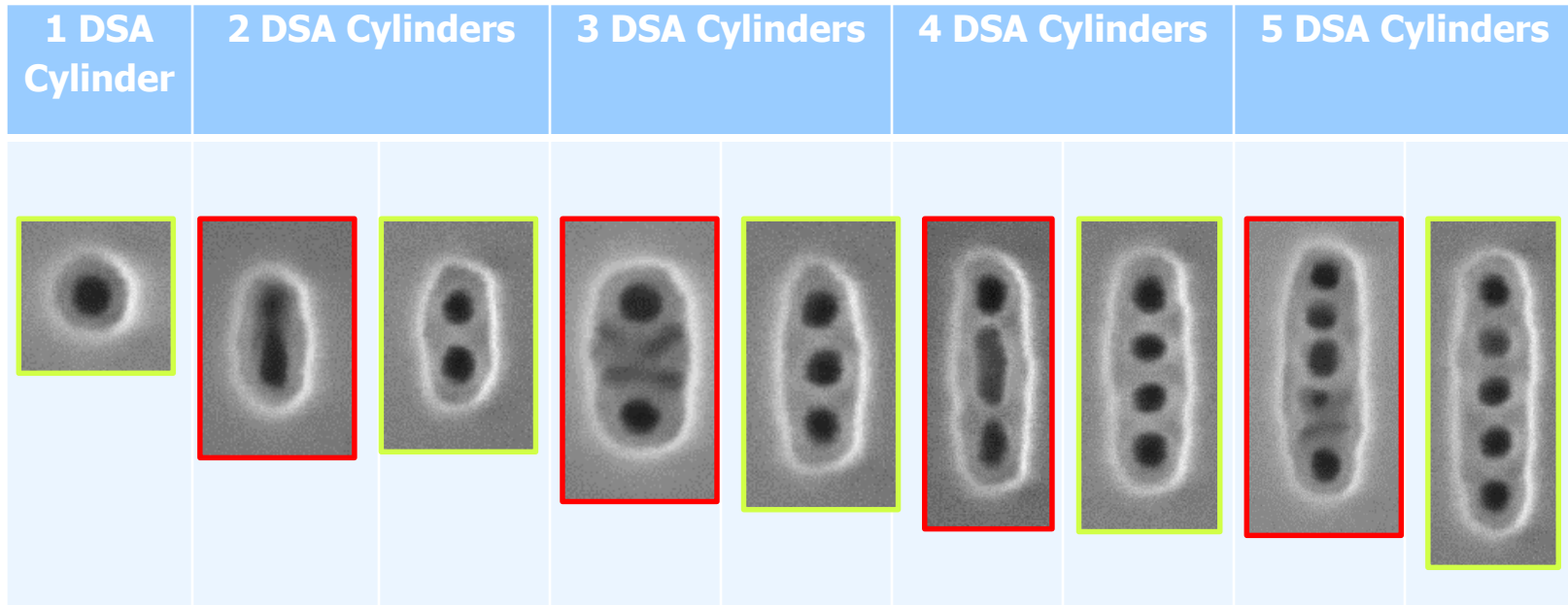
Direct Self-Assembly (DSA)



DSA Process: Grapho-epitaxy for hole printing.



Experimental data

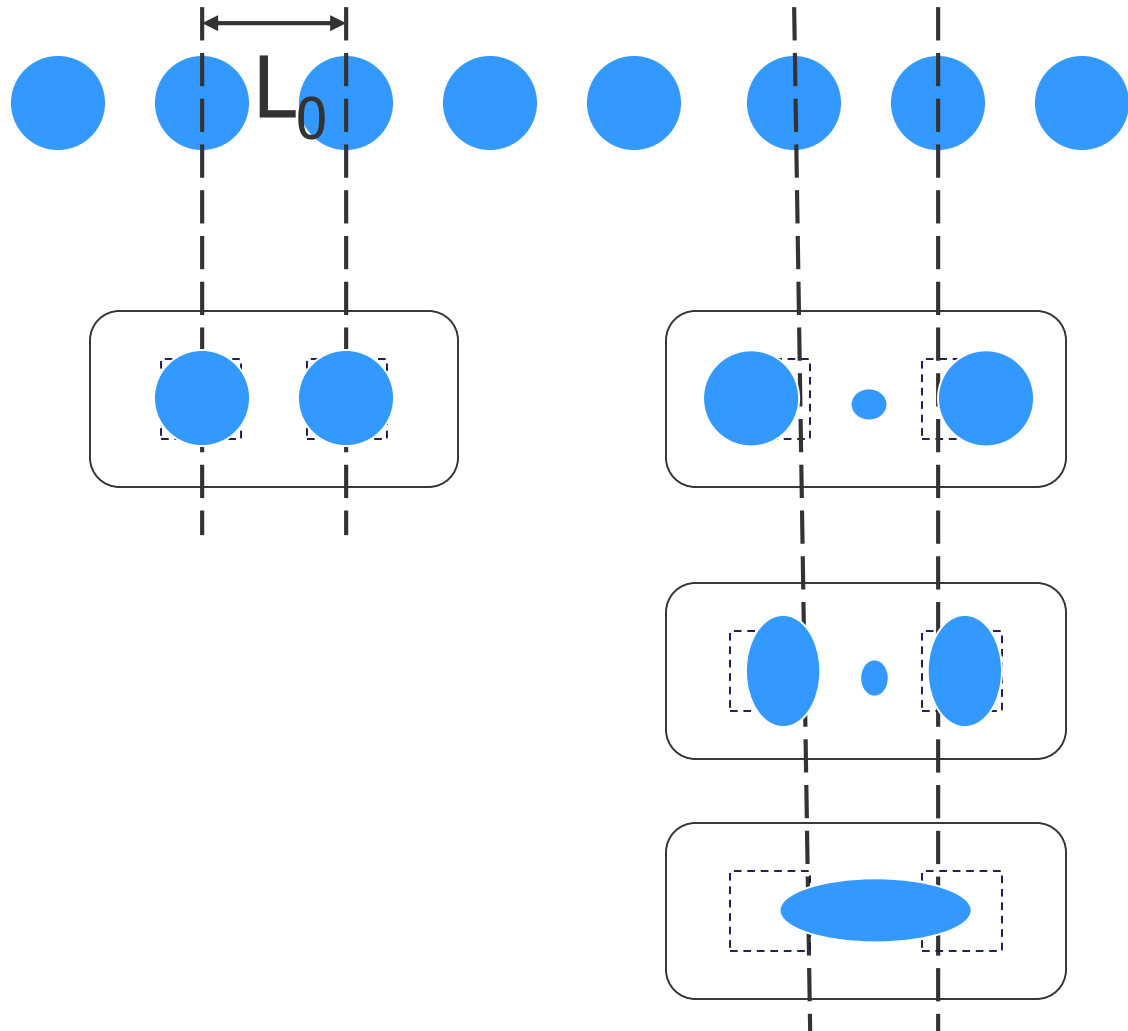


Not in Phase Transition
Phase Transition

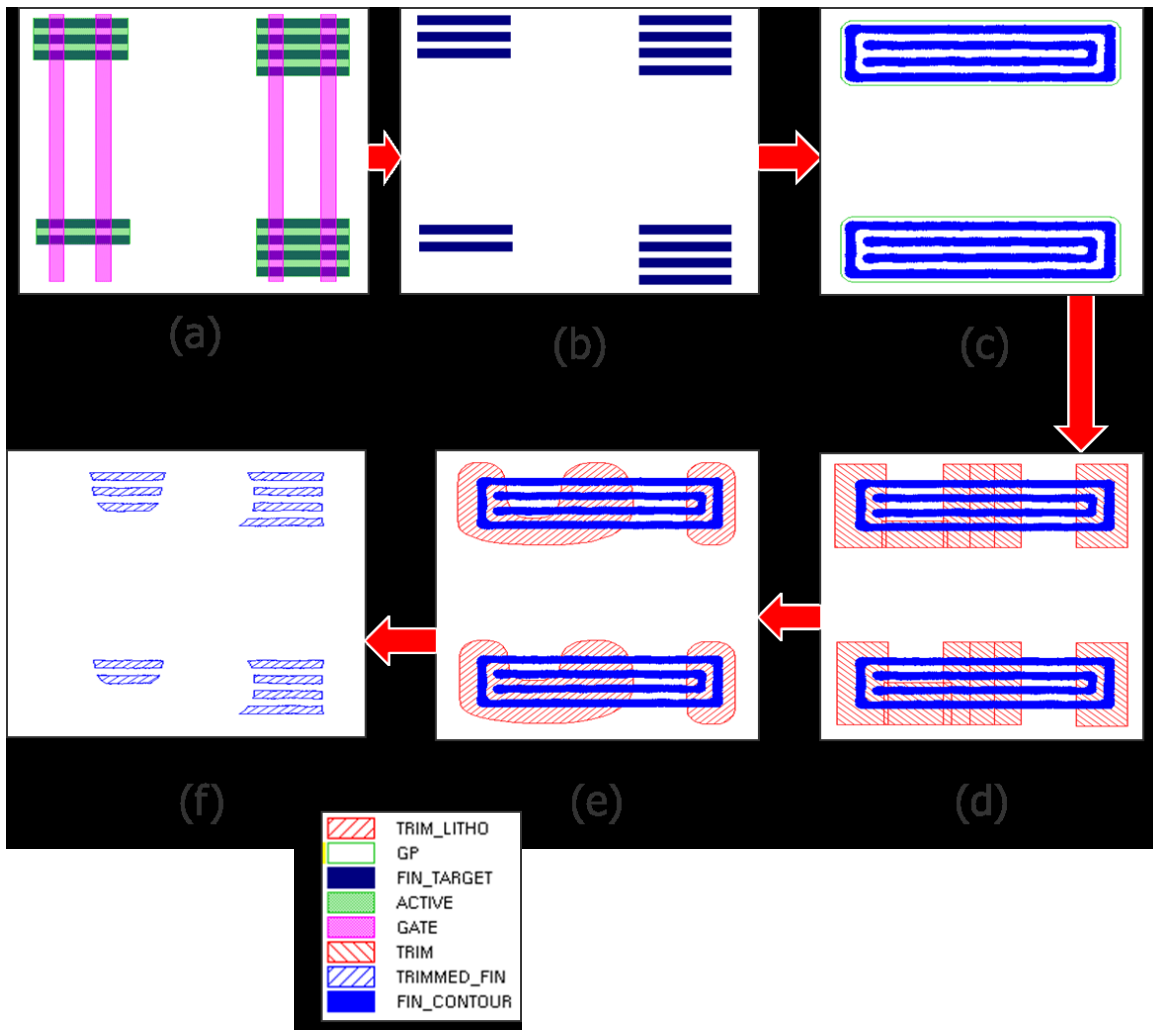
Need to be able to identify guiding pattern images that are in phase transition on full chip (compact model)

Order phase transition

- BCP formulations exhibit a natural periodicity (L_0)
- When confinement is not commensurable to the natural BCP periodicity, a phase transition happens.
- Phase transition conditions are metastable and their morphology impossible to predict systematically.

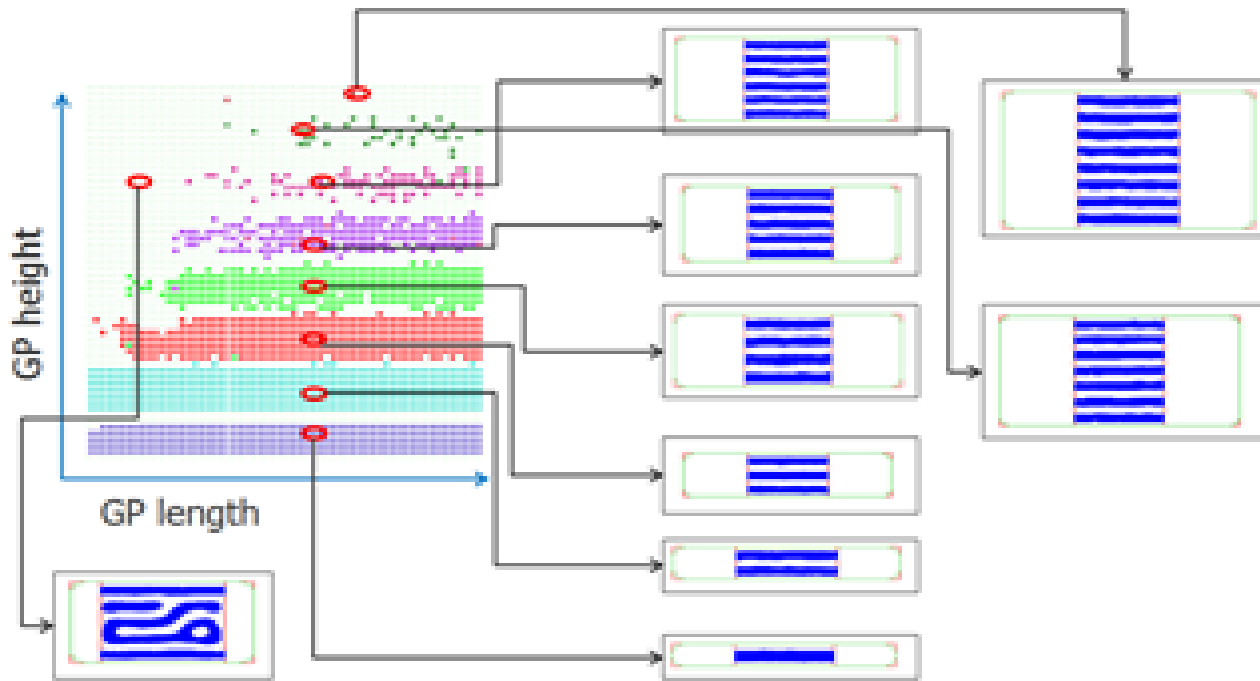


DSA for FinFET Fins



- a) Intended layout
- b) Fins
- c) DSA fins (Grouped to maximize assembly robustness)
- d) Trim region
- e) Trim post litho (shows the importance of proper OPC)
- f) Trimmed fins

DSA for FinFET Fins



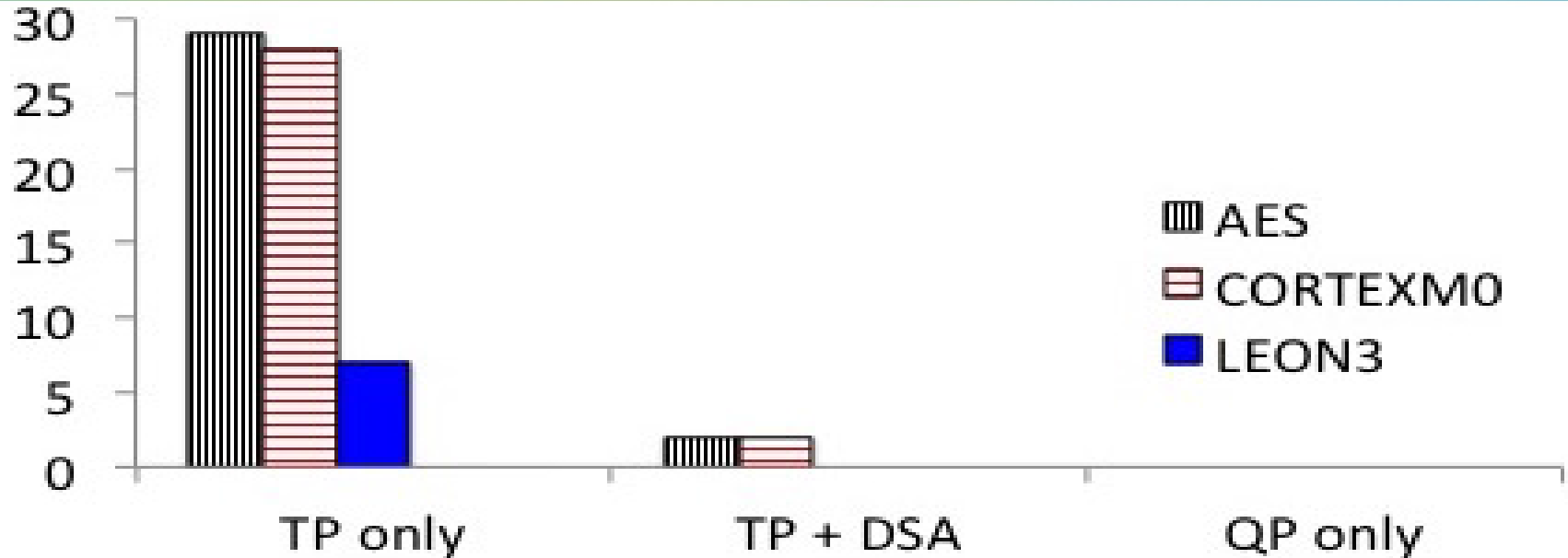
J. Mitra "Process, Design Rule and Layout Co-optimization for sub-10nm FinFet Devices using DSA" DAC 2015

- There is no single fin control
- There is an optimal aspect ratio for every discrete number of contacts
- There are forbidden regions where assembly doesn't occur
- There are optimal regions where assembly is very robust

Where Does DSA Fit into Manufacturing?

Technology	Number of masks for Metal	Number of masks for via	DSA	Risk
Metal MP + Via MP	2 or 3 Depending on cut-mask distribution	3	No	Low (no new technologies required)
Metal MP + Via DP	2 or 3 Depending on cut-mask distribution	2	Yes	Medium (DSA process required)
Metal single + Via DP	1 (EUV)	2	Yes	High (DSA and EUV process required)

Using DSA to Reduce number of MP Masks



- DSA can be used to reduce number of masks
- Trying to create DSA groups after MP decomposition usually does not work 100%
 - Can be made to work with some design restrictions
 - Can be made to work with combined MP-DSA decomposition (DSA-aware decomposition)

DSA-Compliant Layout Design

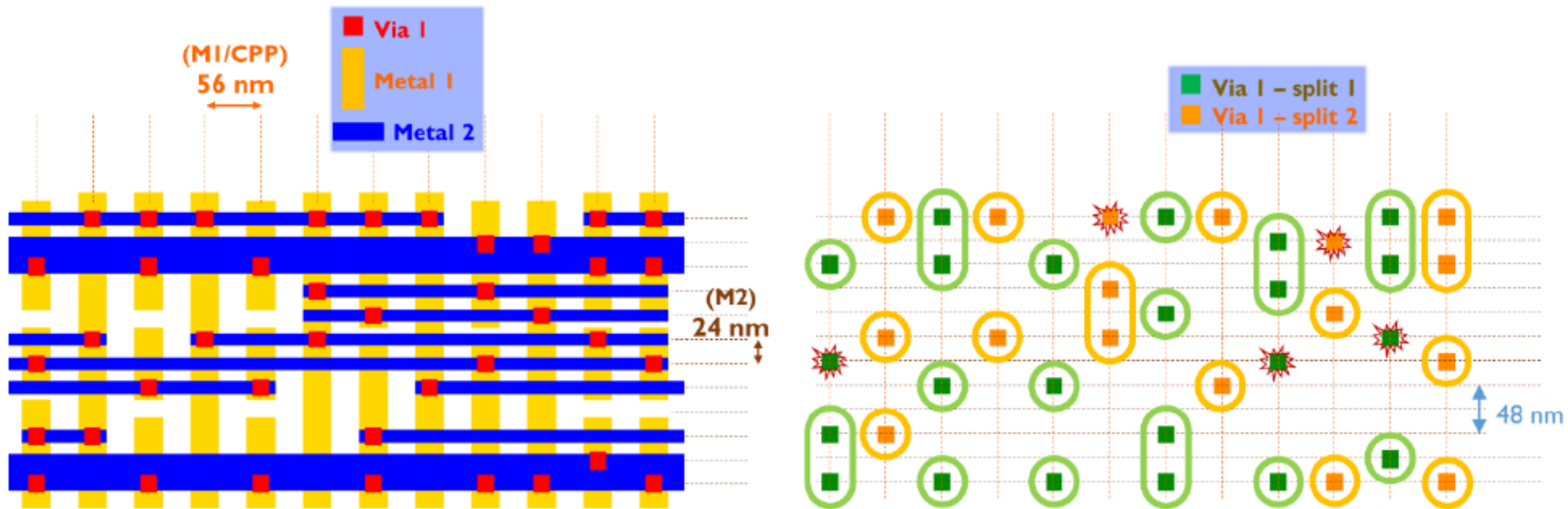
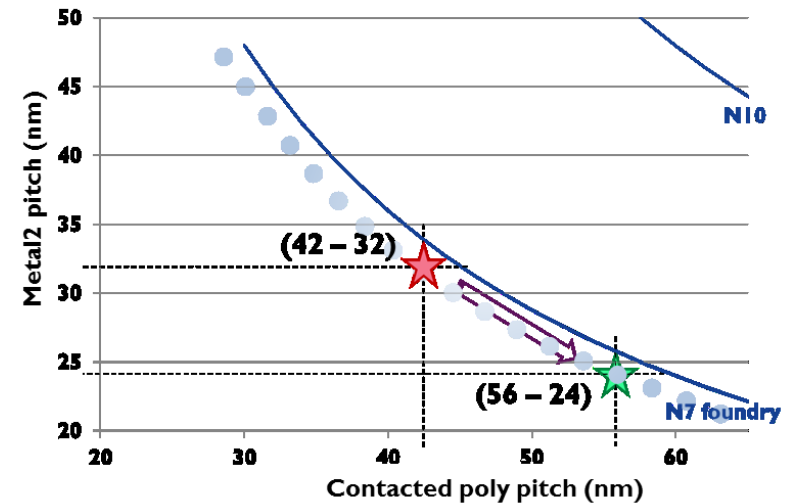
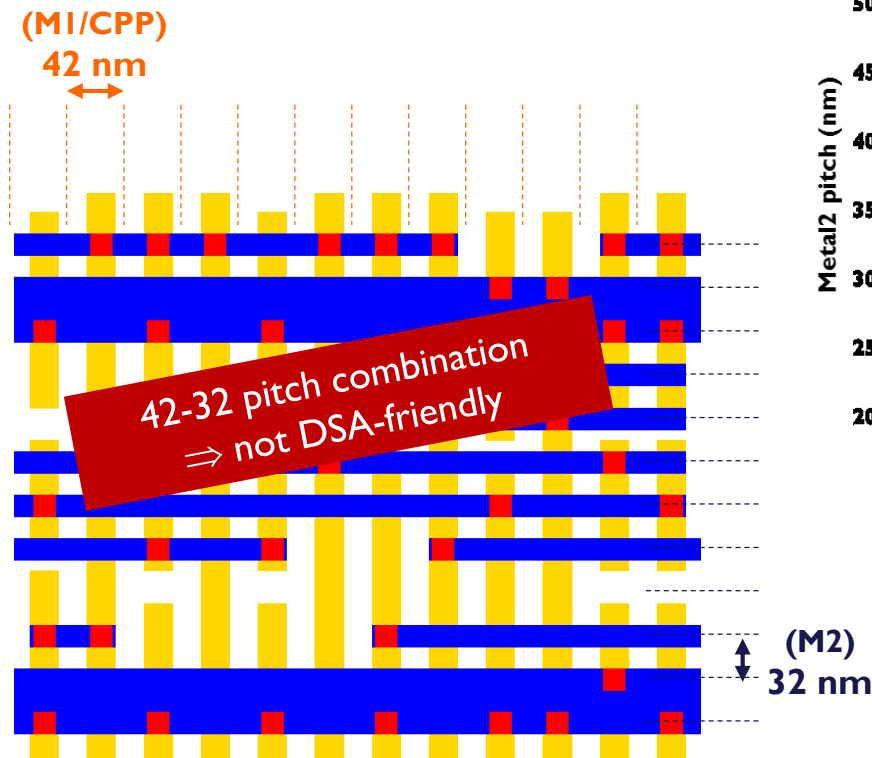
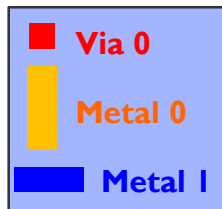


Figure 10. The altered N7 design allows for much simpler DSA decomposition and paves the road for a 2-color option.

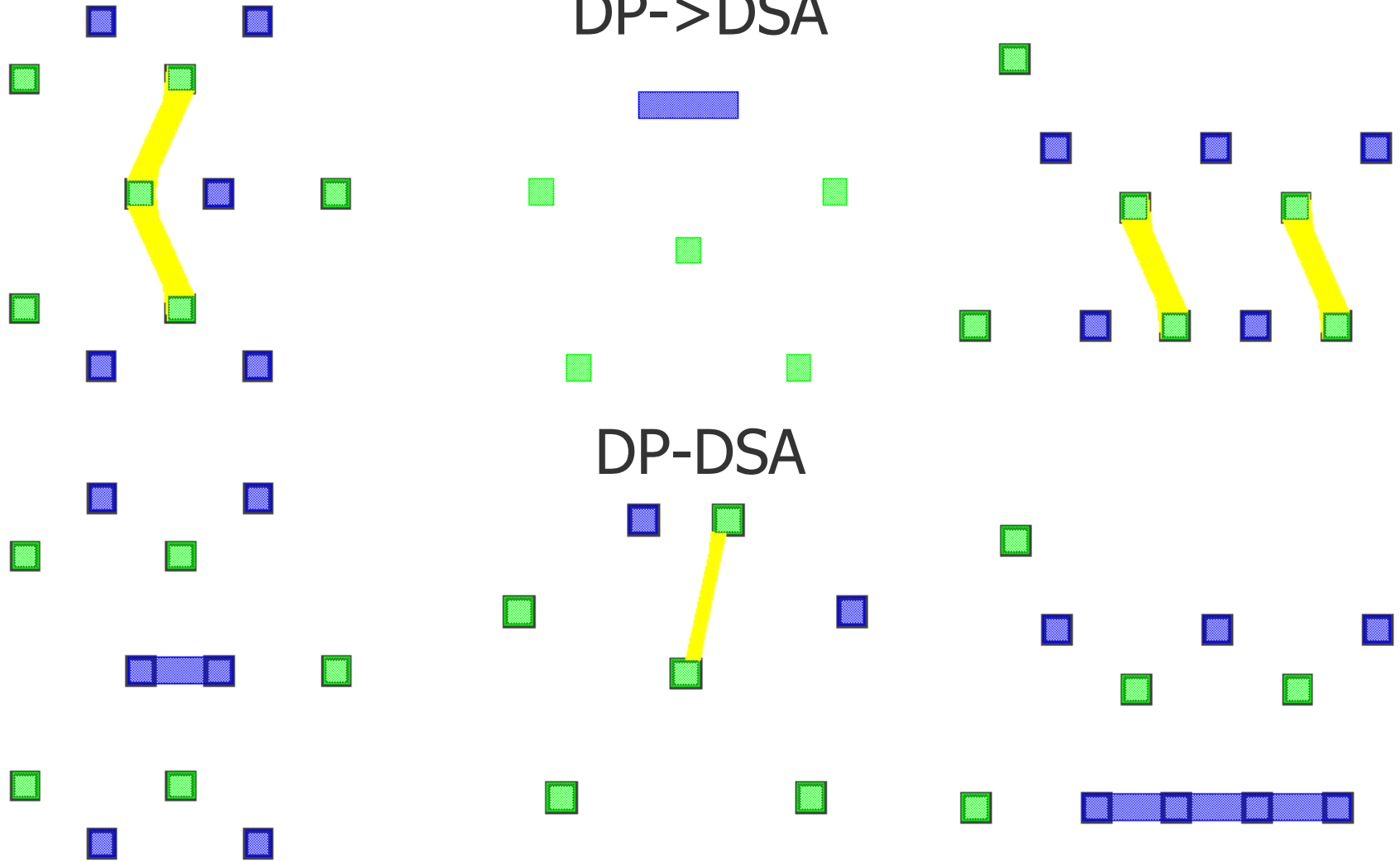
R. Gronheid, J. Doise, et al "Implementation of templated DSA for via layer patterning at the 7nm node". Proceedings of SPIE Advanced lithography 2015

- Metal is unidirectional to facilitate a multi-patterning approach.
- Some re-design is still required to accommodate DSA groups. Why? Because 2D content is transferred to density of vias, as every 2D metal bend becomes a via in this type of layout style.

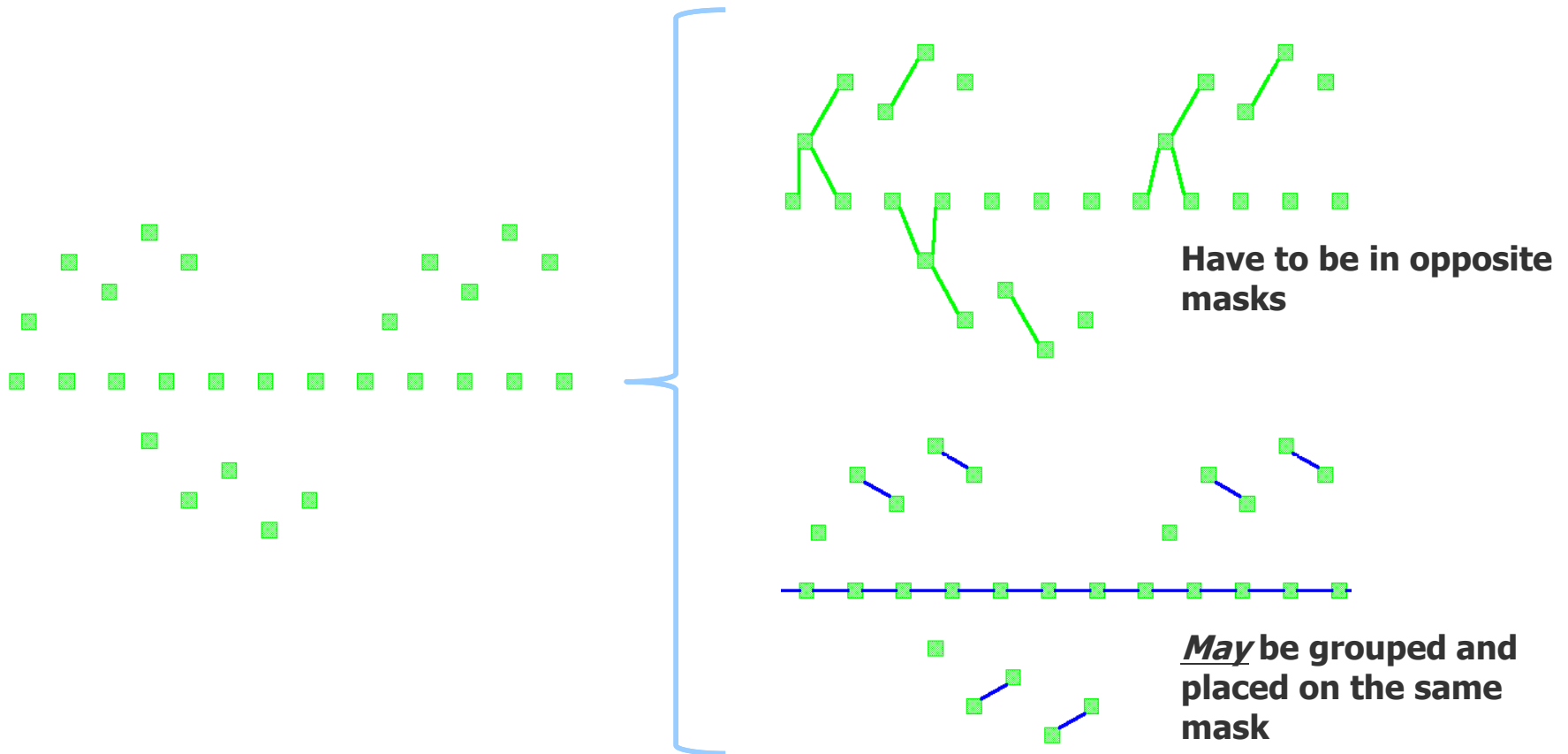
DSA-friendly layout Co-optimization of DSA and design is required



DSA-Aware MultiPatterning

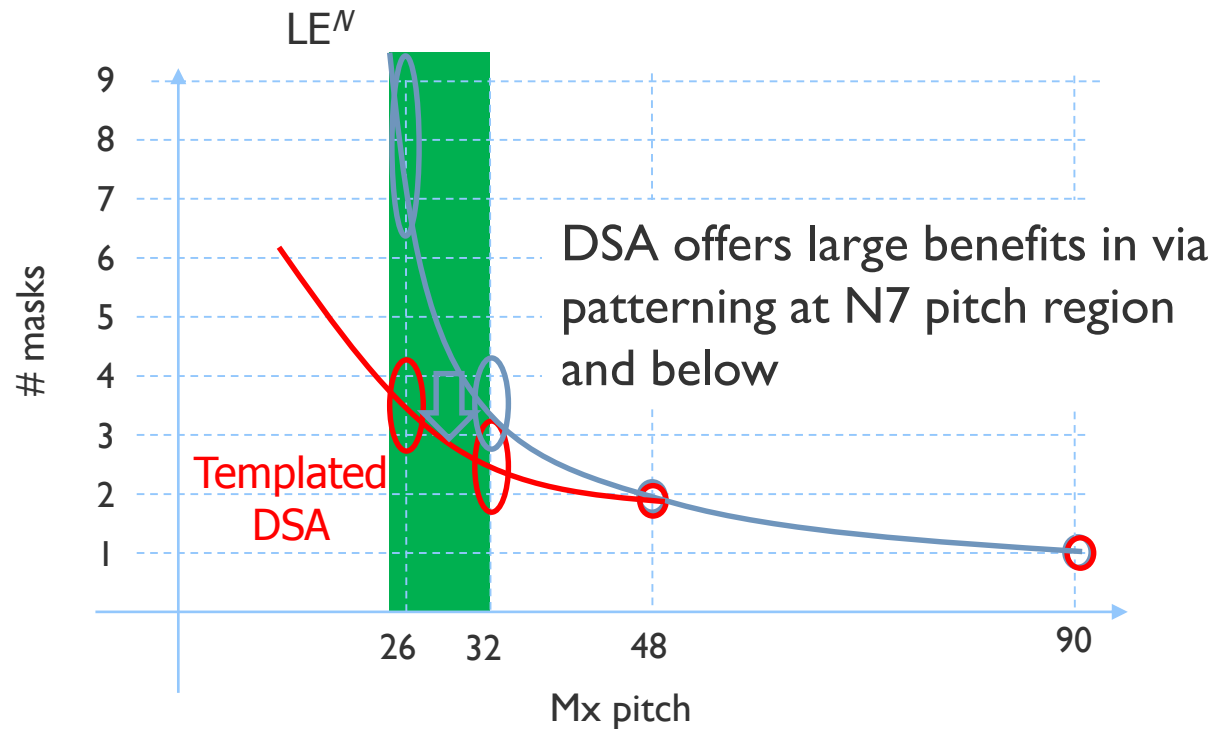


DSA-aware DP: Separator selection



- Theoretically, the more holes to be grouped, the smaller the number of masks; however, in practice the spatial distribution of the holes and the increased noise of DSA for larger groups limit the number of masks that can be safely removed.

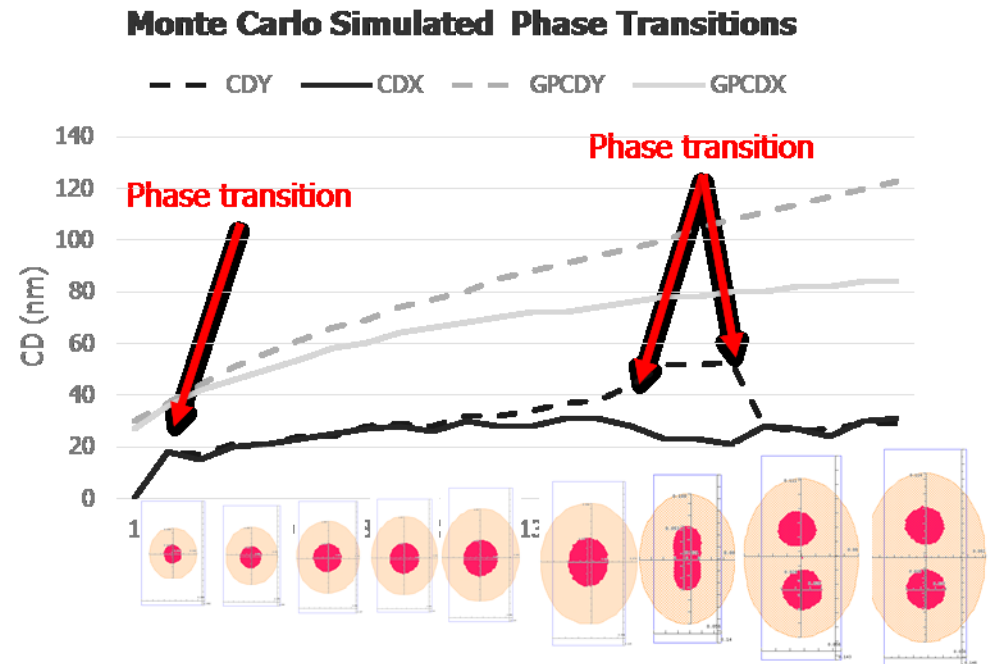
Required mask # for Vx patterning



As the Mx pitch is reduced, the number of masks DSA can reduce increases.

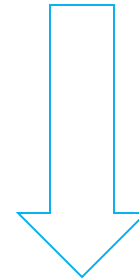
DSA Compact model

- Goal of the compact model is to represent complex systems in a useful and computationally inexpensive way
- To be useful the compact model needs to provide:
 - For correction and verification: Accurate hole placement (i.e. center to center displacements)
 - For verification: Predict when there is no proper assembly (i.e. the guiding pattern defined an order phase transition).



Creating a DSA Compact Model

Compact Model Calibration

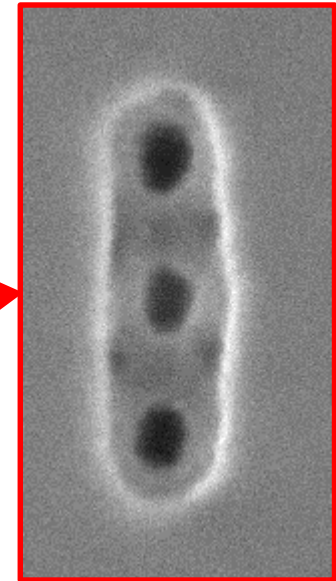
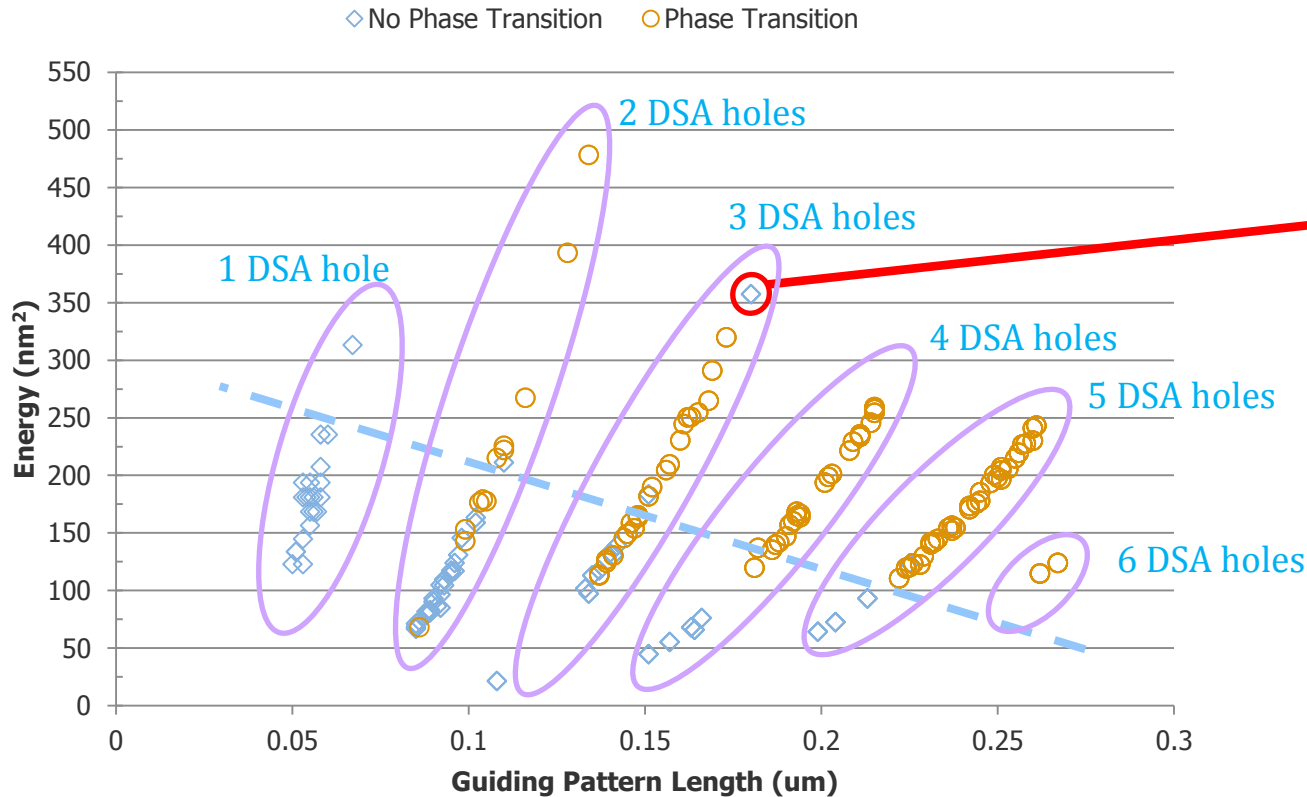


Compact Model Phase Verification

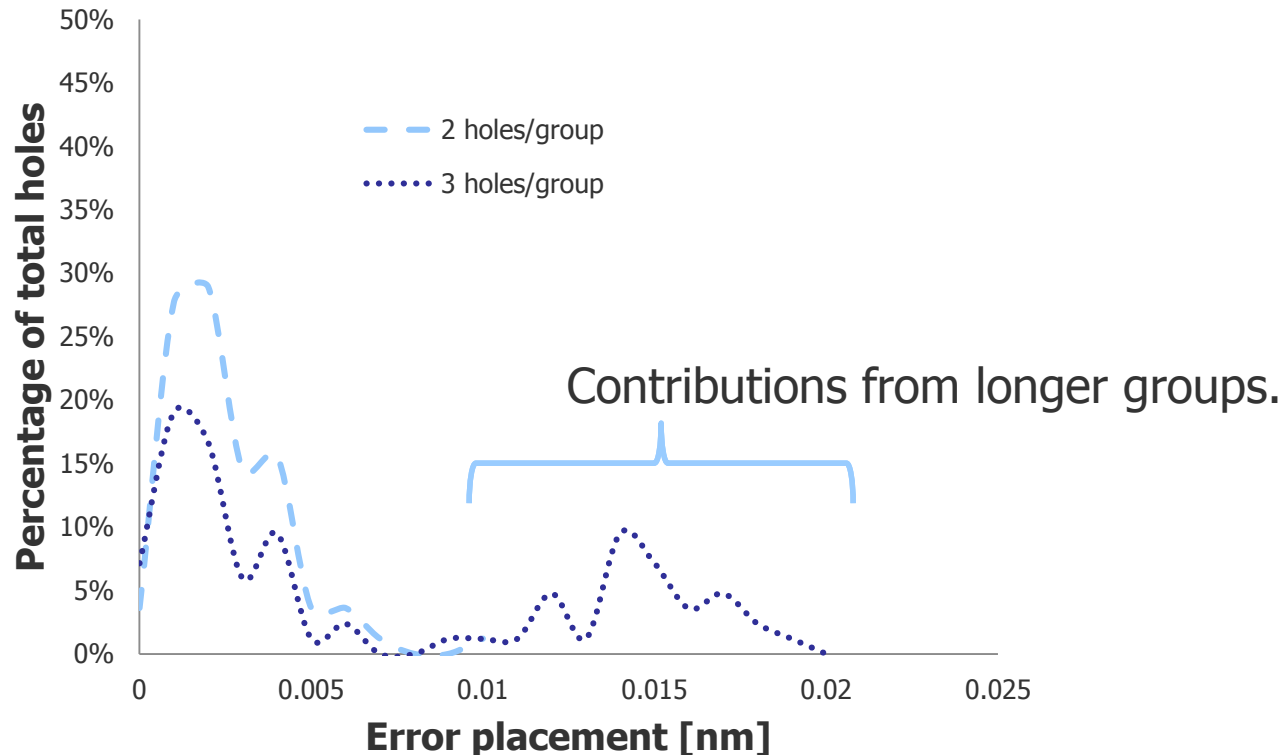


Experimental validation of 'energy' as a phase transition metric

DSA Guiding Pattern Length vs Energy



PW-Error Placement depends strongly in maximum number of holes in a group



- Error placement computed center to center (actual vs reference) considering:
 - 4%EL, 20nm DOF, +/- 0.25nm mask bias (1X)

Conclusions

- DSA feasibility is demonstrated for several applications
 - Each application must be specifically targeted
- DSA can be used to reduce the cost of multipatterning
- Multipatterning needs to be DSA-aware
- Use of DSA will likely impact design rules
 - Design co-optimization required to fully realize DSA potential
- DSA can be combined with traditional lithography or EUV
- Compact models and full-chip DSA models are required to compute DSA guiding patterns and estimate variability

THANK YOU