Xing (Sean) Wei

2016-1-28

Easy-logic technology ltd.

RTL-level circuit

Gate-level circuit

Circuit-level circuit

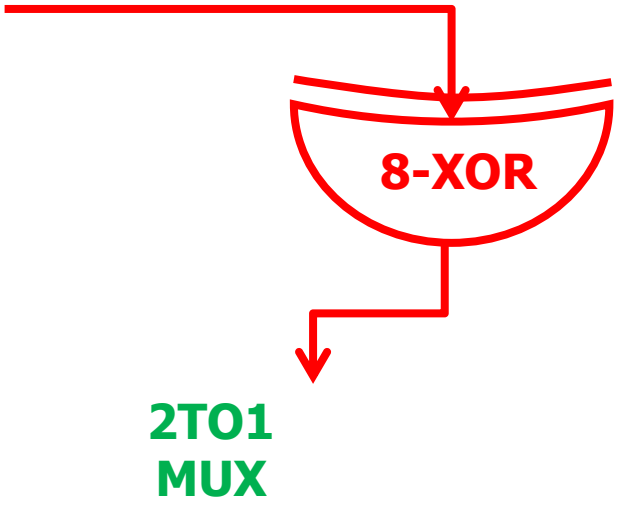
Chip

We need tools to detect HT!

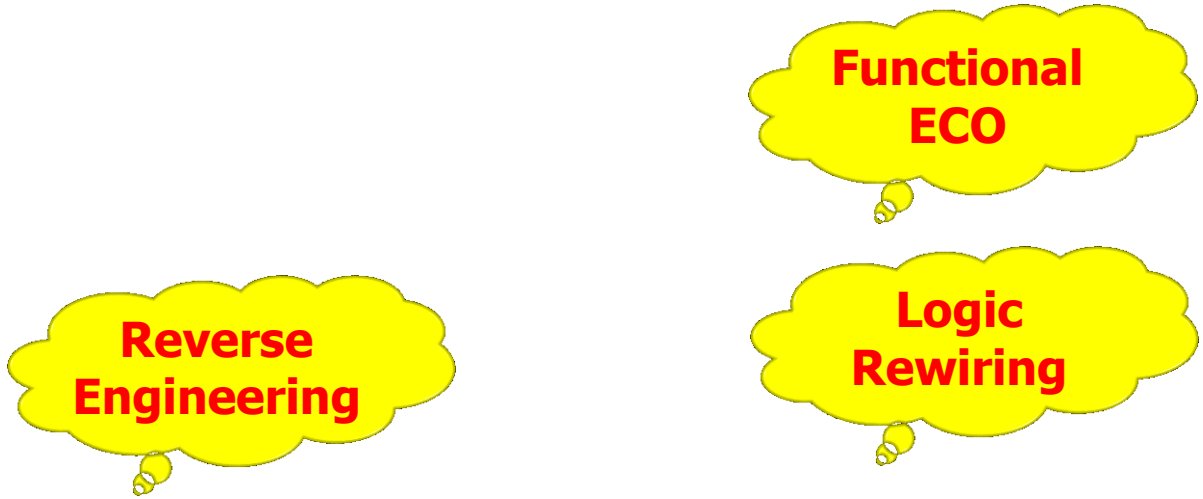
Chip

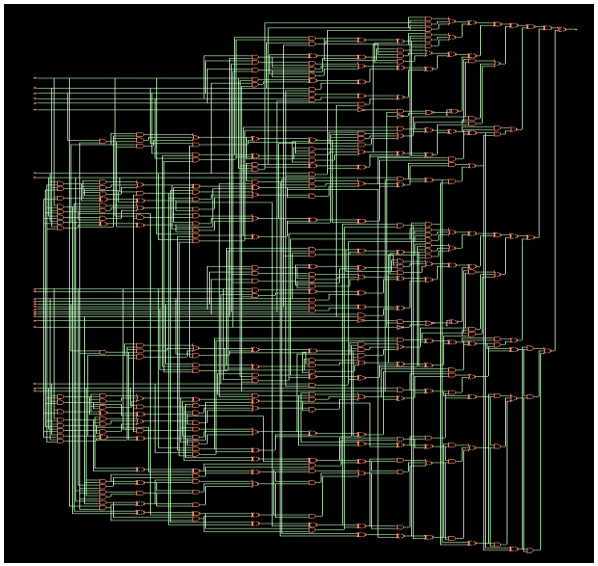
Invisible to customers!

Red: added part and
Green: revised part

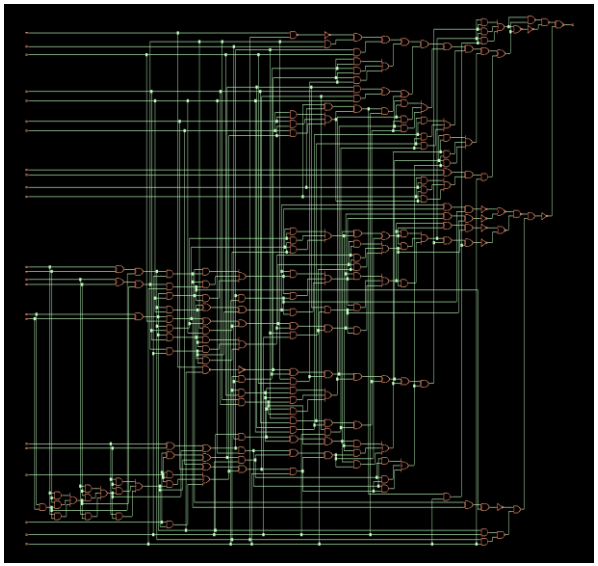


- *formal verification*
- *functional ECO*
- *logic rewiring*


Functional
ECO
Logic
Rewiring
Reverse
Engineering



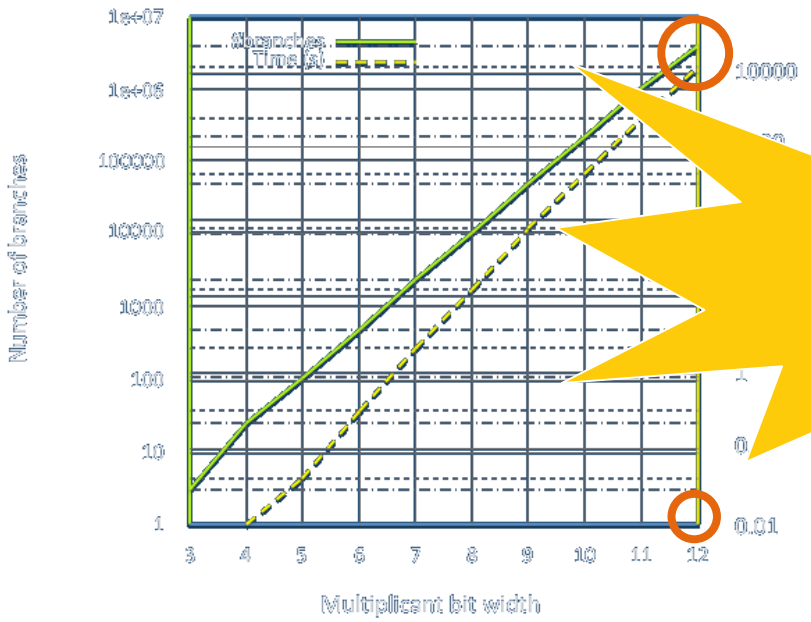
?



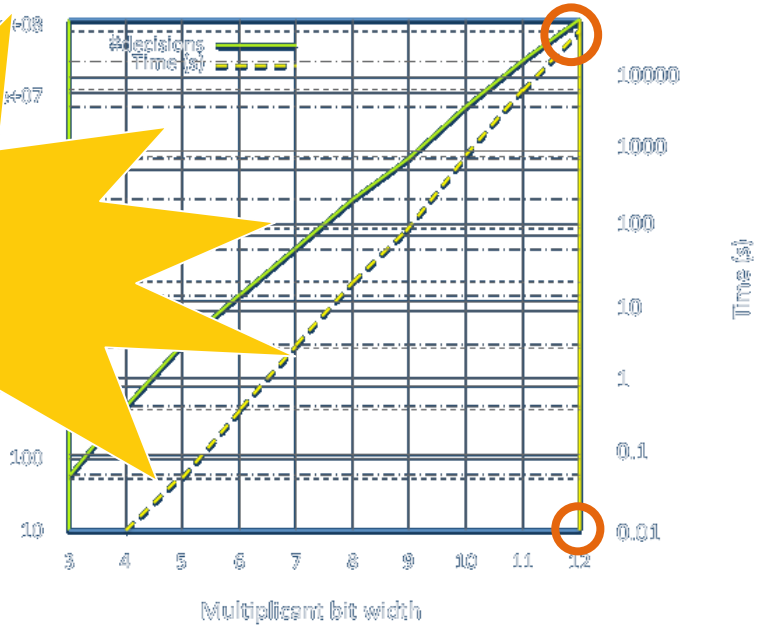
Use OBDD?
SAT?

Exponential

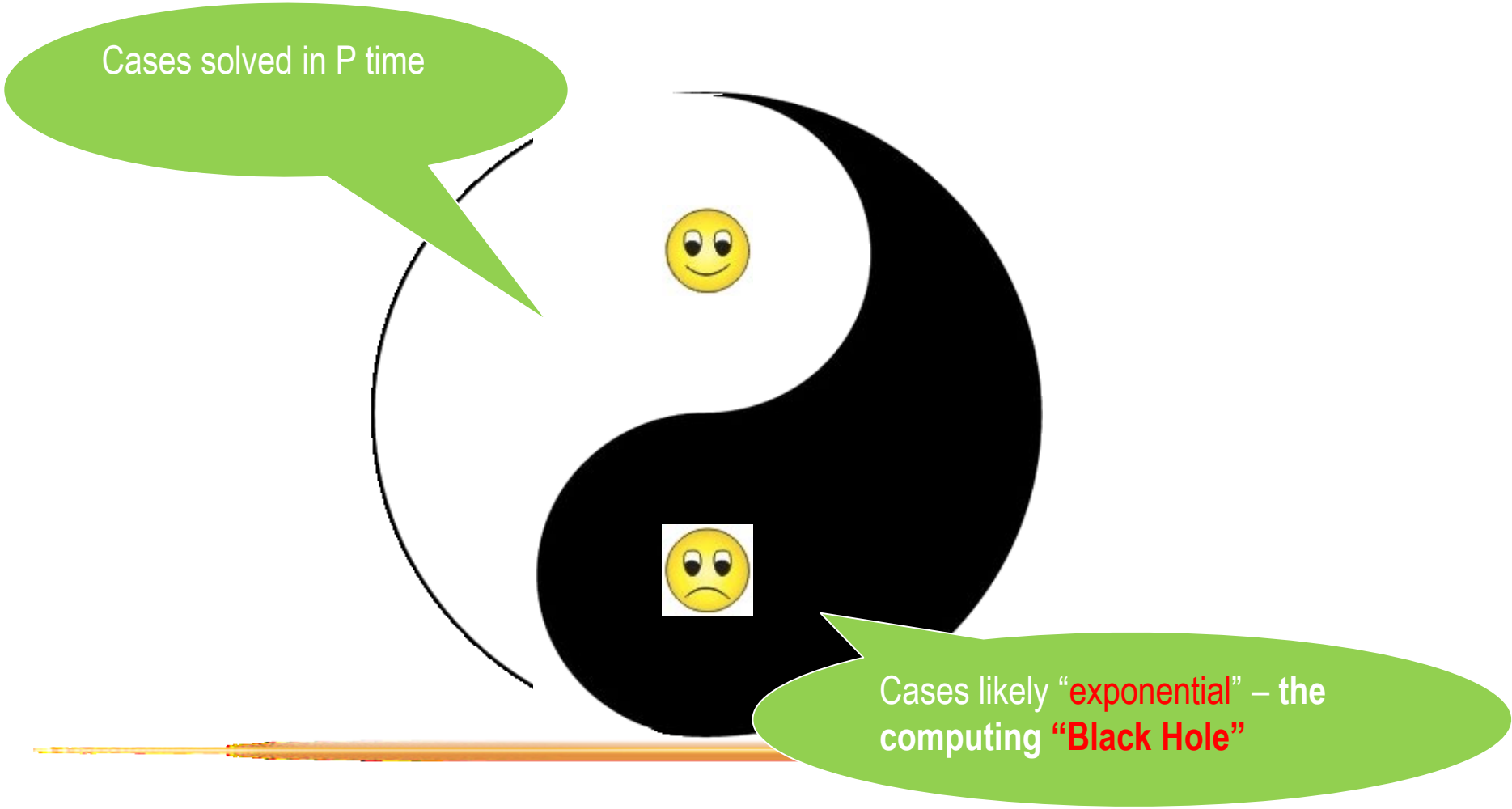
Solving time for a 64-bit multiplier?



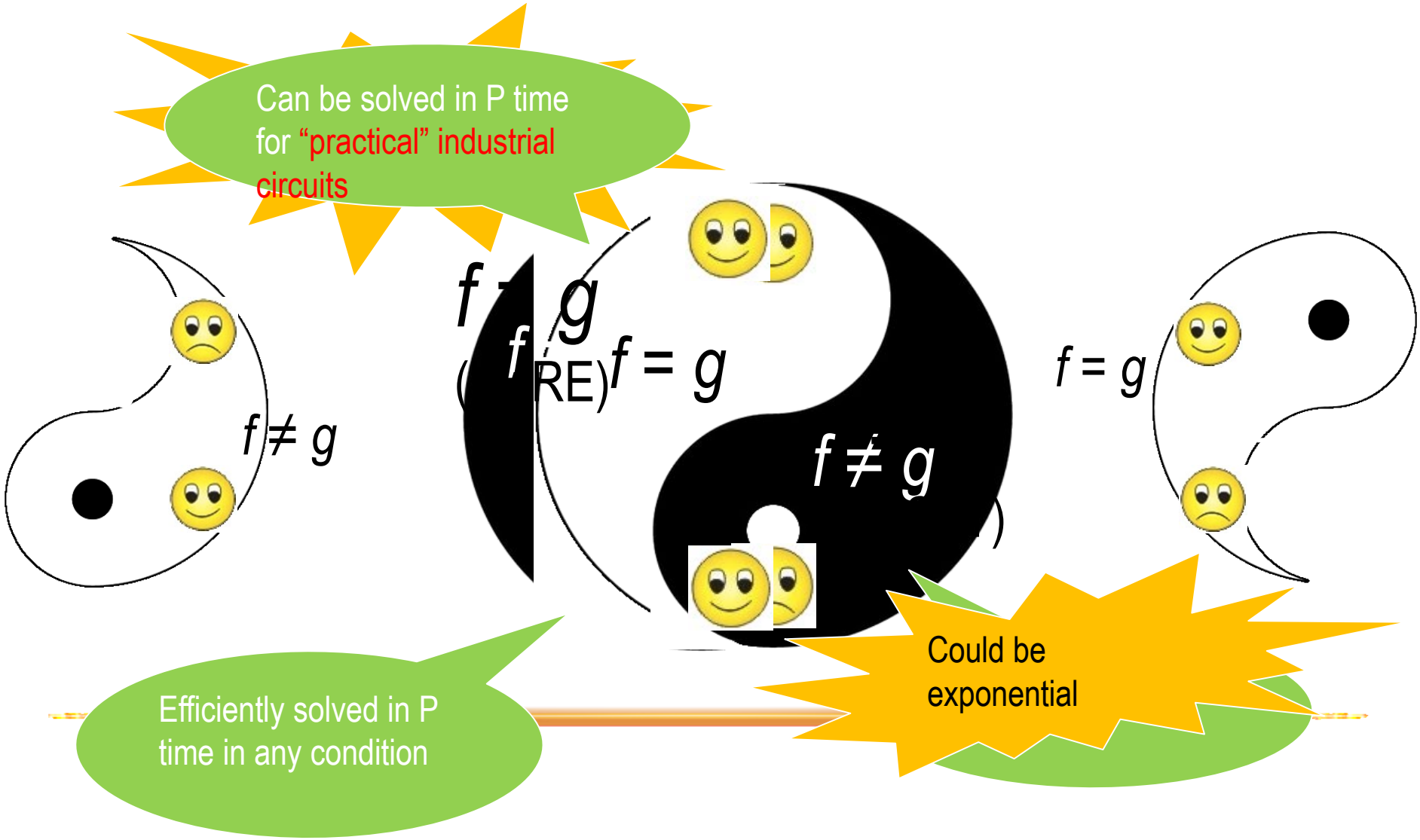
Over 10^{20} centuries!

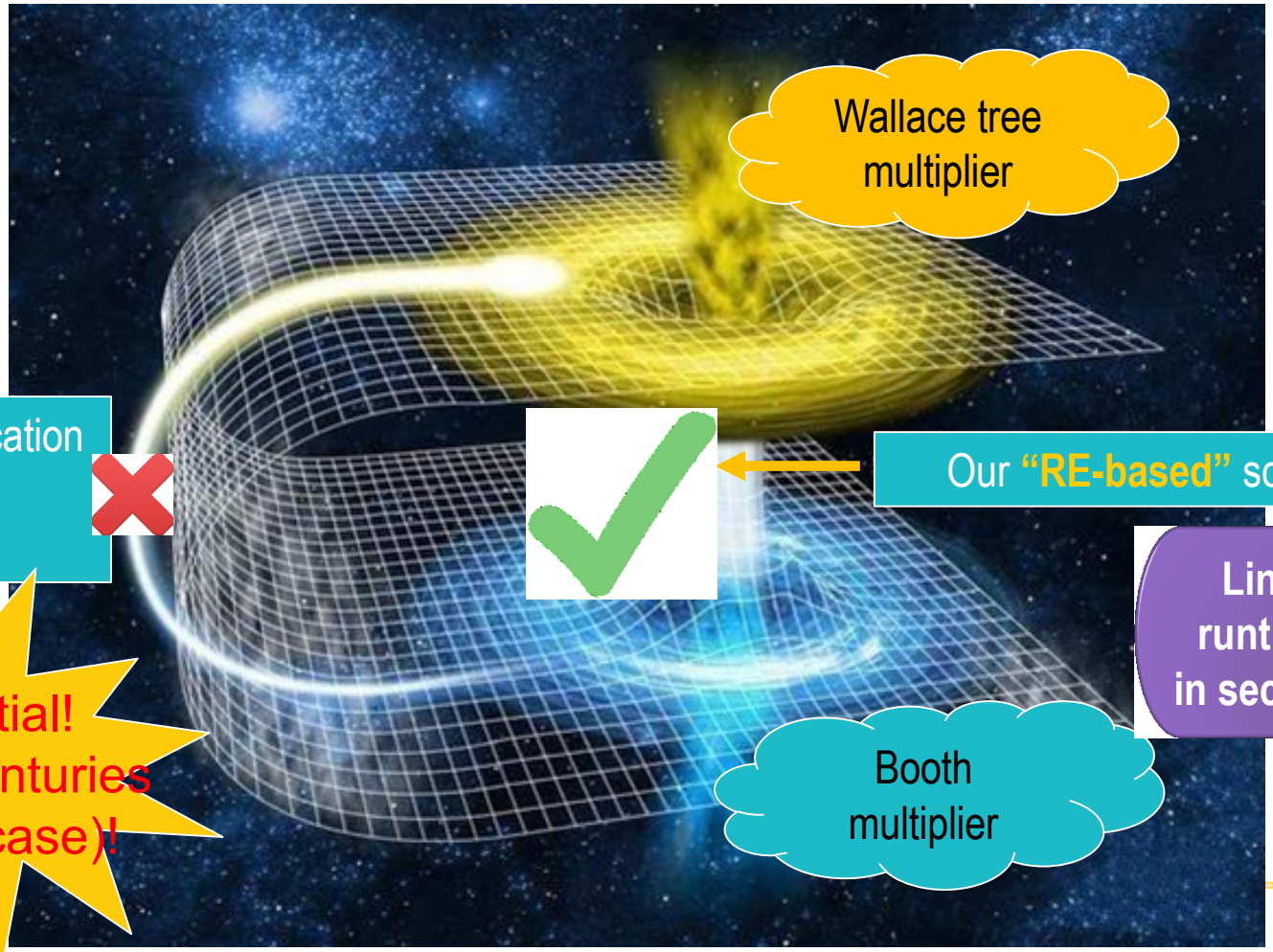


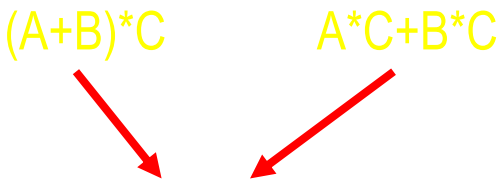
Black Hole

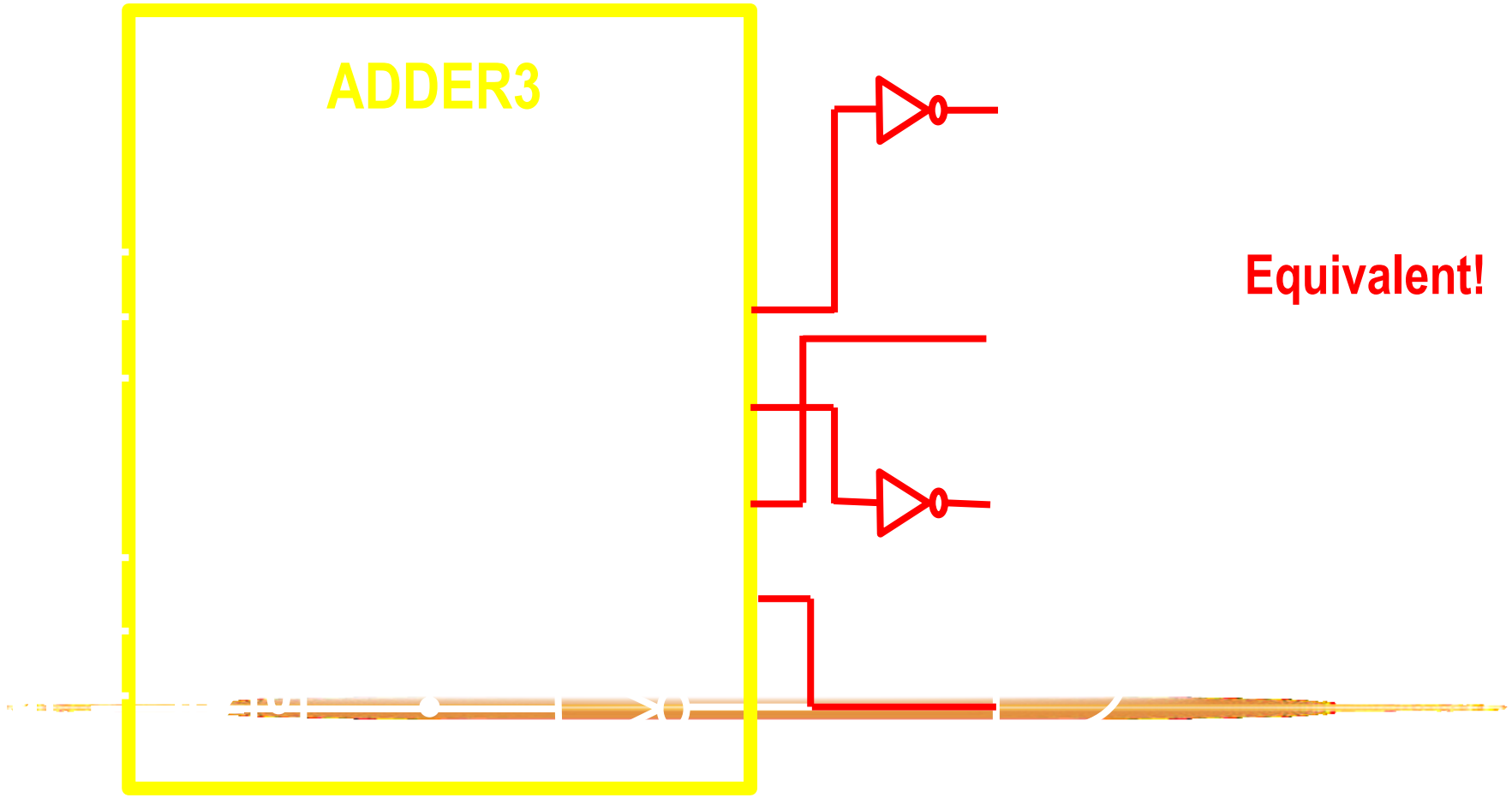

Cases solved in P time
Cases likely "exponential" – the computing "Black Hole"

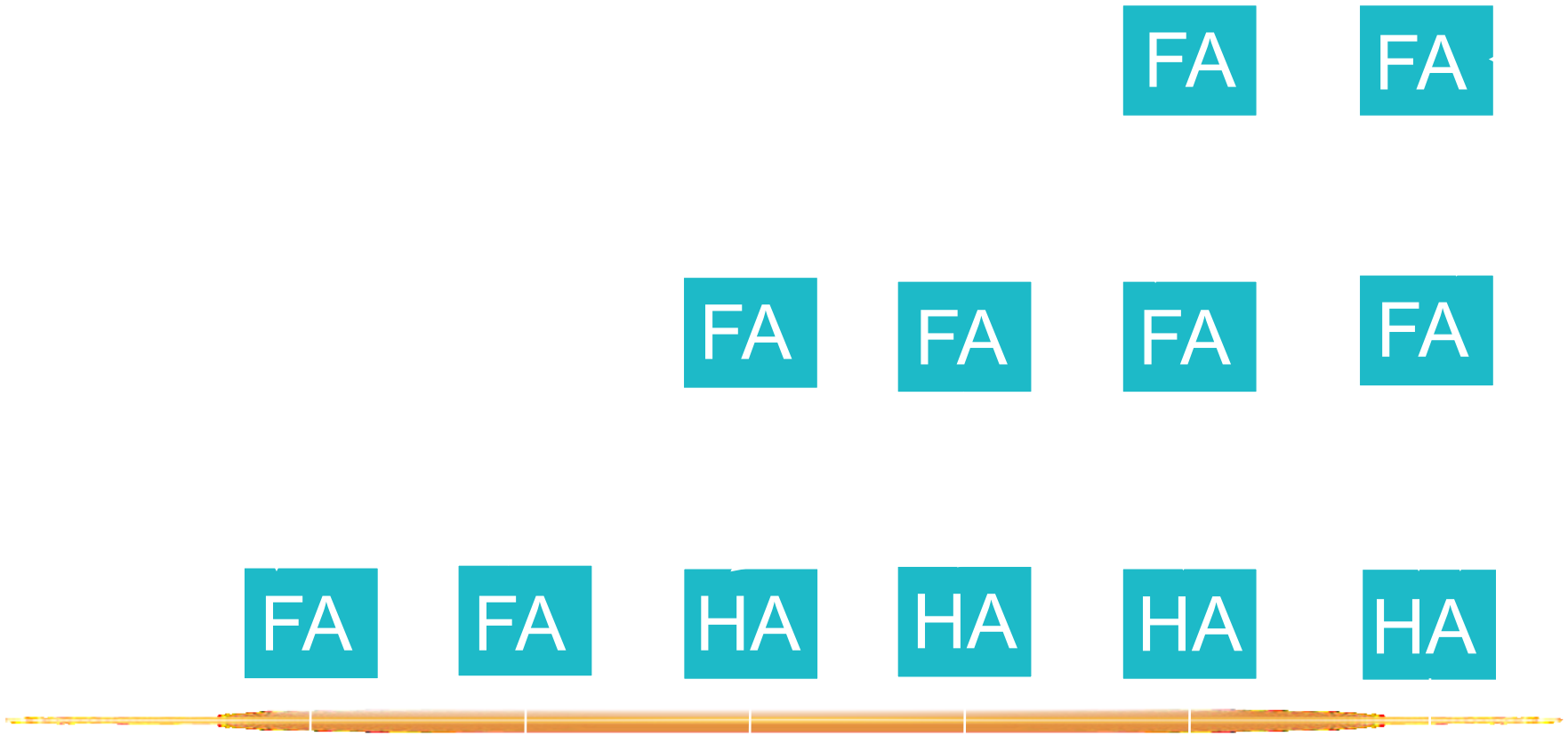
@

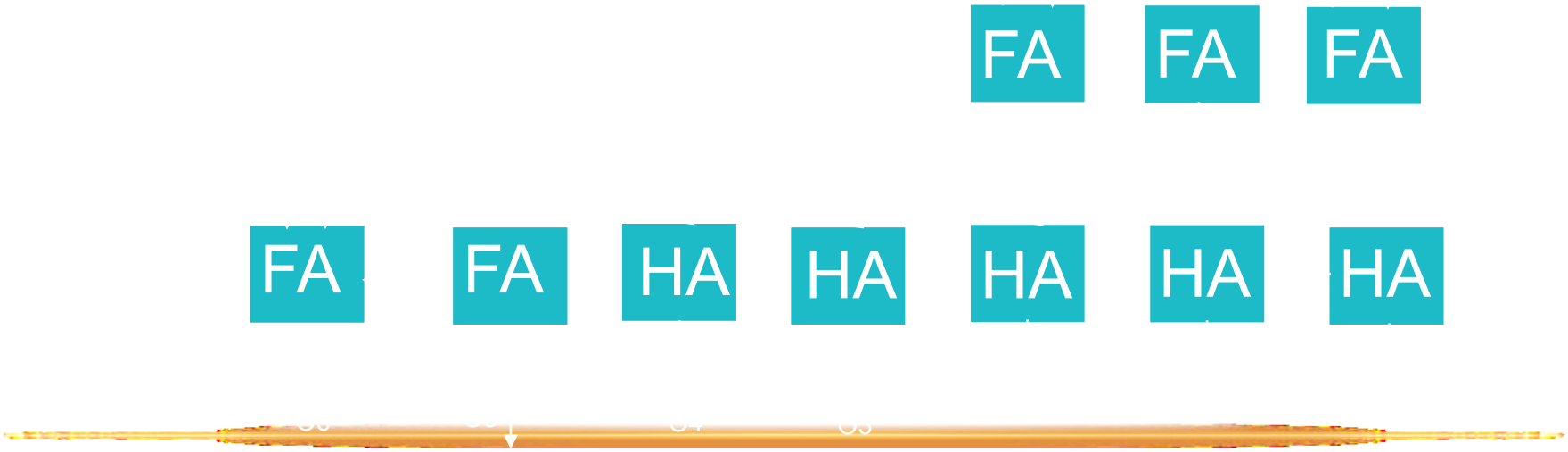

Can be solved in P time for “practical” industrial circuits
f ≠ g
f = g
f = g
f ≠ g
f = g
Efficiently solved in P time in any condition
Could be exponential


Wallace tree multiplier
Traditional verification flow: BDD, SAT
Our "RE-based" scheme
Linear runtime ! in seconds!
Exponential! Over 10^{10} centuries (for 32-bit case)!
Booth multiplier

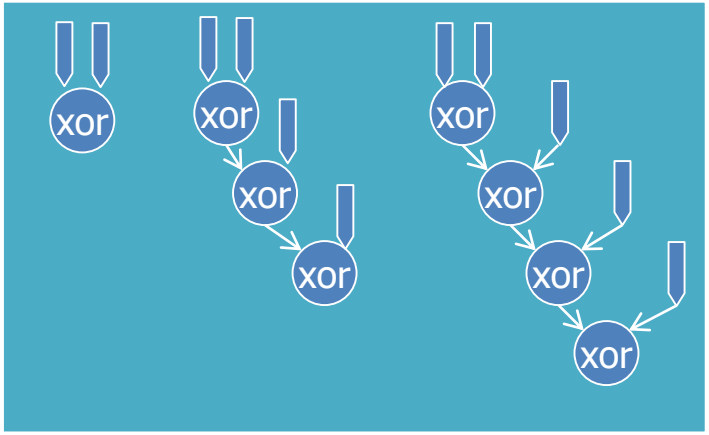

(A+B)*C
A*C+B*C

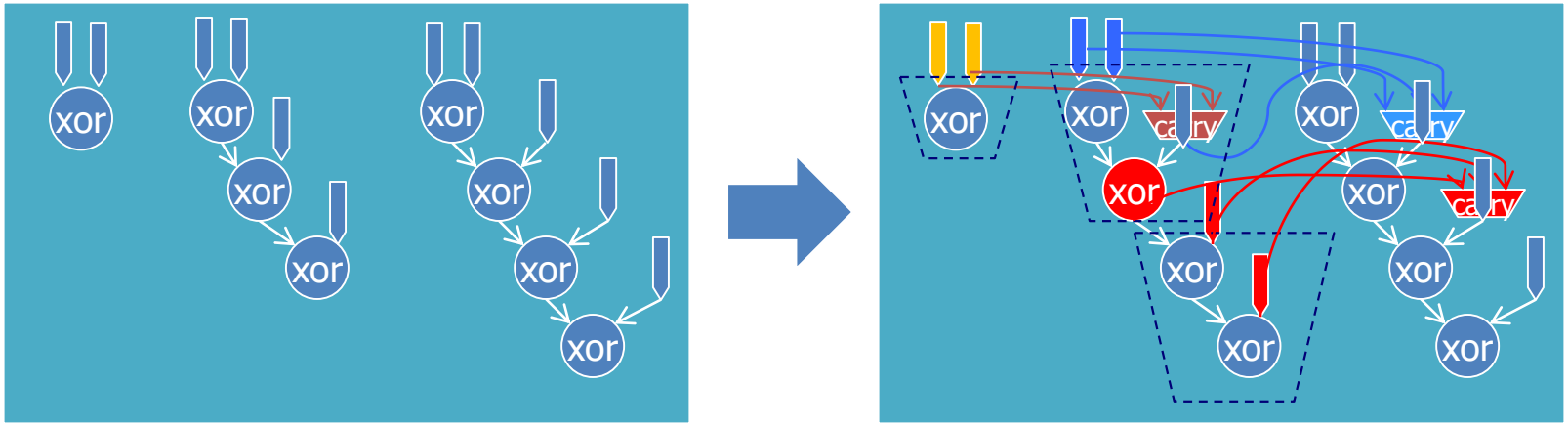

ADDER3
Equivalent!

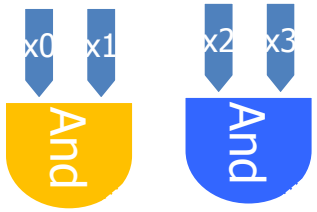

FA
FA
FA
FA
FA
FA
FA
FA
FA
HA
HA
HA
HA
HA

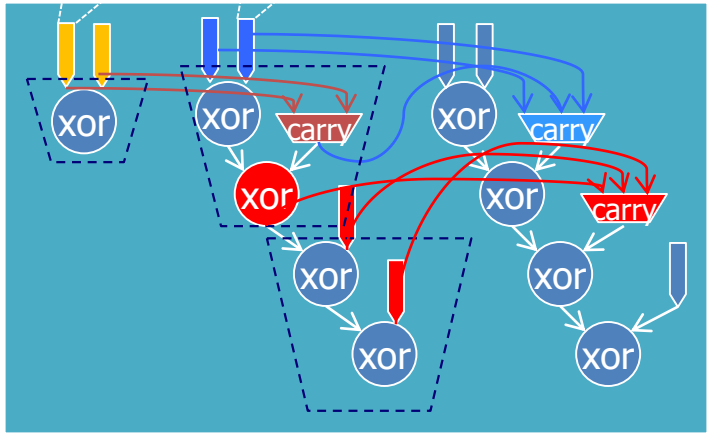

FA
FA
FA
FA
FA
HA
HA
HA
HA
HA

Global Circuit




xor
xor
xor
xor
xor
xor
xor
xor
xor
xor
carry
carry
carry
xor
xor
xor
xor
xor
xor

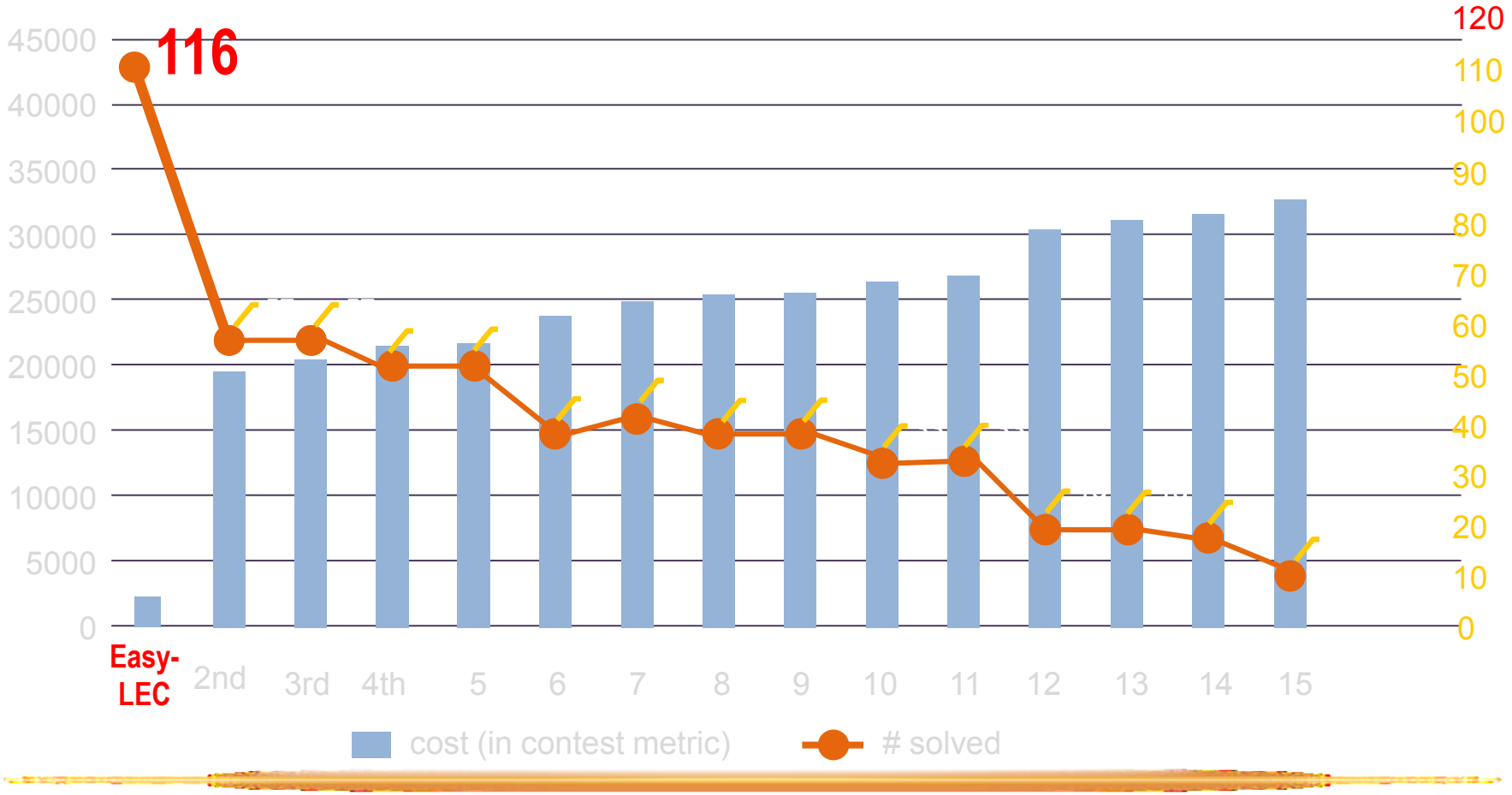

x0
x1
x2
x3
And
And

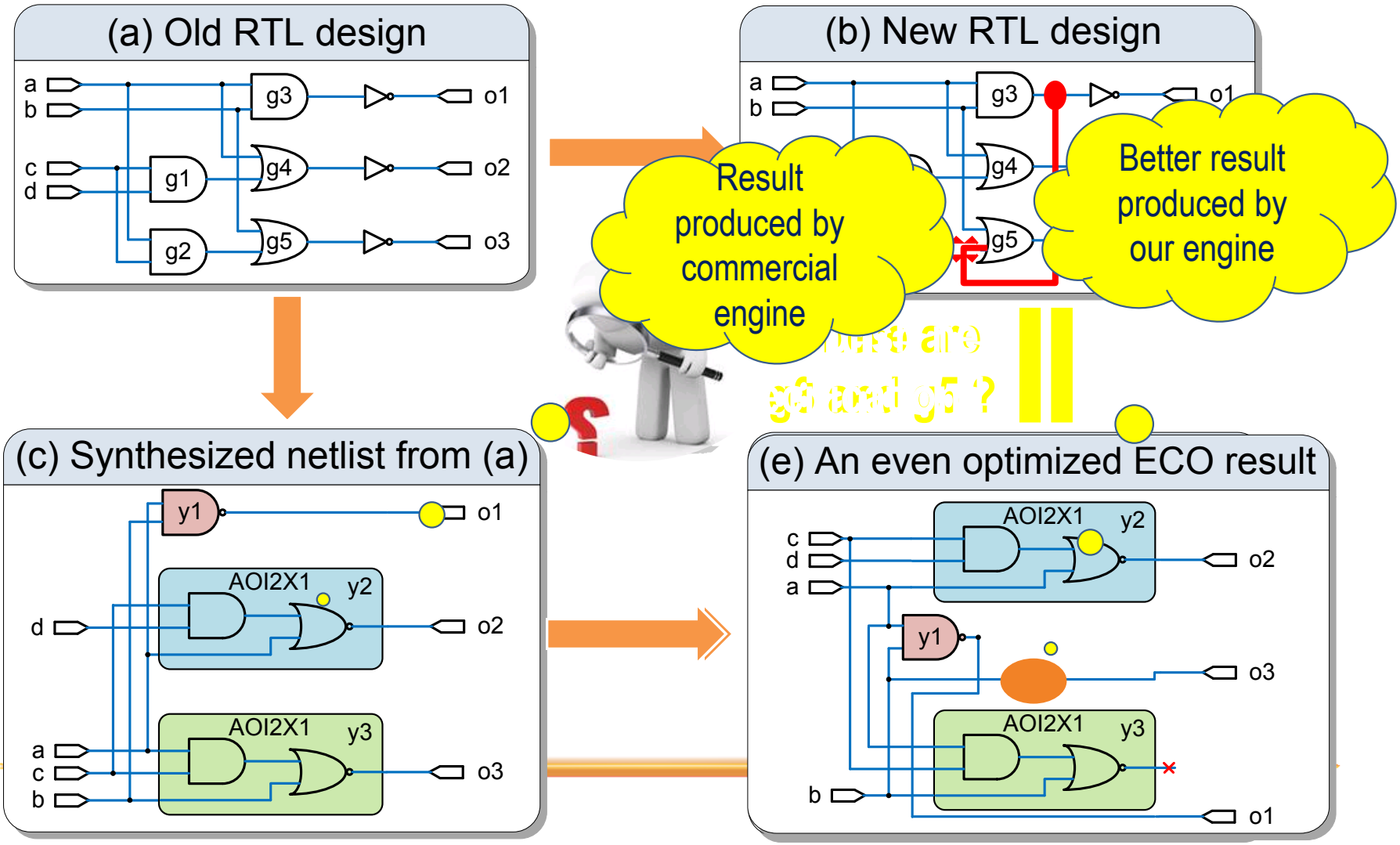

xor
xor
carry
xor
carry
xor
xor
carry
xor
xor
xor
xor

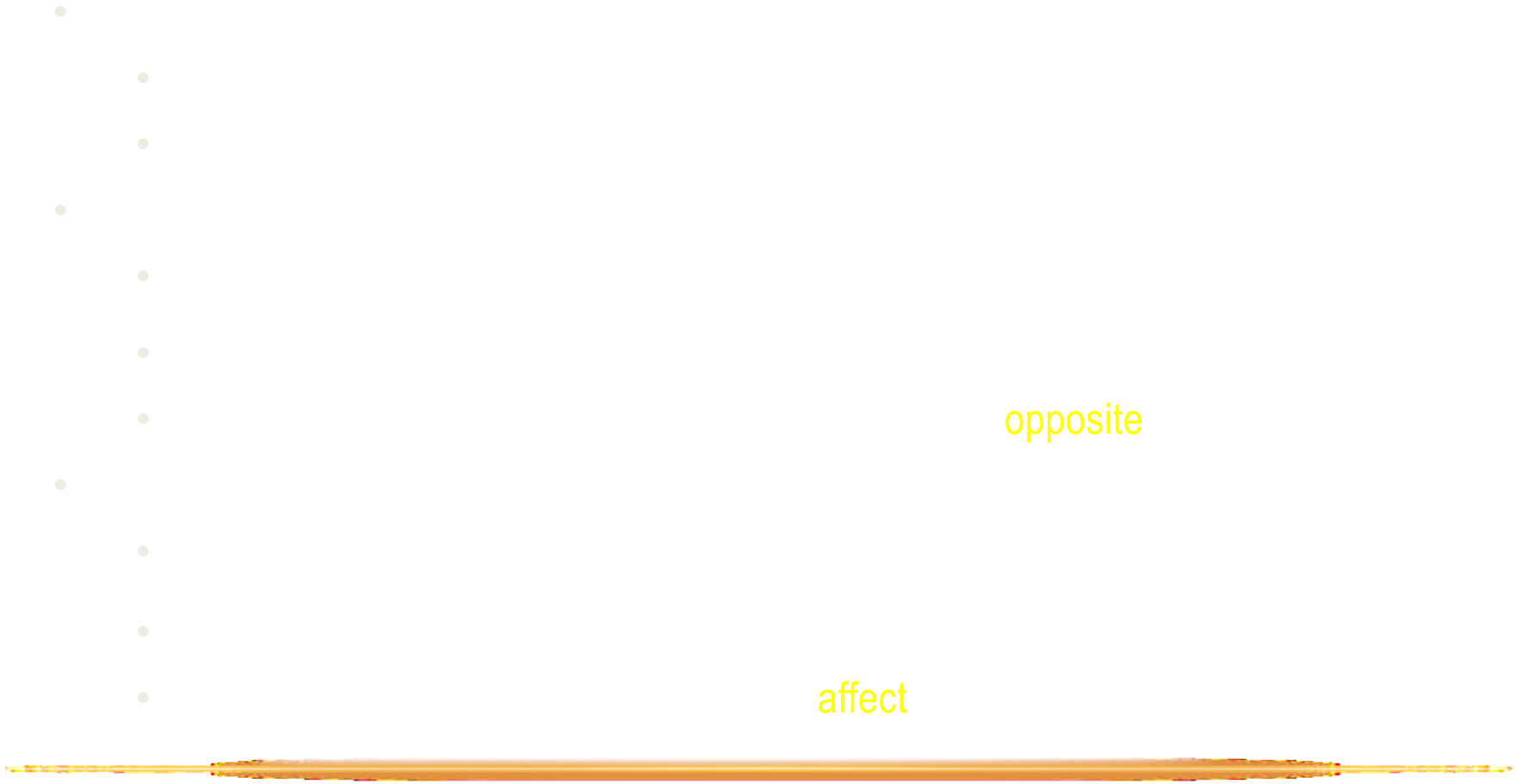
120

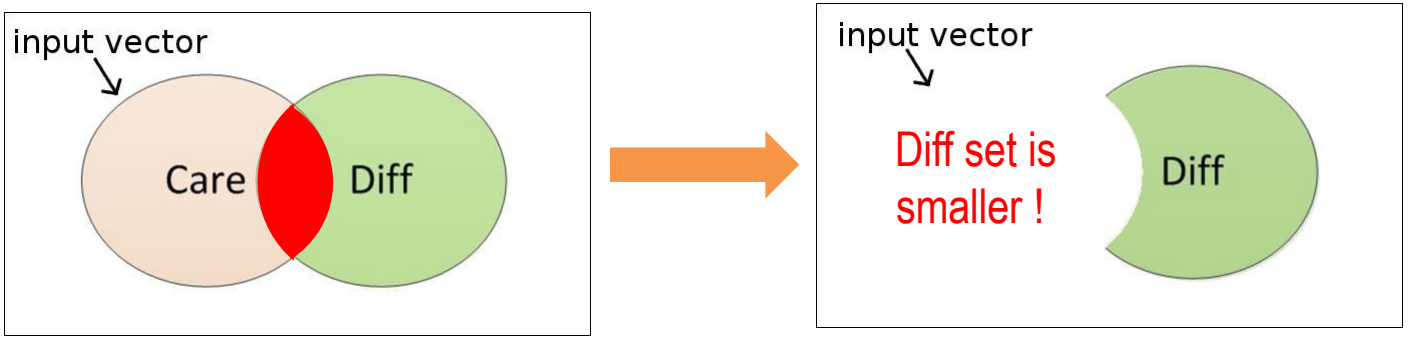
< 50% cases

black hole




(a) Old RTL design
a
b
c
d
g1
g2
g3
g4
g5
o1
o2
o3
(b) New RTL design
Result produced by commercial engine
Better result produced by our engine
(c) Synthesized netlist from (a)
y1
AOI2X1
y2
AOI2X1
y3
(e) An even optimized ECO result

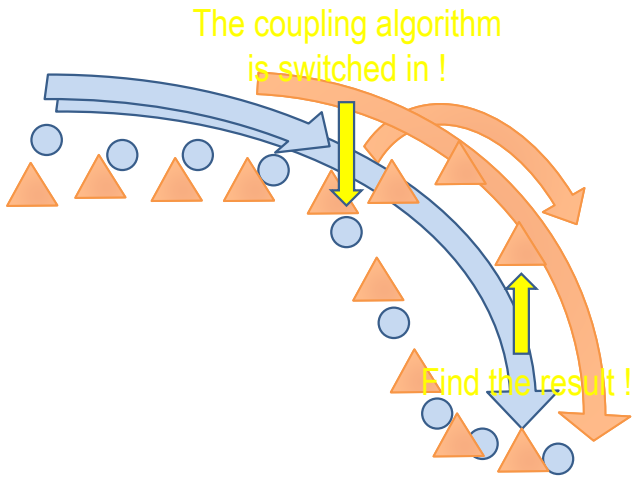

opposite
affect

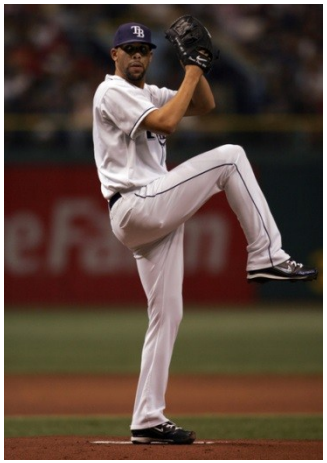

input vector
Care
Diff
input vector
Diff set is
smaller !
Diff

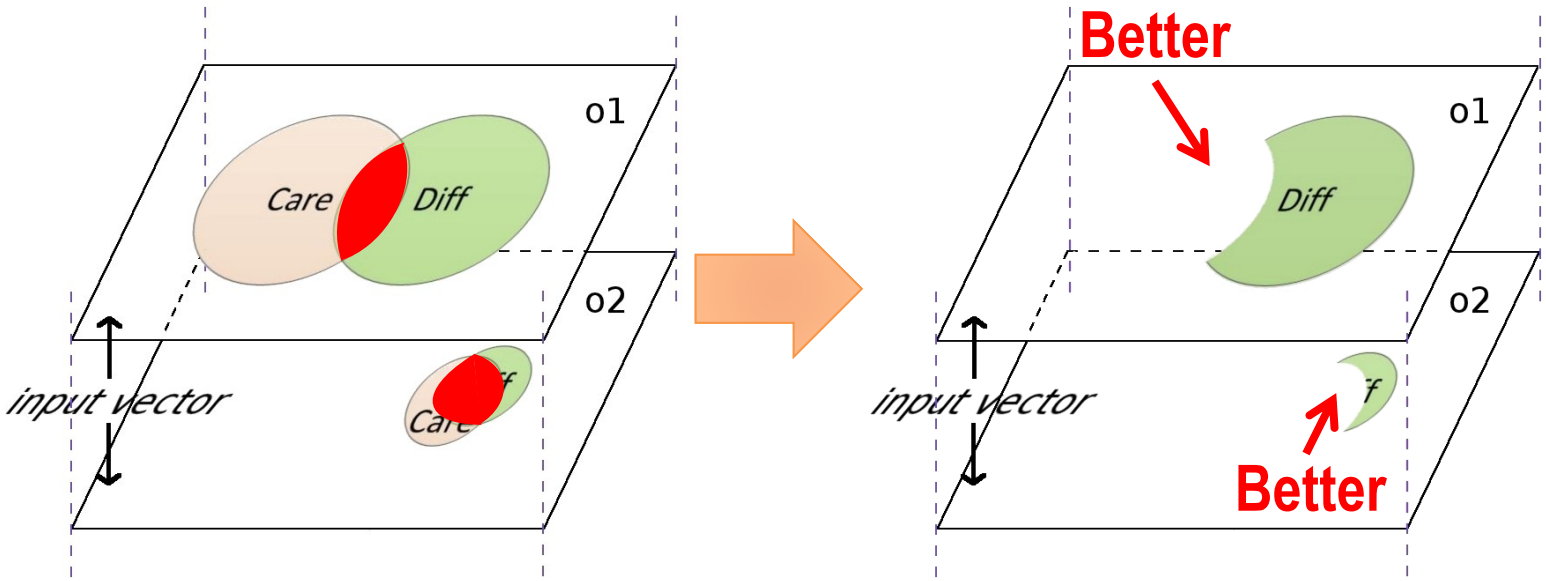
similar style

strategic contrast

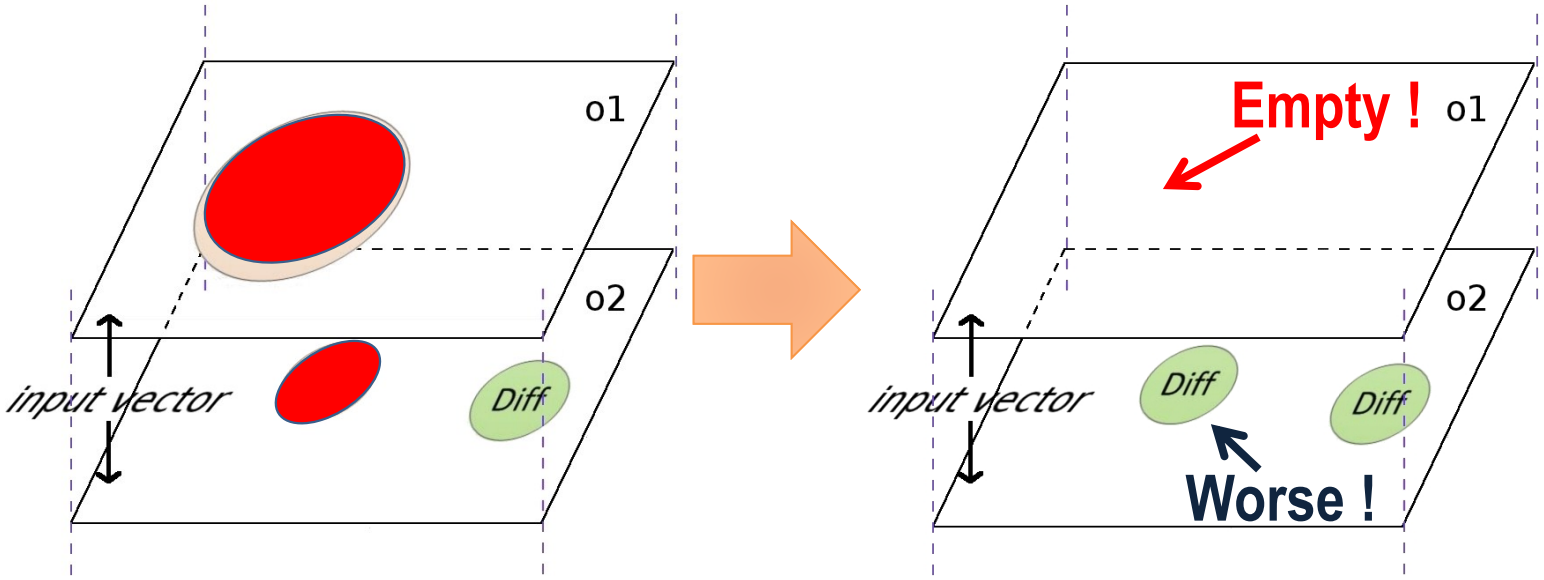
performance jump





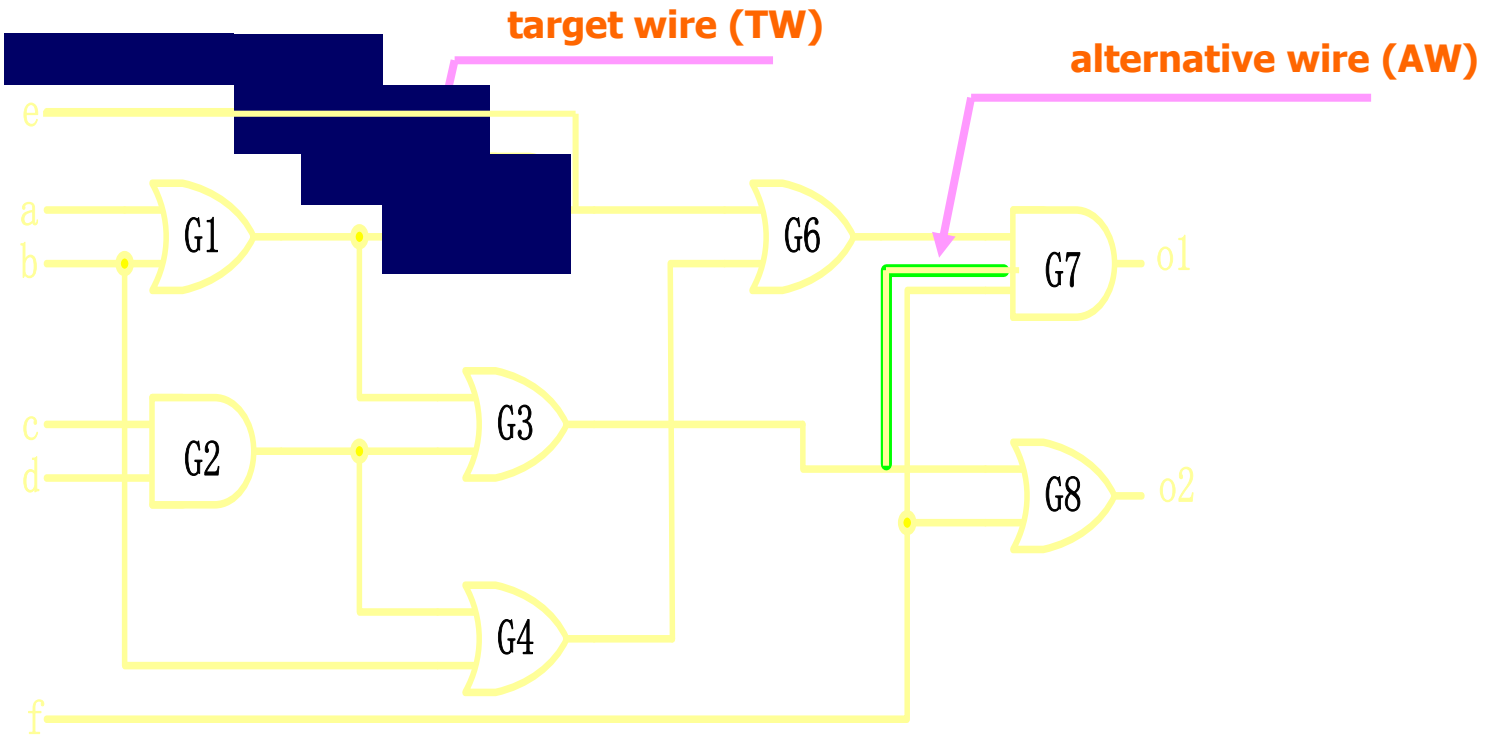

o1
Care
Diff
o2
input vector
Better
o1
Diff
o2
input vector
Better

- Input
-
- For do
  - If then
    -
  - Else
    -
  - End if
    -
    -
    -
- End for
- For do
  - If then
    -
    -
    - If then
      -
      -
    - End if
  - End if
- End for
-


o1
o2
input vector
Diff
Empty !
o1
o2
input vector
Diff
Diff
Worse !

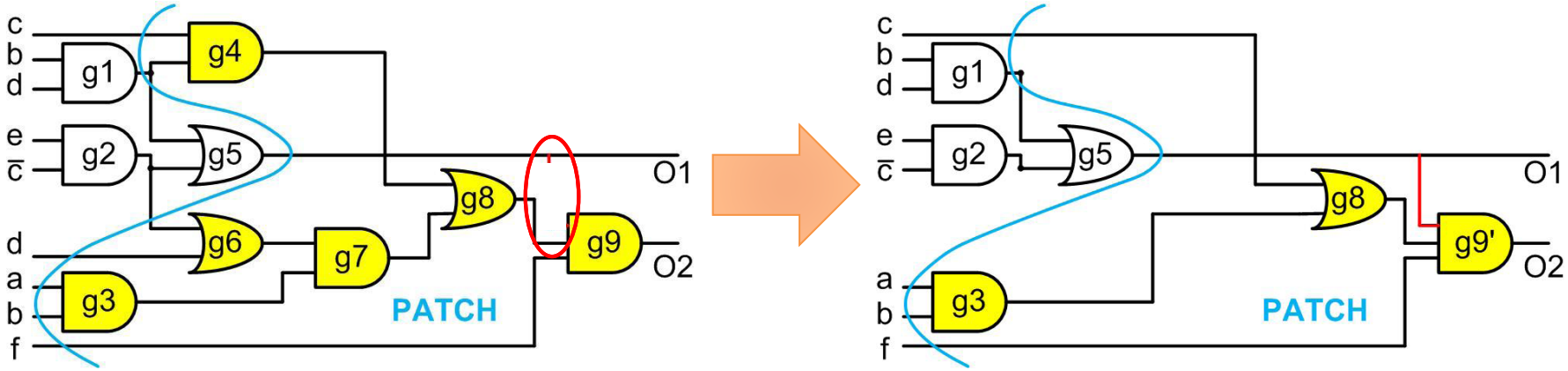
- Input
-
- For do
  - If then
    -
    -
    -
  - End if
- End for
- For do
  - If then
    -
    -
    - If then
      -
      -
    - End if
  - End if
- End for
-

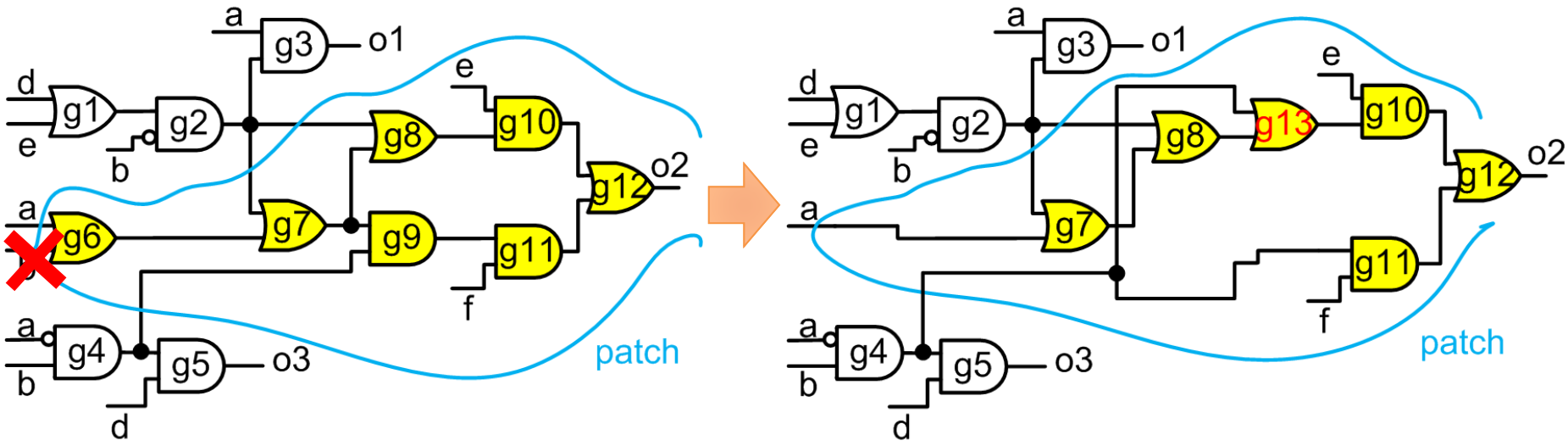
- Add
- Remove


target wire (TW)
alternative wire (AW)
e
a
b
c
d
f
G1
G2
G3
G4
G6
G7
G8
o1
o2

-
  -
-
-
  -

Logic Optimization and Equivalence Checking by Implication Analysis,


c
b
d
e
c̄
d
a
b
f
g1
g2
g3
g4
g5
g6
g7
g8
g9
g9'
O1
O2
PATCH



X. Yang, T.-K. Lam, and Y.-L. Wu, "ECR: A low complexity generalized error cancellation rewiring scheme," DAC2010

61% 14%

Case	Ours		ECO_{1st} at ICCAD2012	
	Patch size	CPU Time	Patch size	CPU Time
open01	0	0	0	0
open02	0	0	0	0
open03	1	18	0	10
open04	0	21	0	10
open05	0	1	0	65
open06	0	24	0	235
……	……	……	……	……
hidden17	54	27	111	383
hidden18	55	45	55	126
hidden19	65	48	FAIL	FAIL
hidden20	53	78	117	456
hidden21	73	146	86	498
hidden22	22	28	FAIL	FAIL
total	*757*	*957*	*1094*	*6597*
ratio1	***61%***	***14%***	***1***	***1***

Thank You!