A High Performance Reliable NoC Router

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Background

- highly integrated chips
- Reliability challenges on NoC

Purpose

- permanent faults on router components
- High reliability, high performance and low cost

Related Work

- BulletProof
  N-modular redundancy techniques
  heavy hardware overhead
- Vicis Router
  low area cost
  error detection & system recovery
- Pavan Poluri's design
  low cost correction circuitry
  poor performance under heavy network

Contribution

Fault tolerant strategies on 4 main pipeline units

- Double routing strategy for the RC failure
- Default winner strategy for the VA failure
- Runtime arbiter selection strategy for the SA failure
- Double bypass bus strategy for the crossbar failure

Contribution

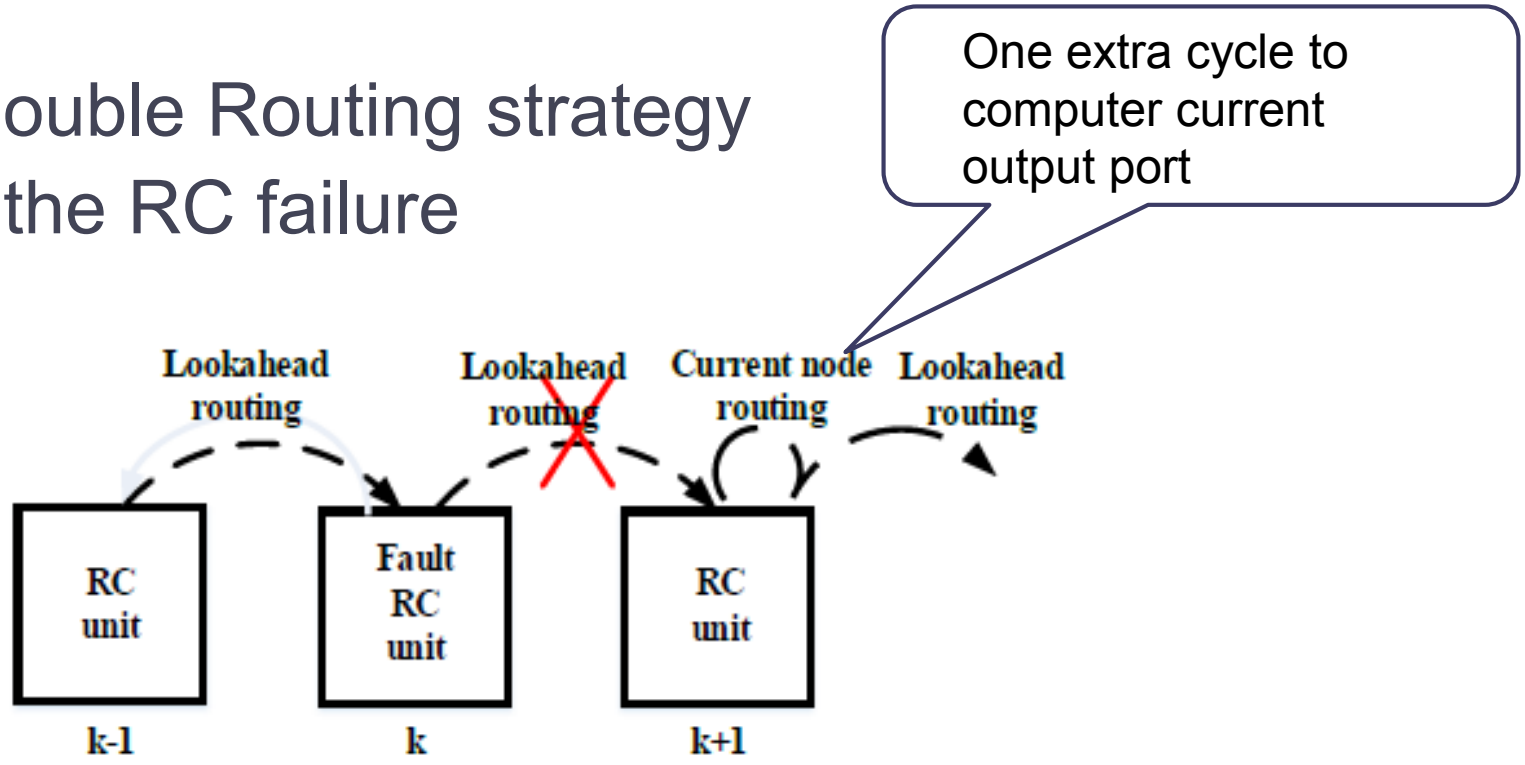
- Maintain performance in fault tolerance
- Pipeline optimization
- Routing algorithm

- Reliable NoC router
- High performance
- High reliability
- Low cost

Proposed Reliable NoC Router

Fault tolerant RC design

- Double Routing strategy for the RC failure



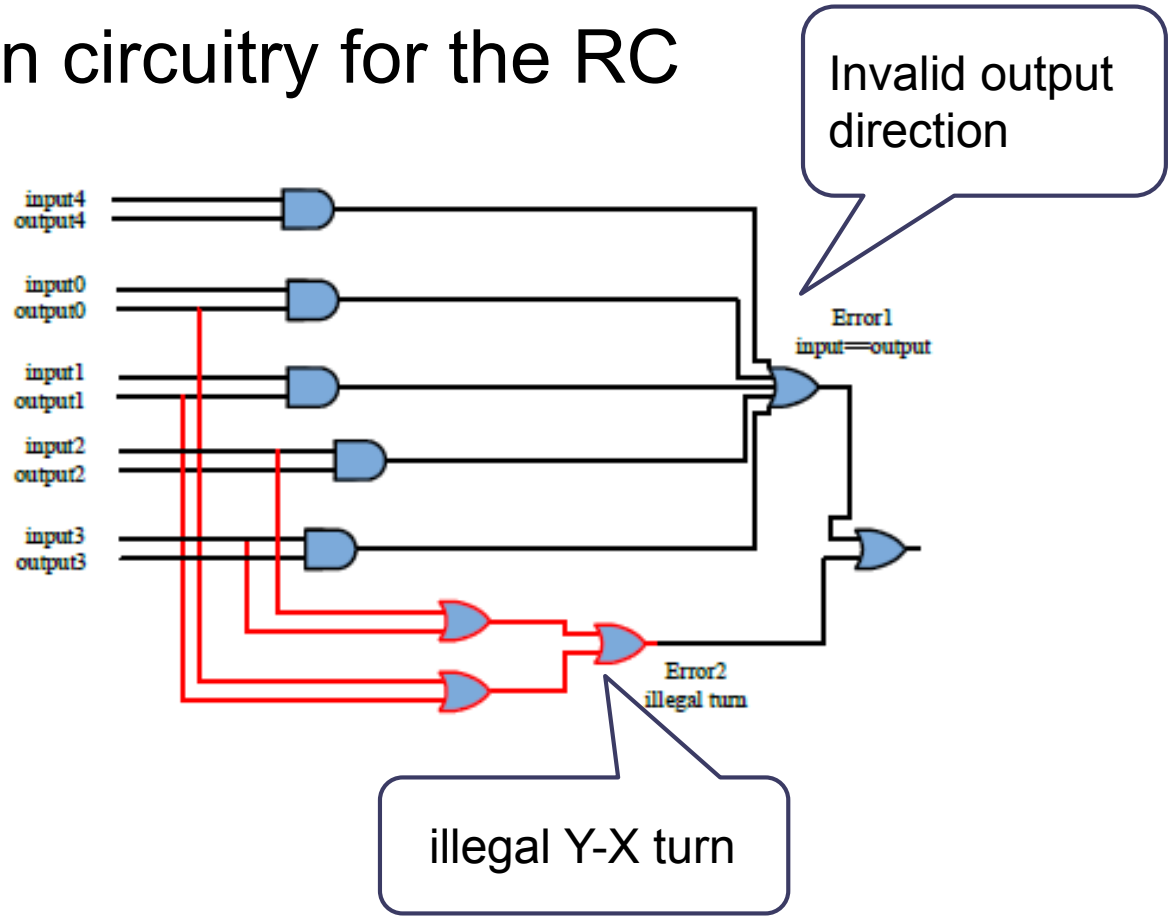
Proposed Reliable NoC Router

Fault tolerant RC design

- Fault detection circuitry for the RC

Key idea

Check functional rule



Proposed Reliable NoC Router

Fault tolerant VA design

VA fault scenario

first step: Input VC arbiter is faulty

→ Flit is blocked

need tolerate fault

second step: Output VC arbiter is faulty

→ Flits can be re-allocated to other VCs

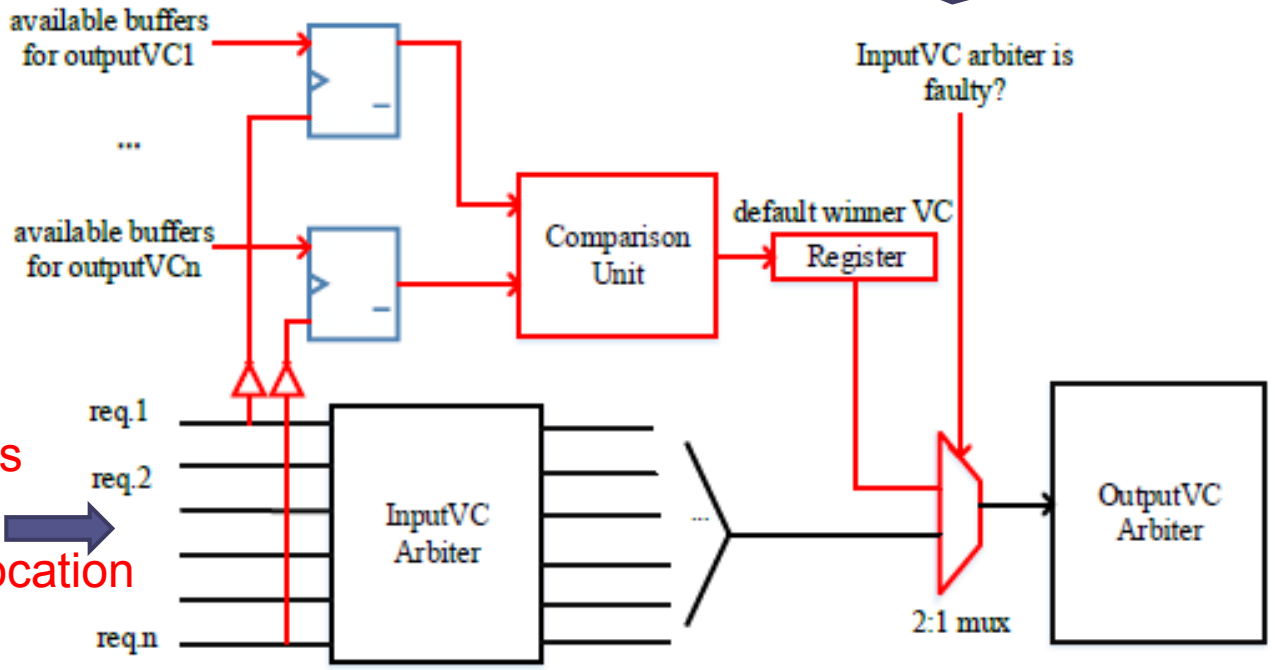
need avoid performance degradation

Proposed Reliable NoC Router

Fault tolerant VA design

- Default winner strategy

Red part acts as the second path to tolerate fault

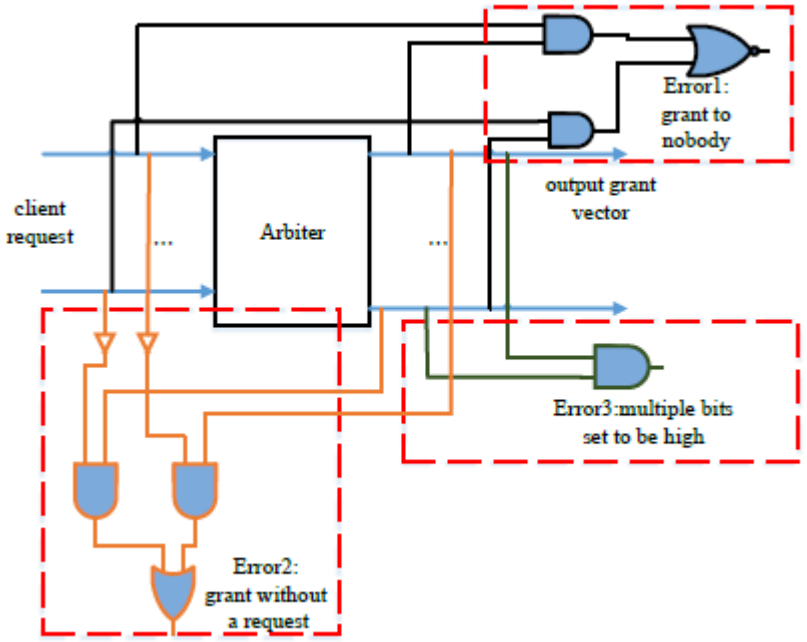


Add restrictions on VA requsts to avoid re-allocation

Proposed Reliable NoC Router

Fault tolerant VA design

- arbiter detection circuitry

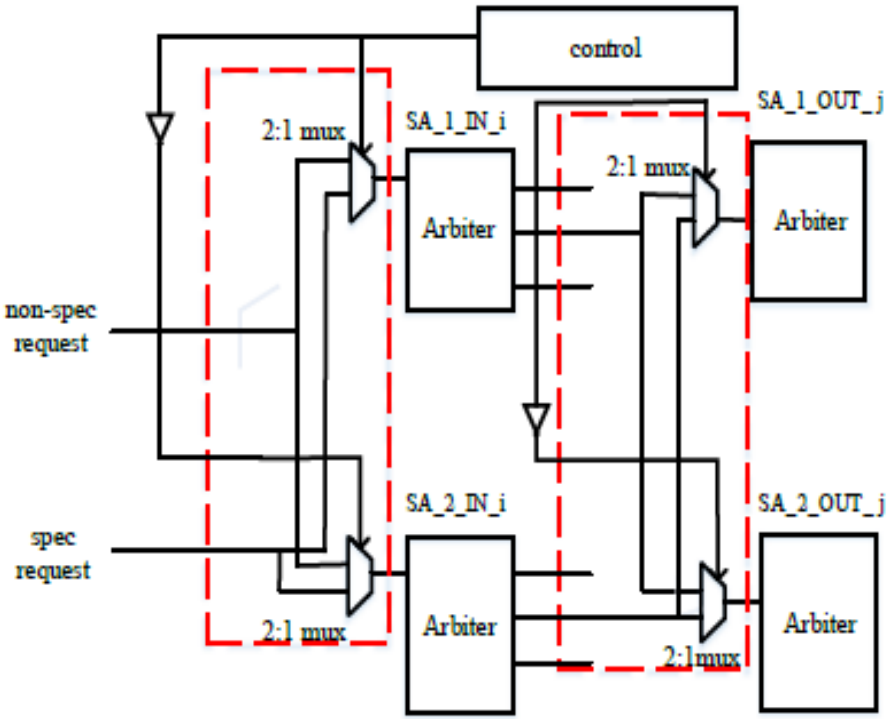


Proposed Reliable NoC Router

Fault tolerant SA design

hardware redundancy:two parallel switch allocators

- Runtime arbiter selection strategy



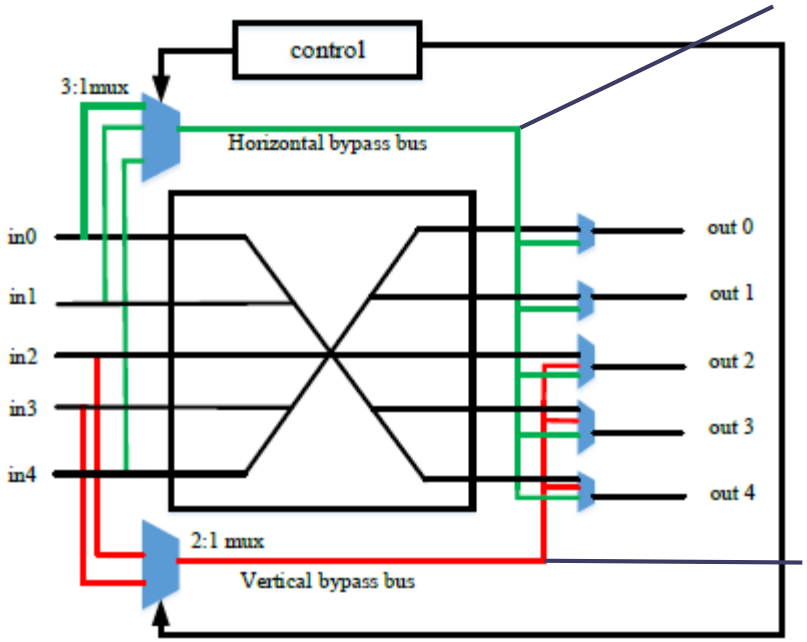
runtime select non-faulty arbiter to proceed non-speculative SA request

low cost
only several 2:1 mux

Proposed Reliable NoC Router

Fault tolerant crossbar design

- double bypass bus strategy

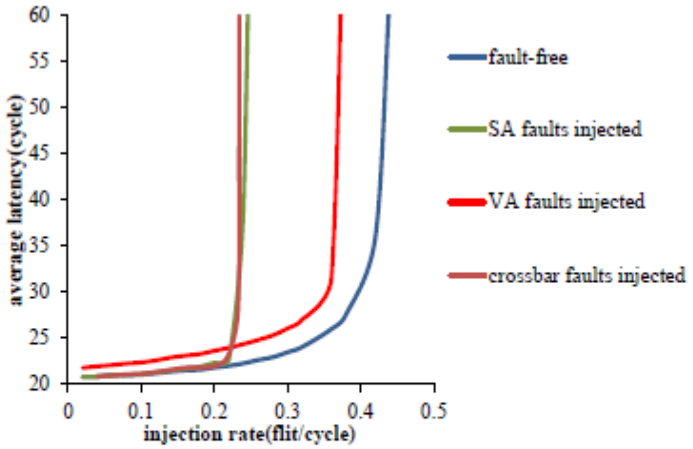


traverse flits from x-dimension or local router

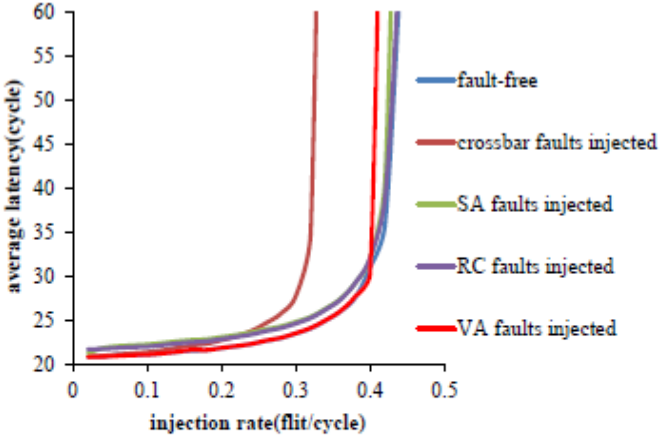
traverse flits from y-dimension

Performance Analysis

- Saturation throughput comparison



(a) Average latency in Poluri's proposed reliable NoC router

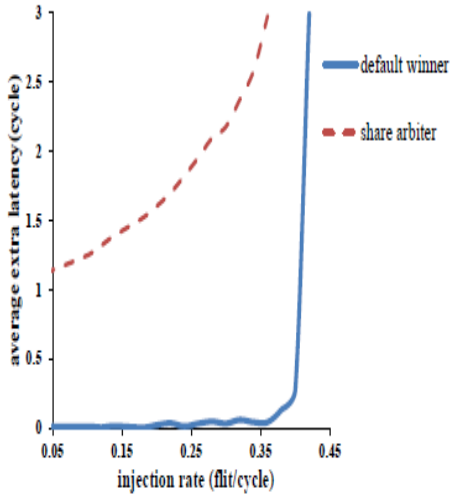


(b) Average latency in our proposed fault tolerant router

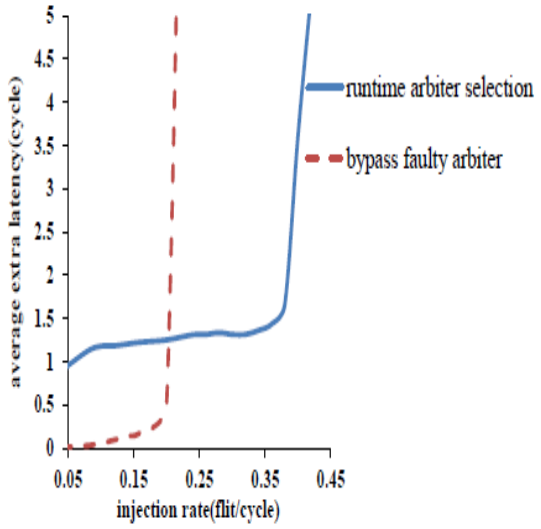
Performance Analysis

- Extra latency evaluation for different strategies

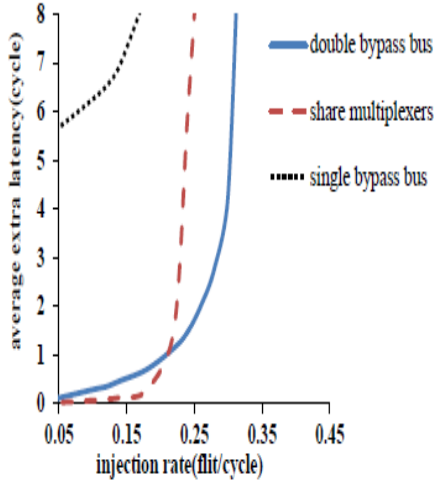
VA



SA

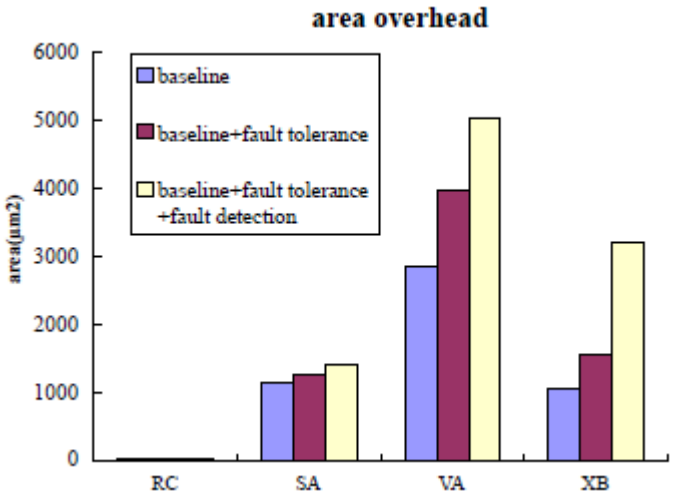


XB



Reliability Analysis

- Hardware consumption analysis



entire overhead: 9.8%

increase to 27% when in corporating the detection circuitry

Reliability Analysis

- Reliability comparison using SPF
- SPF

  faults to cause a failure /area overhead

Architecture	Area	Faults to cause failure	SPF
BulletProof	52%	3.15	2.07
Vicis	42%	9.3	6.55
Poluri's design	31%	15	11.4
Our reliable router	27%	21	16.5

Thank you!