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Flexible Transition Metal Dichalcogenide Field-Effect Transistors: A Circuit-Level Simulation Study of Delay and Power under Bending, Process Variation, and Scaling

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Introduction

- Flexible transistors are interested in some applications such as wearable technology and electronic paper.
- The TMD monolayer (MX_2) is an emerging nano-material, that consists of transition metal (M) and chalcogen atoms (X).
- TMDs have finite band gap by nature (e.g. 1.80 and 1.62 eV for MoS_2 and WSe_2, respectively.)
- Circuit level simulation is needed to evaluate the performance of TMDFETs.
- Existing simulations are limited to transistor level, expect for the work of [Chen, 2015] which is limited to 90nm and above.

TMDFET Modeling: Existing Work

- [Jimenez, 2012]: The first drift-diffusion compact model of long-channel devices.
- [Cao, 2014]: Another drift-diffusion-based compact model with slightly different expressions.
- [Chen, 2015]: First SPICE-compatible model with bending effect for 90-nm and above.

Our Contributions

- Modeling ballistic current and validating with numerical simulation data.
- Developing a compact model for TMDFETs in 16-nm technology node.
- Modeling the effect of bending.
- Studying the effects of process variation and circuit-level performance.
- Comparing the performance of TMDFET circuits with Si-based ones.

Modeling of TMDFET

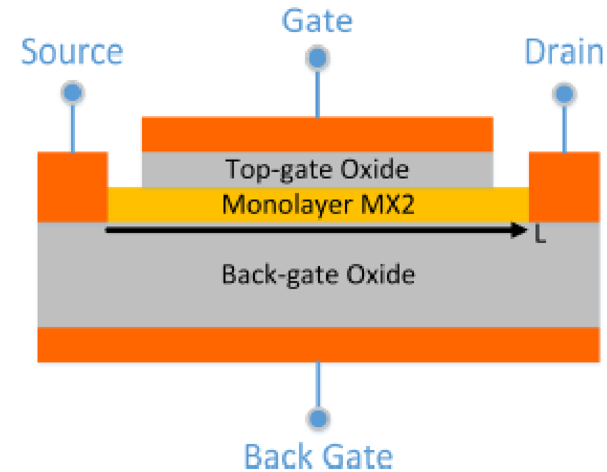
- In sub-20 nm, a ballistic transport model is more suitable. This can be described using Landauer-Buttiker formula.

$$I_D = \frac{q}{\hbar^2}\sqrt{\frac{m_y^* k_B T}{2\pi^3}} \int dE_{k_x} \left[F_{-1/2}\left(\frac{\mu_1 - E_{k_x}}{k_B T}\right) - F_{-1/2}\left(\frac{\mu_2 - E_{k_x}}{k_B T}\right) \right] T_{SD}(E_{k_x})$$

- It has no closed-form solution and must be integrated numerically.
- It is not SPICE-compatible.
- We deliver a new model that addresses these problems without directly using the ballistic transport model.

Device Under Study

- Device parameters:
  - W: channel width
  - L_{CH}: channel length
  - ε_{ch}: channel permittivity
  - T_{ch}: channel thickness
  - $\varepsilon_{tg(bg)}$ and $T_{tg(bg)}$: permittivity and thickness of top gate
  - $\varepsilon_{tg(bg)}$ and $T_{tg(bg)}$: permittivity and thickness of bottom gate



Short Channel Effect

- In short channel transistors the electric field along the channel can no longer be regarded as constant.
- The GCA (gradual channel approximation) start to deviate from reality.
- TMDFETs are less affected by SCE, because of:
  - thin-film channel
  - low dielectric constant
- At our target technology node of 16nm, the SCE is not too prominent.

Adaptation for Quasi-Ballisticity

- The mean free path λ of TMD monolayers is ~15 nm.
- The device is in quasi-ballistic region, since $L_{CH} \simeq \lambda$.
- Drift-diffusion current:

$$I_{D,sat} = WC_{ox}(V_G - V_t)v_{sat}$$

- Ballistic current approximation:

$$I_{D,bal} = WC_{ox}(V_G - V_t)v_{inj}$$

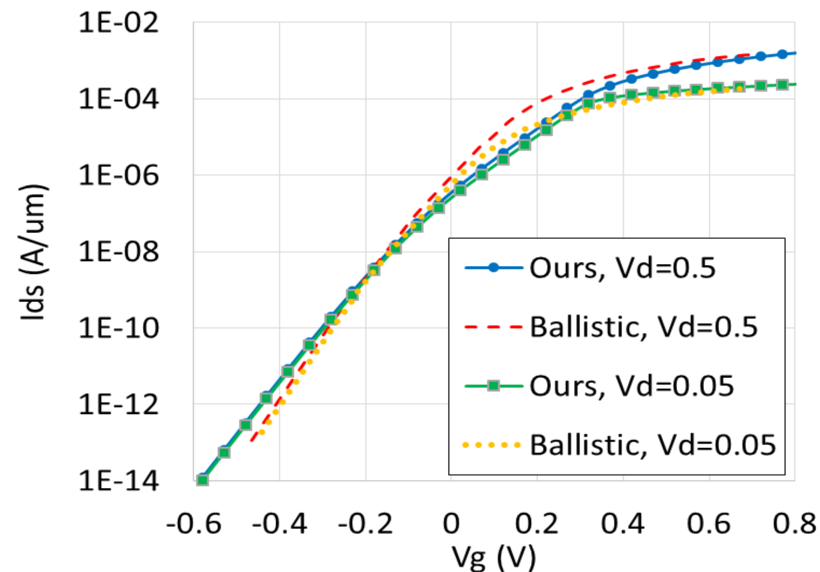
- The ballistic enhancement factor (BEF):

$$BEF = \frac{v_{inj}}{v_{sat}} = \frac{I_{D,bal}}{I_{D,sat}}$$

- The ballistic current can be approximated using drift-diffusion current.
- The accurate evaluation of the *BEF* requires sophisticated and time consuming numerical models.

BEF Approximation

- Constant BEF:
  - As a first order approximation, *BEF* can be estimated as a constant.
  - *BEF*≃2.5 is obtained by considering the whole device operating regions.



BEF Approximation

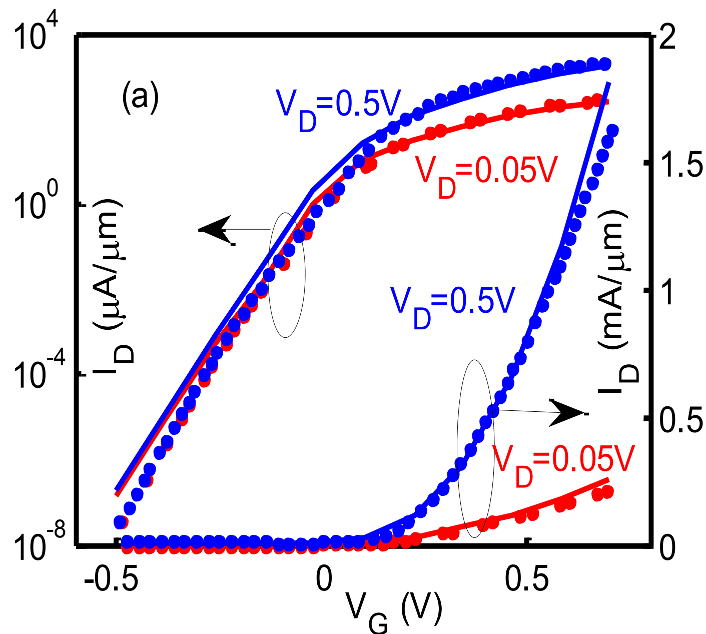
- Refined BEF:
  - The ratio between the ballistic current and drift-diffusion current varies in different regions depending on the bias voltages.
- We introduce a refined *BEF* that depends on the V_G and V_D voltages.

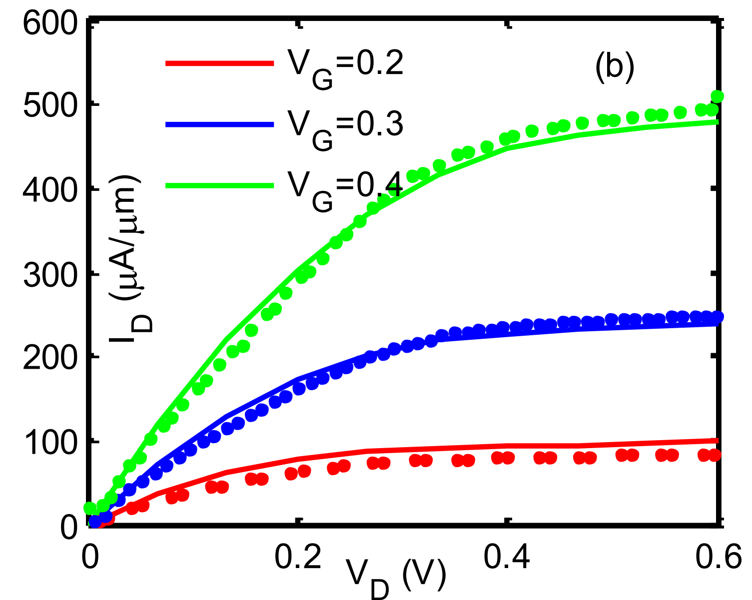
$$BEF = \gamma_1 V_G + \gamma_2 V_D$$

  - where $\gamma_1 = 0.36$ and $\gamma_2 = 0.04$ are obtained empirically.

Model Validation

- The result of I-V curve has good agreement with the numerical results.





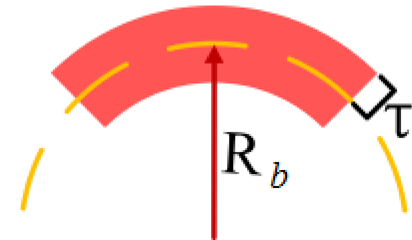
solid lines : Refined BEF model

dots: Numerical results in [Yoon, 2011].

Modeling Flexibility

- Bending is defined in terms of the applied strain ϵ

$$\epsilon = \frac{\tau}{R_b}$$



  - R_b: bending radius
  - τ: half film thickness
- The band gap of TMD monolayers has a linearly decreasing relationship with respect to ϵ.
- Bandgap under applied strain

$$E_g = E_{g0} - c\epsilon$$

  - c is a material depending coefficient

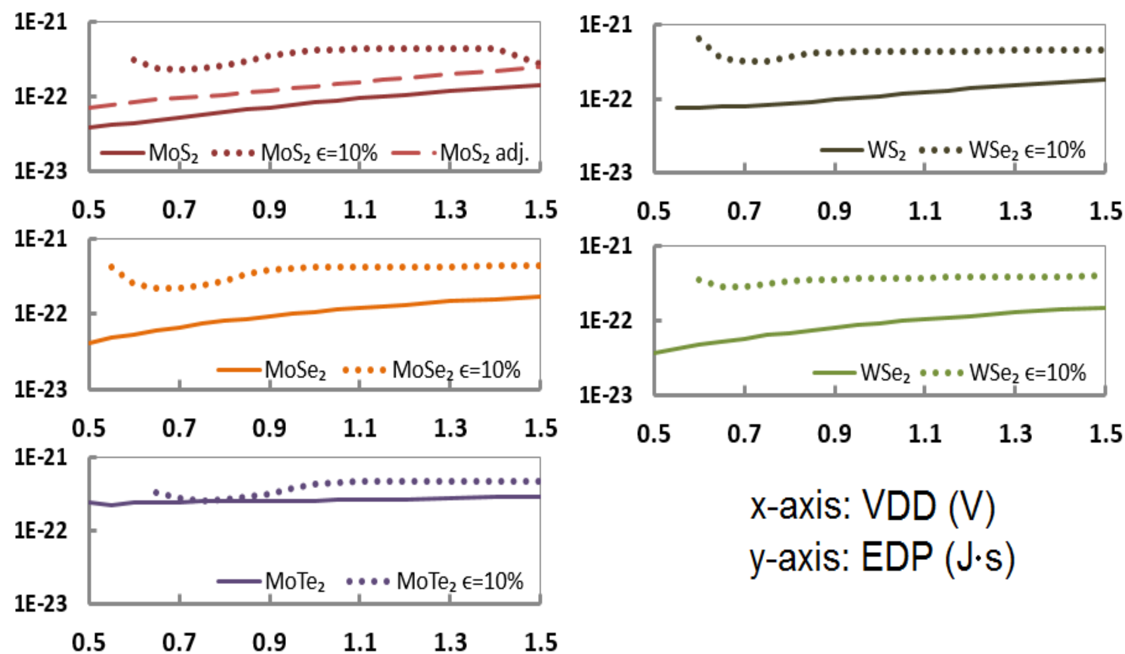
MX_2	E_{g0}	c
MoS_2	1.80 eV	0.1046
$MoSe_2$	1.51 eV	0.06958
$MoTe_2$	1.10 eV	0.04006
WS_2	1.93 eV	0.1078
WSe_2	1.62 eV	0.06778

Experimental Results

- We performed various circuit-level simulations to evaluate TMDFET circuits' performance.
- The default transistor parameters:
  - W = 32 nm
  - L_{CH} = 16 nm
  - T_{ox} = 2.8 nm
  - Gate oxide is HfO_2.

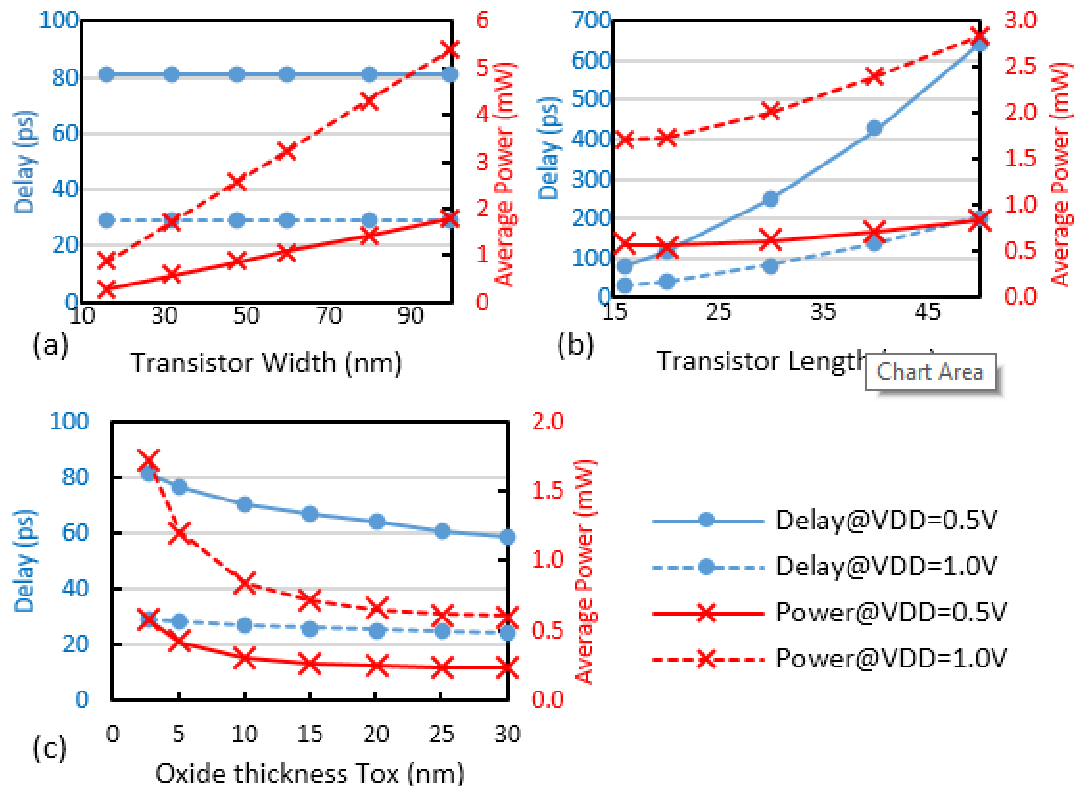
Supply Voltage Exploration

- The supply voltage V_{DD} is swept from 0.5 V to 1.5 V
- EDP of unstrained TMDFETs mostly increases with V_{DD}
- TMDFETs with $\epsilon = 10\%$ have a minimum EDP between V_{DD} = 0.65 to 0.75 V



Variation in Design Parameters

- W, L_{CH}, and T_{ox} are varied by 10%.
- Results show that
  - Variation in L_{CH} results in the most change in delay.
  - Variation in W and T_{ox} results in more change in power.

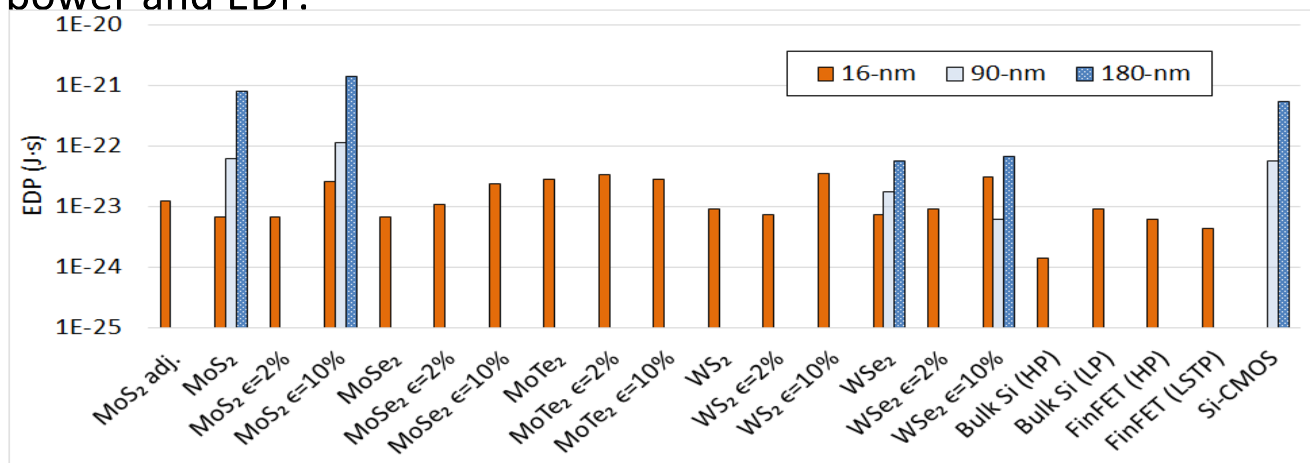


Cross-Technology Comparison

- Basic logic gates (*inv*, *nand*2, *nor*2, *nand*3, *nor*3, *nand*4, *xor*2), a 7-stage fanout-of-4 buffer chain, and *c*17 circuits are simulated.
- Technologies:
  - TMDFET
  - High-performance (HP) bulk-Si
  - Low-power (LP) bulk-Si
  - High-performance (HP) Si-based FinFET
  - Low-standby-power (LSTP) Si-based FinFET

Results

- Bending causes the band gap to decrease, resulting in
  - Delay and I_{on}/I_{off} ratio to decrease.
  - Power and EDP to increase.
- On the 180-nm and 90-nm technology nodes, WSe_2 FET's EDP is only 12.7% and 40.7% of that of Si-based transistors.
- TMDFETs have higher EDP compared to Si-based transistors (at least 4.7×) on the 16-nm technology node.
  - The delay of MoS_2FET is 34.2% higher and power is 1.71×.
- Flexible TMDFETs can be tuned by bending to achieve a lower delay at the cost of higher power and EDP.



Conclusion

- We presented a parameterized, SPICE-compatible compact model of TMDFETs 16-nm technology node.
- We performed extensive SPICE simulations on the circuit-level.
- We also investigated the effects from bending.
  - bending results in lower delay at the cost of higher power and the risk of poor transistor operation.
- Our SPICE model will be made open-source at nanoHub.

Thanks

Any question?