Efficient Circuit Failure Probability Calculation along Product Lifetime Considering Device Aging

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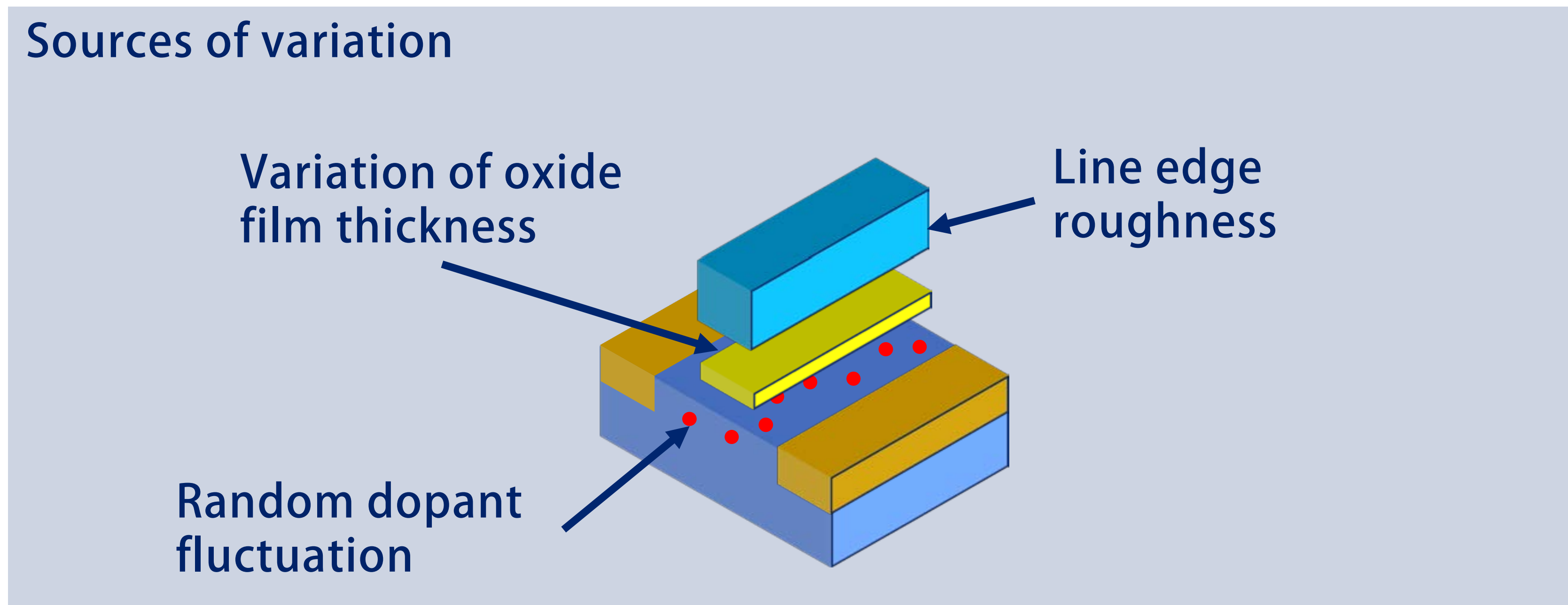
Introduction: Increasing Process Variations

- As minimum feature size shrinks, effect of process variations becomes more and more dramatic



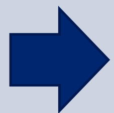
- First mentioned by William Shockley in his analysis of junction breakdown
- Getting more attention at sub-100nm

Why Failure Probability Analysis?

Higher device density and smaller device size are two major factors causing serious yield loss

(1) Increasing Device Density

Consider 1M identical memory cells and assume that failure probability of each cell is 10^{-6}



Probability of Failure:

$$1-(0.999999)^{1000000}=0.63$$

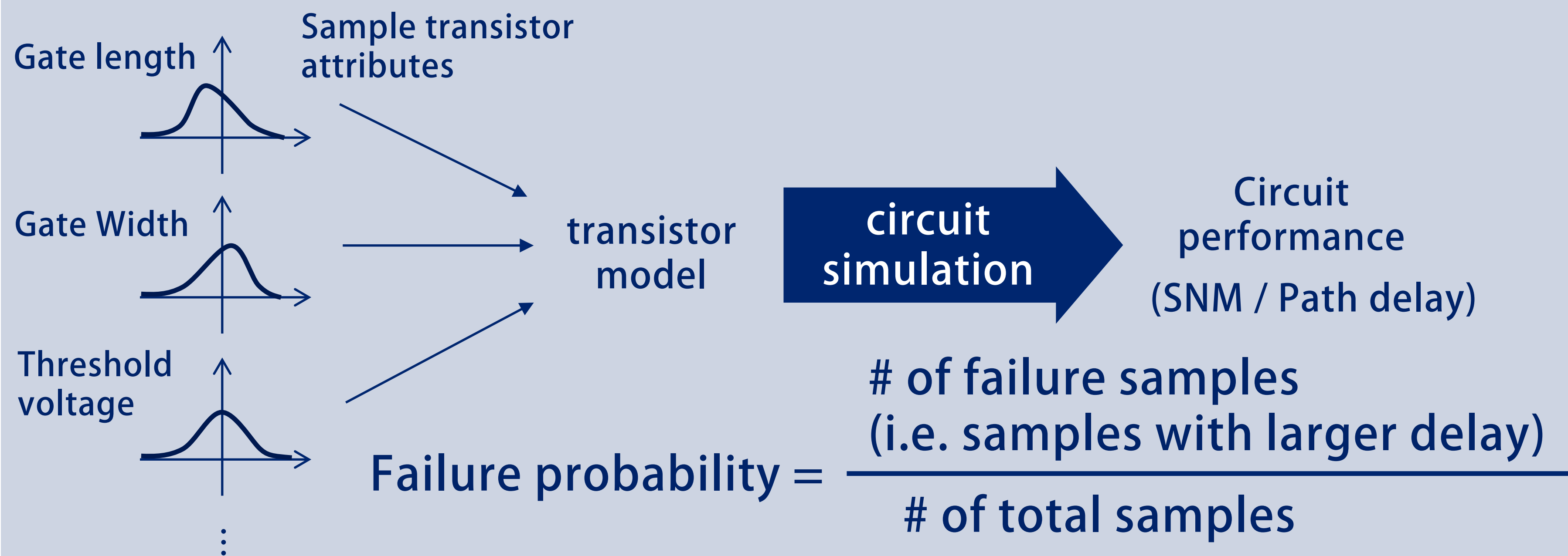
(2) Smaller Device Size

Impact of process variation becomes large compared to device size

Rare circuit failure probability analysis is essential technique for debugging in pre-silicon validation phase

Monte Carlo Simulation

Still used as golden reference for circuit failure probability



$$\text{Failure probability} = \frac{\text{\# of failure samples (i.e. samples with larger delay)}}{\text{\# of total samples}}$$

Problem

- Billions of Monte Carlo trials are required to obtain sufficient number of failure samples
- Increasing sampling efficiency (e.g. importance sampling) is mandatory

Aging

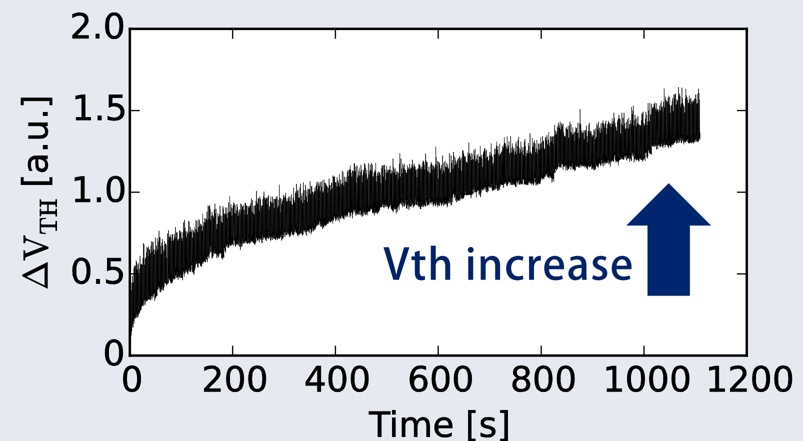
- **Increasing device density promotes device degradation:**
  - Negative/Positive bias temperature instability (NBTI/PBTI)
  - Hot-carrier injection (HCI) etc.

NBTI-induced Vth shift

NBTI/PBTI = gradual shifts of threshold voltages of transistors

Right figure:
NBTI observed on pMOS transistors fabricated using 180nm CMOS process

Threshold voltage increase is clearly observed



Lifetime Yield

- Device aging causes temporal change of yield: Lifetime Yield
  - Lifetime yield = Initial yield (Process variation) + Aging effect

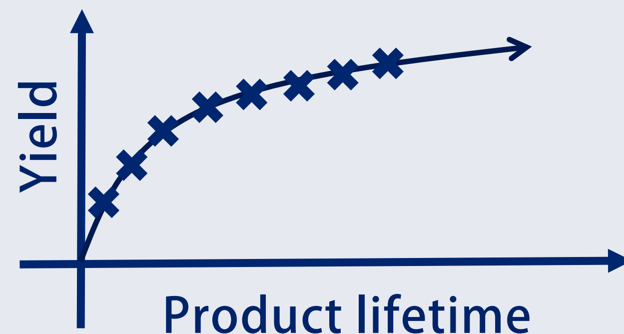
Lifetime yield estimation:

Estimate $P(F|\varphi)$ as a function of φ

F : Failure event

φ : Device age

multiple yield estimation at each aging time step



Problem:
Lifetime yield estimation requires multiple yield estimation at each aging time step ➔ Quite time consuming

Purpose of this work:

Evaluate lifetime yield with only a single yield estimation

Augmented reliability problem

Conventional reliability problem

Random variables ➔ transistors' attributes (Vth, width, length,⋯)

AUGMENTED reliability problem

Random variables ➔ transistors' attributes (Vth, width, length,⋯)

+ Device age (artificially treated as random variable)

By treating $\boldsymbol{\varphi}$ as random variable, Bayes theorem can be applied to yield following equation:

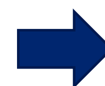
$$P(F|\varphi) = \frac{1}{P(\varphi)} P(F) P(\varphi|F)$$

F : Failure event
φ : Device age

$\boldsymbol{P(\varphi)}$: artificially given probability distribution, i.e. already known

$\boldsymbol{P(F)}$: Augmented failure probability

$\boldsymbol{P(\varphi|F)}$: Conditional failure probability



can be obtained with single Monte Carlo estimation (described in later slide)

Calculation of Augmented Failure Probability

$$P(F|\varphi) = \frac{1}{P(\varphi)} P(F) P(\varphi|F)$$

Since failure event is rare, naive MC takes quite long time to converge

➡ Subset simulation (SubSim) is introduced

Subset simulation

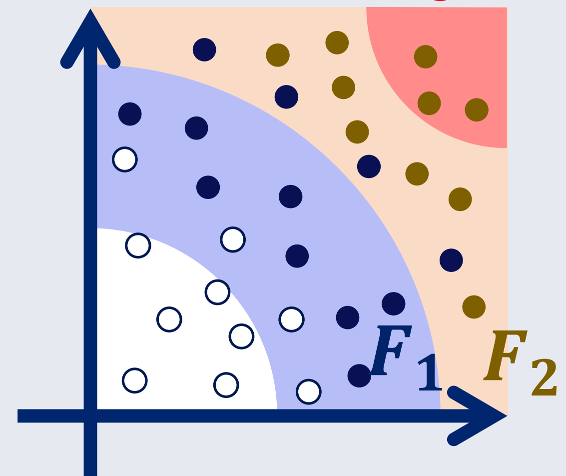
Basic idea: express small failure probability as a product of larger conditional failure probabilities

Small failure probability

$$\boldsymbol{P(F)} = \boldsymbol{P(F_1) \times P(F_2|F_1) \times P(F|F_2)}$$

$$= \boldsymbol{P(F_1) \cdot \prod_{k=2}^{K} P(F_k|F_{k-1})}$$

Larger failure probability
(can be calculated with conventional MC)

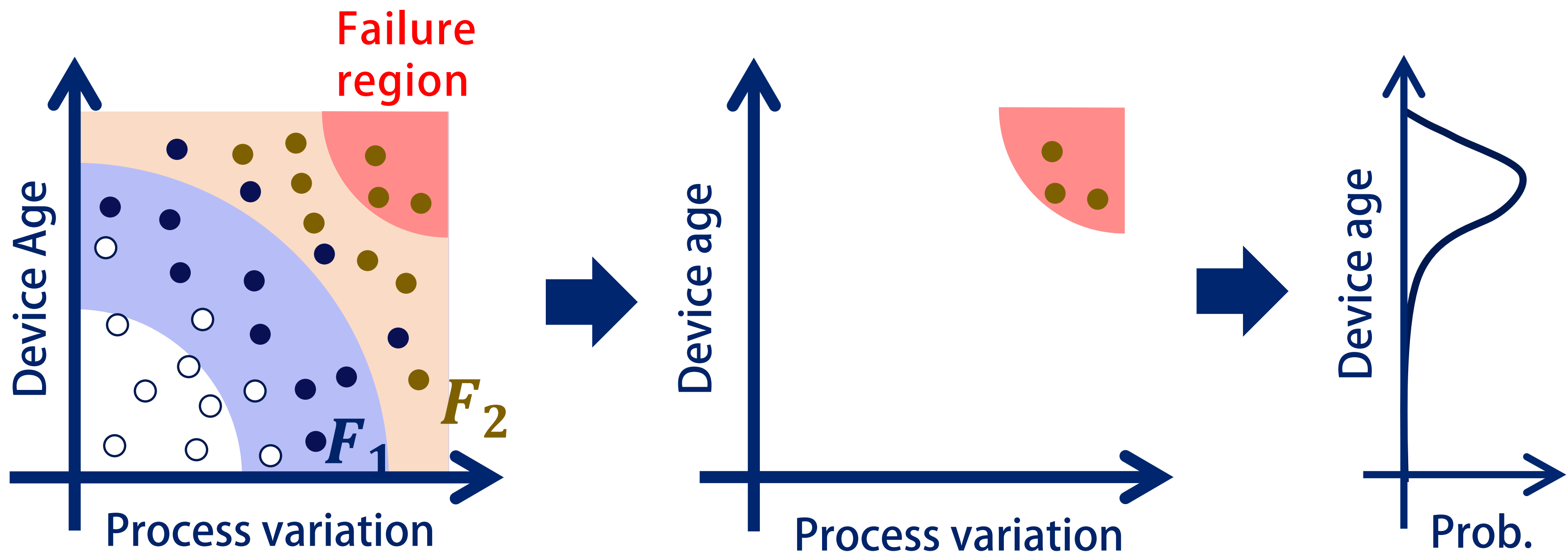


Calculation of Conditional Failure Probability

$$P(F|\varphi) = \frac{1}{P(\varphi)} P(F) P(\varphi|F)$$

At the final step of SubSim, augmented failure samples which incorporates both process variation and device age are obtained

➡ By marginalizing out the term of process variation, the conditional failure probability is obtained

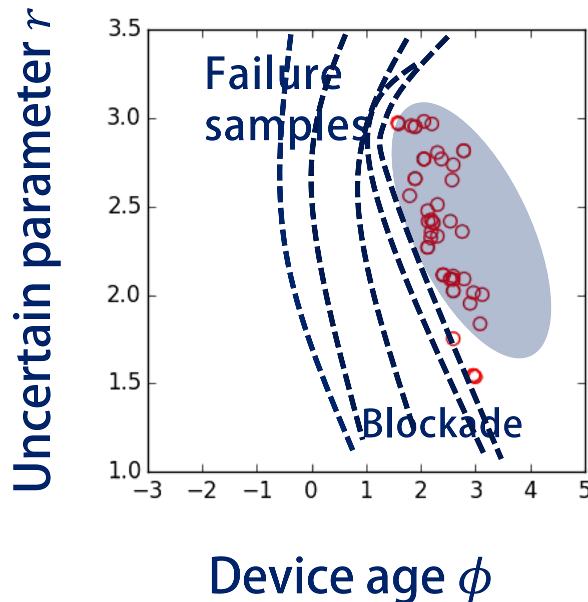


Demonstration: 1-dimensional reliability problem

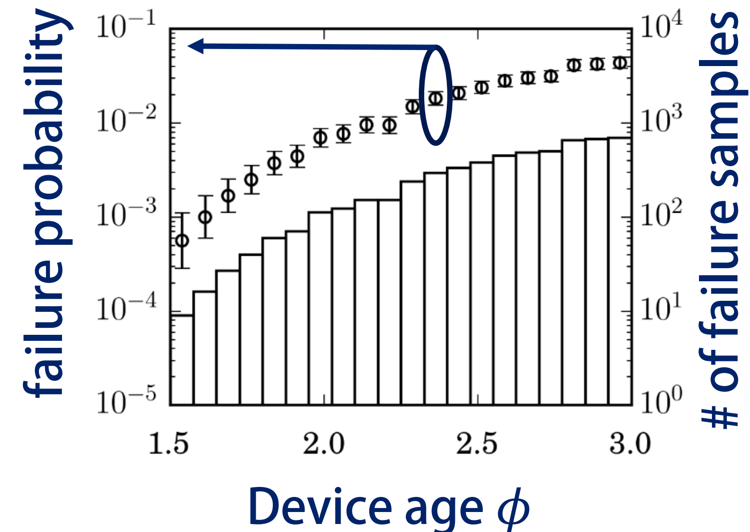
Estimate probability that $r \cdot \phi$ exceeds threshold C

r : Gaussian random variable
ϕ : Device age
C : Target performance threshold

Step1
Generate failure samples using SubSim



Step2
Calculate conditional failure probability



Proposed failure probability calculation method

Initialize

1. Process variability 🡐 D-dimensional normally distributed variable
2. Device age 🡐 1-dimensional uniformly distribute variable

1st Subsim

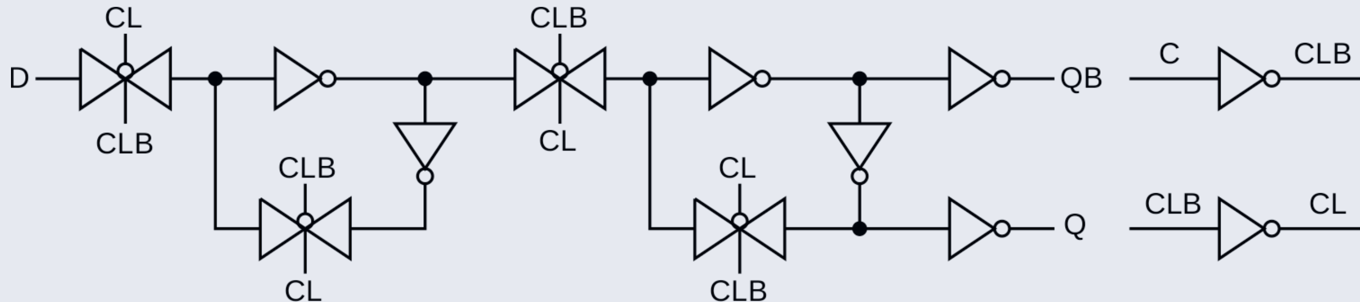
3. Calculate performance metric with SPICE
4. Select worst T samples as seed samples for next iteration

MCMC

5. Generate Markov chains for each T seed samples
6. Again calculate performance metric with SPICE
7. Select worst T samples and as seed sample for next iteration

Numerical Experiment

Target circuit: Standard D Flip-Flop with 24 transistors
Process: Commercial 65-nm

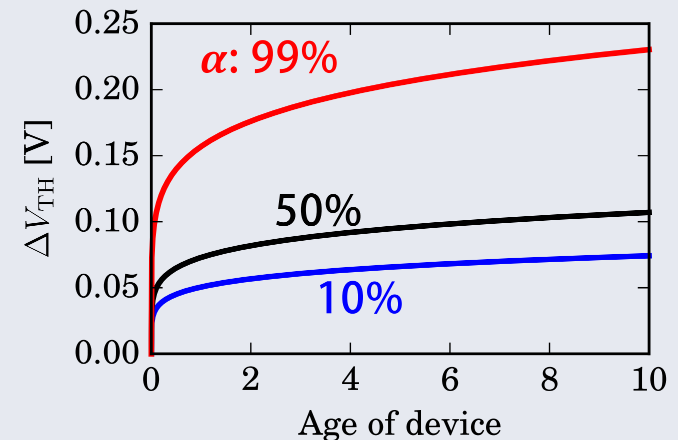


Target failure: Exceedance of Clock-to-Q delay

Aging model: NBTI-induced Vth increase

$$\Delta V_{TH} \propto \left(\frac{\alpha \cdot t}{1-\alpha}\right)^{n}$$

n : Time exponents
α : Stress probability



In our experiment, α is set to be 50%, i.e. DFF stores "1" and "0" with equal probability

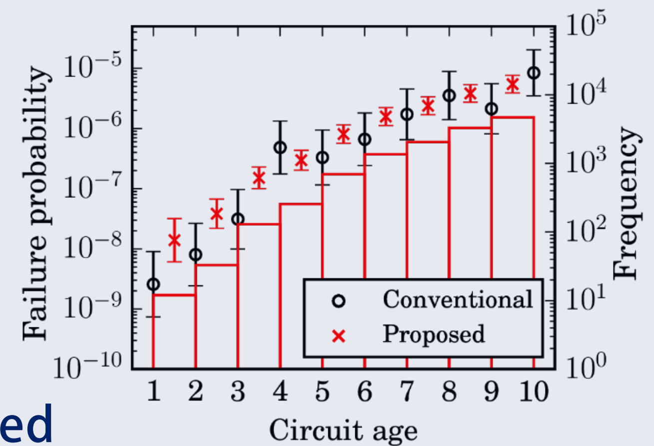
Experimental result

Estimated lifetime yield

- Conventional method
  - Conduct SubSim-based reliability analysis at each aging time step
- Proposed method

Results of conventional and proposed method matches well

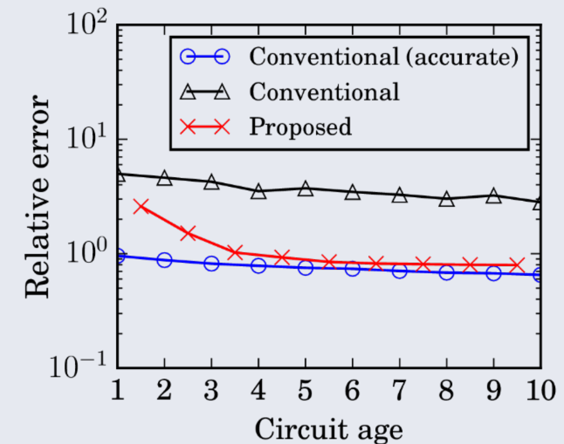
➡ Reliability of the proposed method is validated



Accuracy comparison

- Conventional method
- Conventional method (10x more simulations)
- Proposed method

Proposed method achieves almost same accuracy compared to conventional method with 10x more simulations



$$\text{Relative error} : \frac{\text{95\% of confidence interval}}{\text{Failure probability}}$$

Summary

- Device aging is important physics in deca-nanometer process
- Aging-aware yield estimation becomes urgent issue for reliable circuit design

- In this presentation…
  - Efficient circuit failure probability calculation for life time yield estimation is proposed.
  - By combining subset simulation and augmented reliability, time change of yield is calculated with only single SubSim run.
  - Achieved almost 10x speed up compared to conventional method