Network Flow Based Cut Redistribution and Insertion for Advanced 1D Layout Design

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Outline

- Introduction
- Techniques to Print Cuts with 193i
- Experimental Results
- Conclusion

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- **Introduction**
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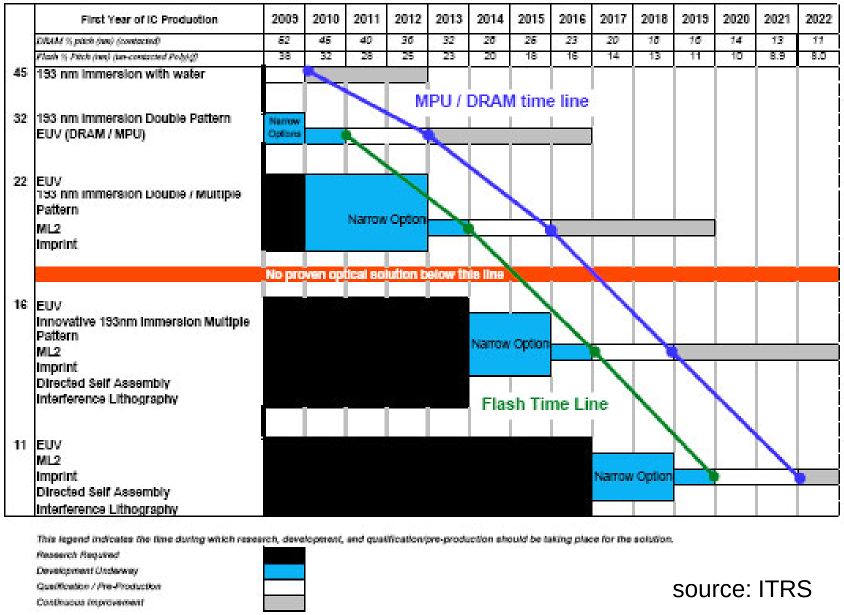
Sub-10nm Technology Node

- **Technology candidates**
  - Quadruple Patterning Lithography
    - **Overlay Error**
  - Self-Aligned Multiple Patterning
    - **Complex Block Mask Shapes**
  - E-Beam
    - **Low Productivity**
  - EUV
    - **Not Ready**

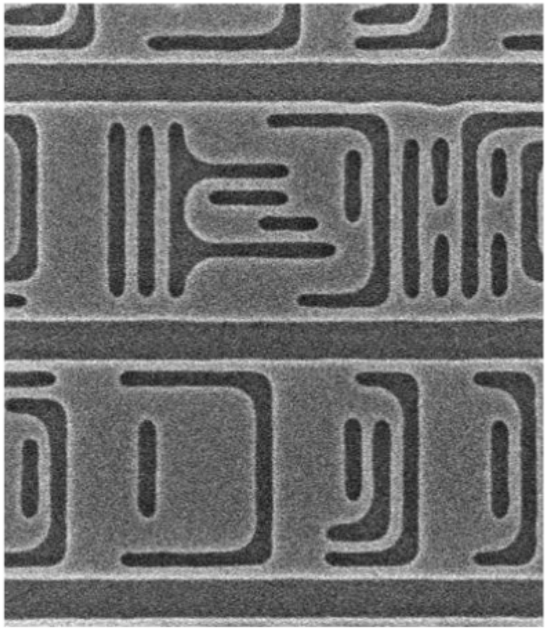


source: ITRS

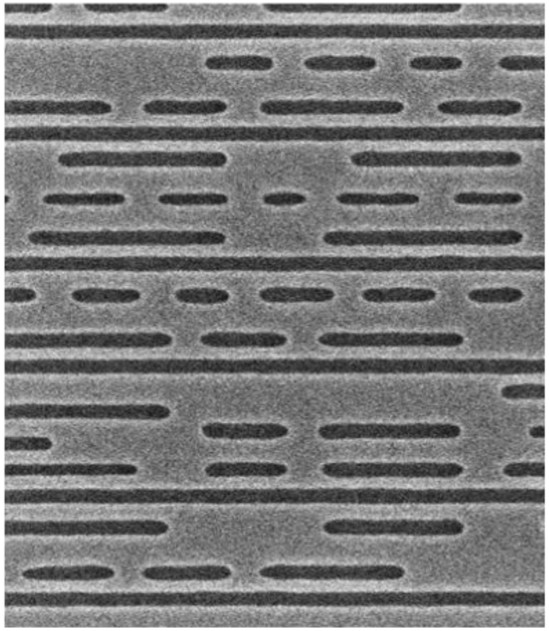
Sub-10nm Technology Node

- **Technology candidates**
  - **Advanced 1D Process**

2D Process



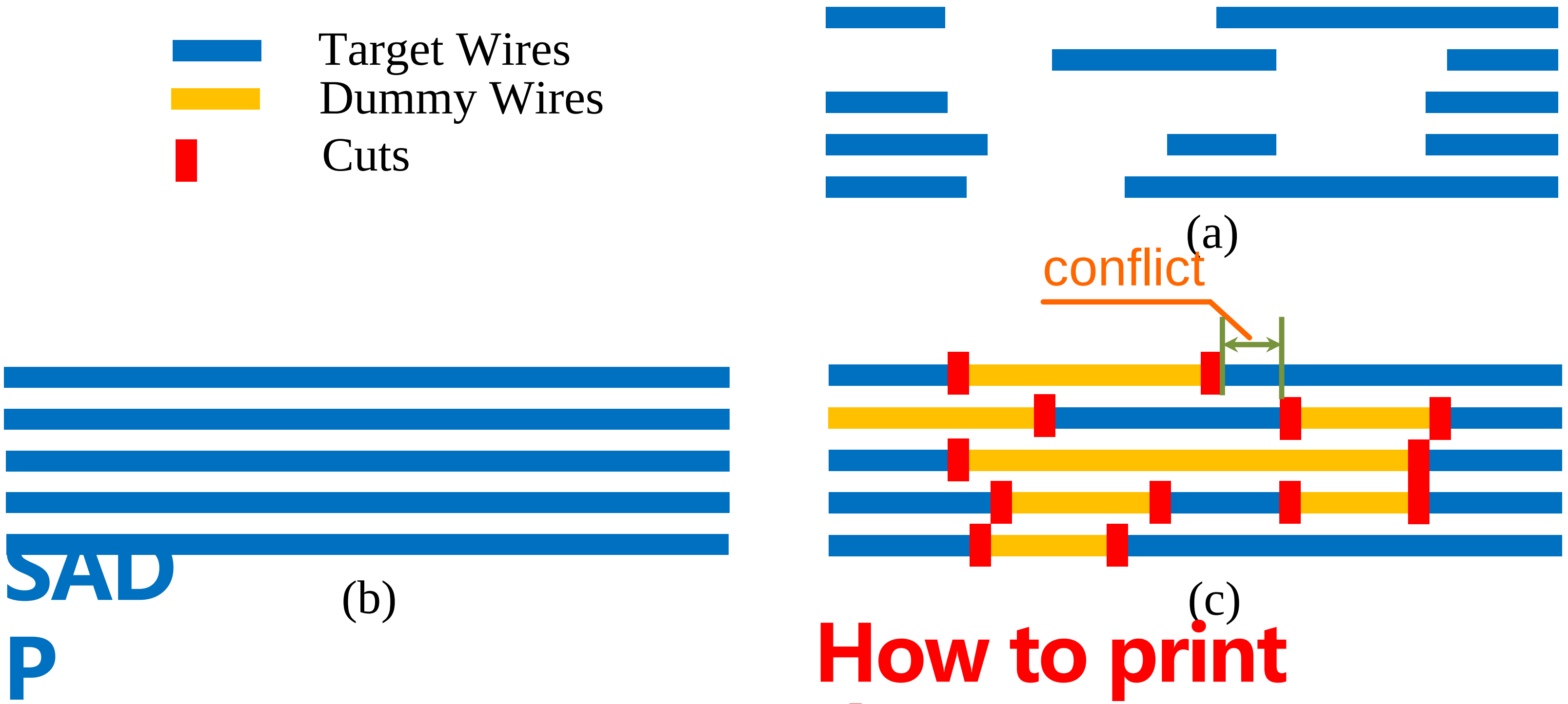
1D Process



source: www.techdesignforums.com/practice/guides/triple-patterning-self-aligned-double-patterning-sadp/

Advanced 1D Process

Process Demo



How to print the cuts?

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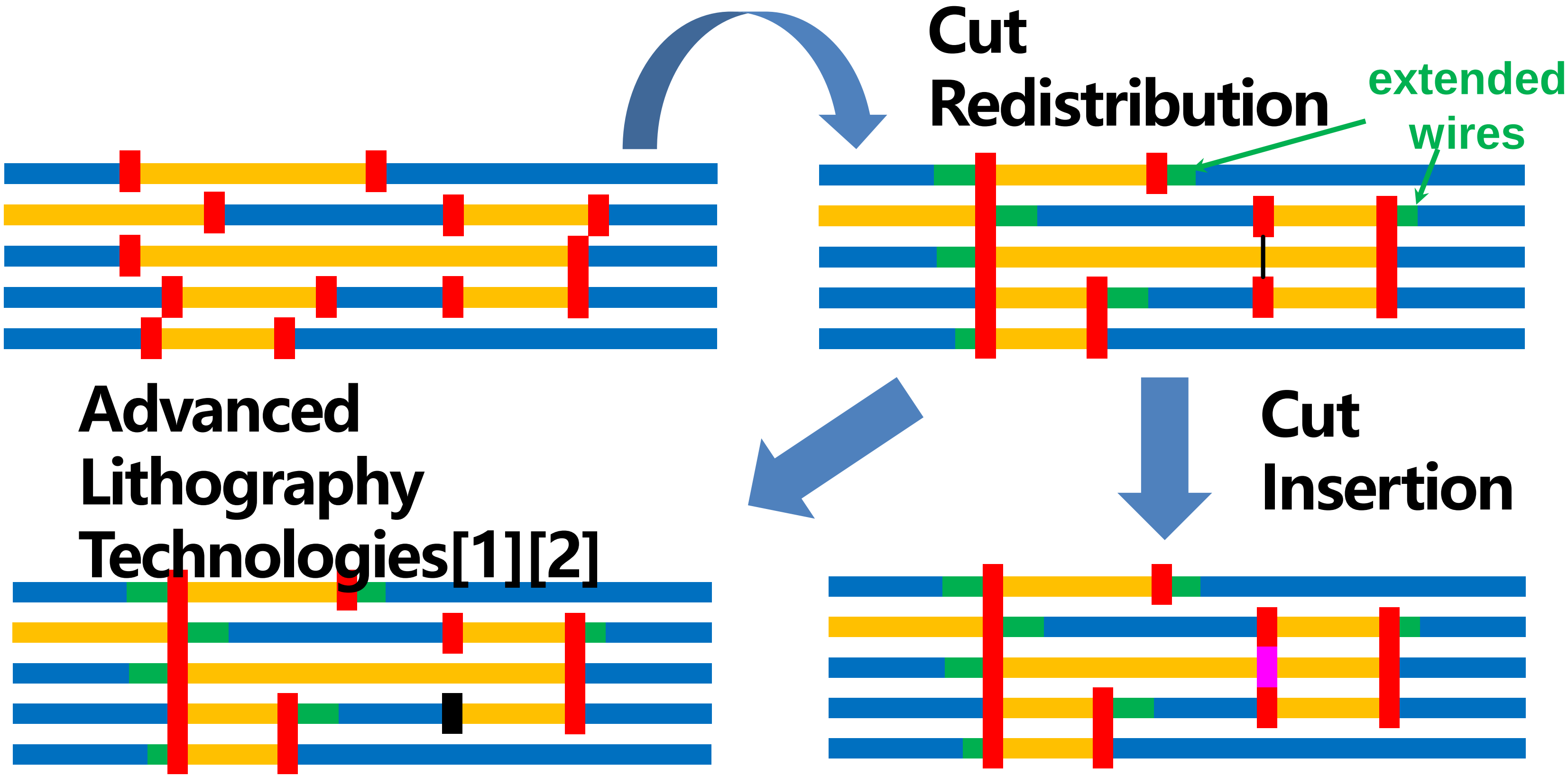
Conflicts Removal Techniques



[1] Y. Du, et al., “Hybrid lithography optimization with e-beam and immersion processes for 16nm 1D gridded design,” ASP-DAC 2012.
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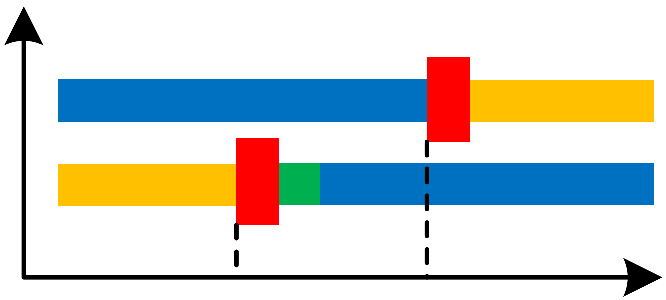
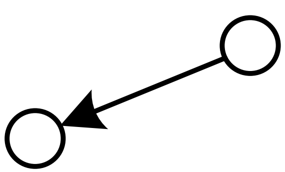
Cut Redistribution

Cut Constraints

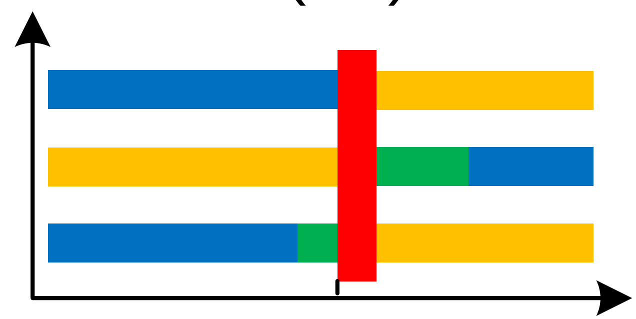
SEPARATION (C1)



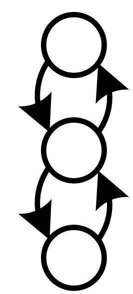
$$x_i - x_j \le -d_b \; for \; |y_i - y_j| = b \; \vee$$
$$x_j - x_i \le -d_b \; for \; |y_i - y_j| = b$$



MERGING (C2)



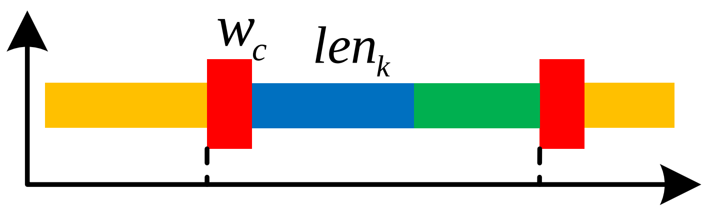
$$x_i - x_j \le 0 \wedge x_j - x_i \le 0$$
$$for \; |y_i - y_j| \le 1$$



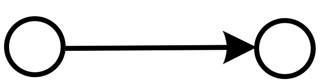
Cut Redistribution

Cut Constraints(cont.)

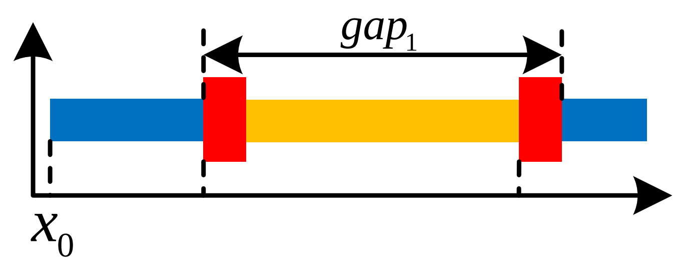
EXTENSION (C3)



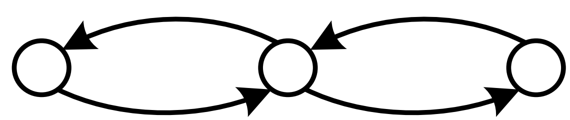
$$x_{i+1} - x_i \le len_k + t_k + w_c$$



BOUND (C4)



$$x_0 - x_i \le -l_i \wedge x_i - x_0 \le r_i - w_c$$



Problem Formulation of Cut Redistribution

Scenarios of two cuts' positions		Constraints
On the same line	Share the same gap	$C1 \vee C2$
	Share the same target wire	$C1 \wedge C3$
	Neither above	$C1$
On different lines		$C1 \vee C2$

C4 must be met for all cuts.

If ∨ is eliminated, the cut redistribution problem can be formulated as:

Dual form of a min-cost flow problem, can be optimally solved.

Total wire length **≈ #violated constraints**

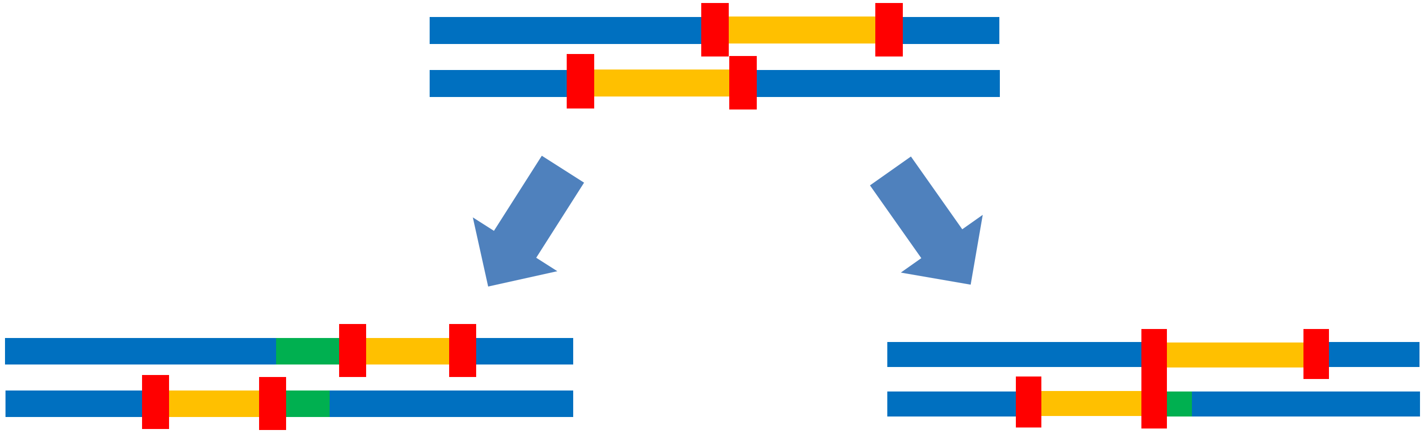
$$\min \sum_{v_i \in V} b_i x_i + \sum_{(v_i, v_j) \in E} m_{ij} \alpha_{ij}$$

$$\text{s.t. } x_i - x_j \le c_{ij} + \alpha_{ij}, \forall (v_i, v_j) \in E$$

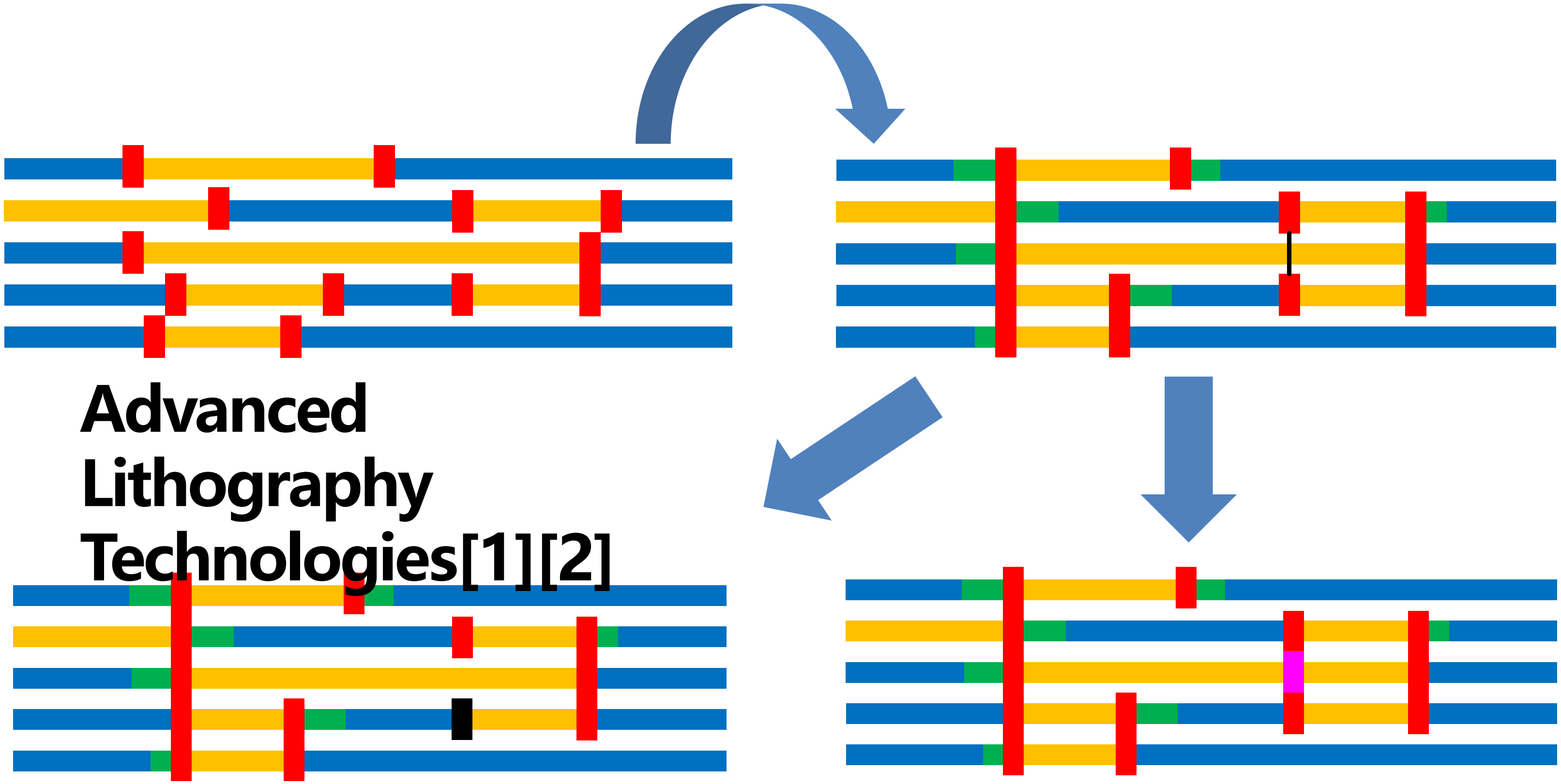
$$\alpha_{ij} \ge 0, \forall (v_i, v_j) \in E.$$

LRM Determination

- **LRM:**
  - ***A* Left-of *B*, *A* Right-of *B*, *A* Merge-into *B***
  - **If LRM of each pair of cuts are given, ∨ in the constraints can be eliminated.**
  - **Determined by randomly generating cuts' initial positions.**



Conflicts Removal Techniques



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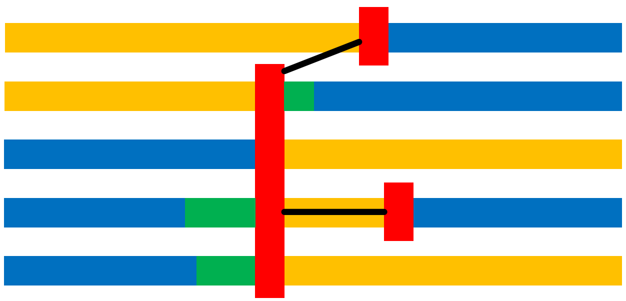
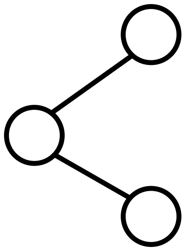
Advanced Lithography Technologies





$G_c = (V_c, E_c)$

MWVC

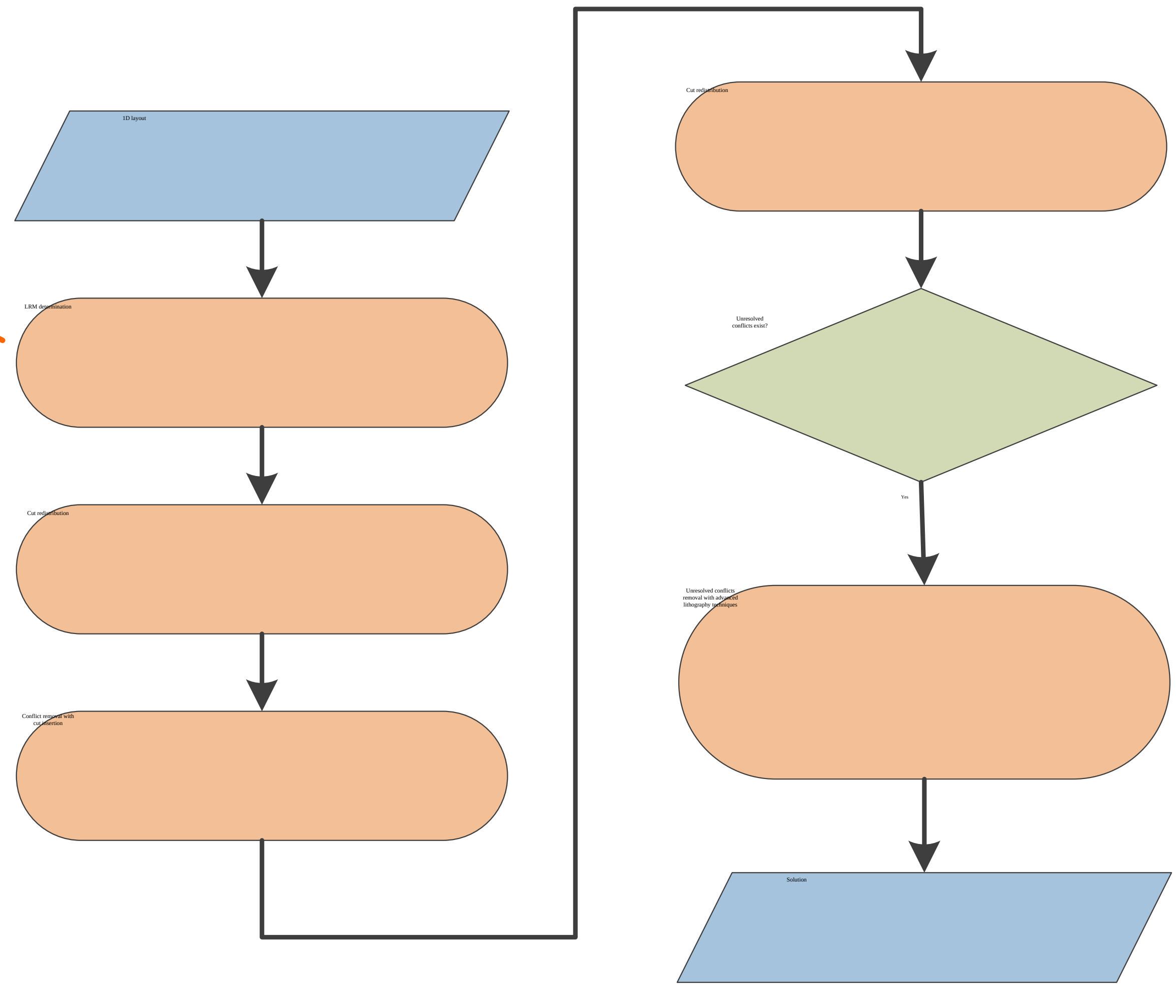
$$\mathbf{min} \sum_{v \in V_c} w_v h_v$$
$$\mathbf{s.t.}\ h_u + h_v \geq 1, \forall (u,v) \in E_c$$
$$h_v \in \{0,1\}, \forall v \in V_c.$$

Technique Candidates	Complementary E-Beam	Multiple Patterning Lithography	MPL+E-Beam
Optimization Model	minimum weighted node cover	*k*-coloring	minimum odd cycle cover

Proposed Framework

conduct n_s runs

randomization



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Comparison with ILP Formulation

	DAC'14		Ours(n_s=2)	
Design	cost	CPU(s)	cost	CPU(s)
50	7053	0.09	6127	0.02
100	12106	2.37	9768	0.02
150	18236	4.08	14382	0.03
200	24244	0.04	22515	0.05
250	29824	4.02	29678	0.09
300	34903	4.88	37785	0.13
1000	134560	1144.65	128635	1.47
2000	260623	623.99	246057	3.36
4000	519447	1866.07	501905	15.83
8000	1091424	12975	1019417	65.88
avg.	213242	1662.52	**201627**	**8.69**
ratio	1	1	**0.946**	**0.005**

$$\boldsymbol{cost} = \boldsymbol{\omega}|\boldsymbol{e}| + \boldsymbol{ext}$$

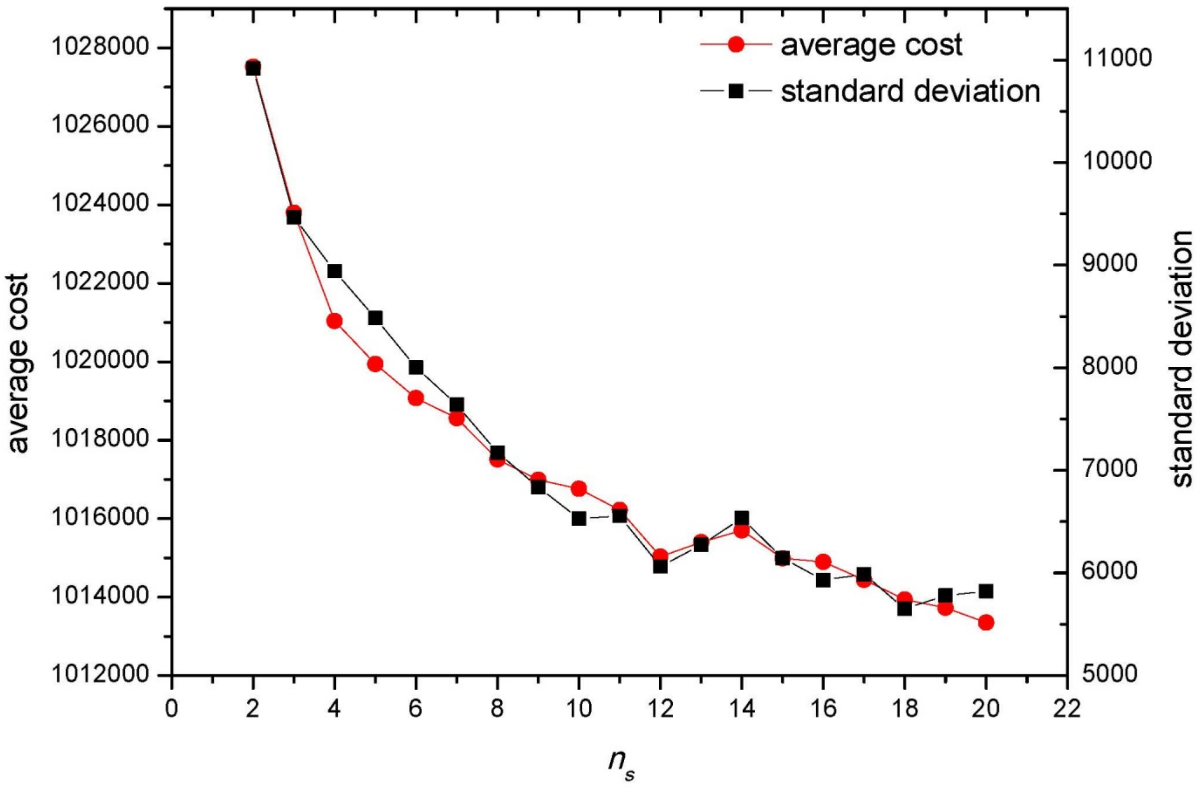
$|\boldsymbol{e}|$: #E-Beam cuts

$\boldsymbol{ext}$: extended wires' length

$\boldsymbol{\omega}$: 500

achieved **200x** speedup

Results with Different n_s



Better solution can be achieved if more CPU resources are given.

Conclusion

- Propose a framework to eliminate the conflicts between cuts with cut redistribution, cut insertion and advanced lithography technologies.

- With fixed LRM, the cut redistribution problem can be formulated as a min-cost flow problem.

- E-Beam throughput optimization problem is formulated as a minimum weighted node cover problem.

- Achieve **200x** speedup.

THX

Q&A