Optimizing Dynamic Mapping Techniques for On-Line NoC Test

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Outline

- Background
- Problem definition
- Testing-aware mapping algorithm (TAMA)
- Evaluation
- Conclusion
Background

Network on Chip

- a modular and scalable communication architecture

Intermittent faults

- tiny defects
- internal defects
- aging process
- wear-out

- occur repeatedly in fixed positions while having a certain randomness on the time of occurrence

Mapping algorithms

- increasing test frequency
- idle times

- decide the location of application tasks
- underlying routing algorithm and the mapping strategy distinguish idle paths
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A link/path test:
 testing all the components between the TPG unit of one router to the TPA unit of the next router
Testing the Paths

An application with 8 tasks and 9 edges running on NoC. We use the underlying XY routing to show the result of free (green) and occupied (red) paths.
On-the-field test strategy

The path test time under two conditions.

- **idle**: represents when the link is not occupied.
- **occupied**: represents when the link is occupied by application.
- **test**: represents when test was interrupted by the application.
- **test**: represents when test ends.

The test start time; Identifying and testing the free paths; Handling the conflicting situation of test and mapping
Define a reliability evaluation: average test time
Lower average test time means higher test frequency
detect intermittent faults
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The link utilization is defined:

\[ L_{utilization} = \frac{\sum_{t=1}^{T_s} N_c(t)}{N_l \times T_s} \]

- \( N_c \): the number of utilized paths at each simulation cycle;
- \( N_l \): the number of paths in the network;
- \( T_s \): the total simulation cycles.
Testing-aware mapping algorithm (TAMA)

- Path utilization is less than 10%
- Paths are mostly in an idle mode
- Test those paths
- On-line test scheduling method
- Balance test and mapping
- A reasonable mapping algorithm
there is a quest for a testing-aware mapping algorithm

TAMA

mapping application

detecting intermittent faults

1: first task

the largest number of edges and communication volume

2: remaining tasks

the breadth-first traversal technique

A. Sorting tasks
Testing-aware mapping algorithm (TAMA)
B. Mapping tasks to nodes

1. first node
   a. maximum number of free neighbors
   b. maximum number of tested links
   c. closer to the manager

2. remaining nodes
   a. closest to the father task node
   b. maximum number of tested links
   c. data flow direction
Testing-aware mapping algorithm (TAMA)
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Maximum Test Time and Average Test Time

(a) Obviously decreases the maximum test time and average test time. The benefit of TAMA is more significant in lower usage rates.

(b) Testing paths at idle times.
Interrupted test rate defined as:

$$T_{\text{interrupted}} = \frac{T_c + T_{ic}}{T_c}$$

- The interrupted test rate is lowested in TAMA
- The fact that TAMA identifies the idle paths

- $T_c$: the total number of test path during the application mapping
- $T_{ic}$: the number of test that are interrupted due to the request of mapping
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AWMD and Average Latency

The AWMA of TAMA is always lower than the other methods. The average latency follows the same trend.
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Conclusion

✓ A mapping algorithm to map application and detect intermittent faults over the NoC platform

✓ Experimental results showed that our mapping algorithm leads to improvements on the maximum test time, average test time and interrupt rate at no comprise of AWMD and average latency
Thank You!

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