Building Blocks

- Retimer based ADPLL
- Direct Modulation Technique
- Low Noise figure using 25% duty generator
  - Driving Passive mixer
  - Current mode operation

<ADPLL based Transmitter>
- **Process**: 1-poly 6-metal 55-nm CMOS
- **Area**: 1.79 mm\(^2\) (Transceiver + DC-DC Converter)
Tx Measurement

- **Fc = 2.44 GHz**
  - -84.8 dBc/Hz @ 100 kHz offset
  - -118.9 dBc/Hz @ 1 MHz offset

- **Phase noise**

- **Preamble** & **Data**

- **Carrier Power**
  - -2.59 dBm
  - -60.00 dBc/
  - 1.00000 MHz

- **Atten**
  - 0.00 dB

- **Mkr1**
  - -118.89 dBc/

- **Ref**
  - -60.00 dBc/
  - 10.00 dB/

- **Frequency Offset**
  - 10 kHz
  - 100 kHz
  - 1 MHz
  - 10 MHz

- **Trace 1**
  - -84.04 dBc/Hz
  - -83.63 dBc/Hz
  - -119.56 dBc/Hz
  - -129.78 dBc/Hz

- **Trace 2**
  - -86.33 dBc/Hz
  - -84.78 dBc/Hz
  - -118.89 dBc/Hz
  - -130.79 dBc/Hz

- **Trace 3**
  - -----
**IIP3, NF / BLE Ch.**

- **6.2 < NF < 6.8 dB**
- **-19 < IIP3 < -18.2 dBm**

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### This Work

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<tr>
<td>CMOS technology</td>
<td>55 nm</td>
<td>55 nm</td>
<td>65 nm</td>
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<td>Supply voltage (V)</td>
<td>3.0</td>
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<tr>
<td>TX output power class</td>
<td>0 dBm</td>
<td>0 dBm</td>
<td>0 dBm</td>
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<td>TRX Switch</td>
<td>Integrated</td>
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<td>None</td>
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<td>TX power Consumption (mW)</td>
<td><strong>6 @ 0 dBm</strong></td>
<td>10.1 @ 0 dBm</td>
<td>10.5 @ 0 dBm</td>
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<td>RX architecture</td>
<td>Low-IF</td>
<td>Low-IF</td>
<td>Zero-IF</td>
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<td>RX power Consumption (mW)</td>
<td>5</td>
<td>11.2</td>
<td>9.3</td>
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<td>Noise figure (dB)</td>
<td>*6.8</td>
<td>5.5</td>
<td>6</td>
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<tr>
<td>RX sensitivity (dBm)</td>
<td>-94</td>
<td>-94.5</td>
<td>-94</td>
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<tr>
<td>Area (mm²)</td>
<td><strong>1.79</strong></td>
<td><strong>2.9</strong></td>
<td>1.1</td>
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