Design of Resource Sharing
Reconfigurable ΔΣ SAR-ADC

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Background

• Need of ADC for wireless sensor network
  – Vast variety of sensing signal

• $\Delta \Sigma$ SAR ADC
  – Fully Passive integrator
    Low power, Small area  Incomplete integrate
    → High resolution is challenging
  – Active integrator
    High resolution Large area
    → Small area is challenging
Block Diagram

- Almost capacitor are Time-sharing
  - Three benefits
    - Reduce the capacitor area ($4C_{DAC}$ with differential)
    - Use Charge shuttling Technique
    - Ease the reduction of nonlinearity
**Resource Sharing Technique**

1. **Δ phase**
   - \( C_{DAC} \) set the difference voltage

2. **Σ phase**
   - The charge is transferred \( C_{STORE} \) to \( C_{DAC} \)

3. **Quantization Phase**

4. **Store phase**
   - the integrated signal returns to \( C_{STORE} \)
Measurement Results

- **SAR only mode**
  - Sampling freq. vs SNDR, Power
  - Peak ENOB: 7.7bit

- **ΔΣ assisted mode**
  - FFT spectrum
  - SNDR = 62.9dB
  - Fin = 12KHz
  - Fs = 4.096MHz
  - BW = 60kHz