A 5.8GHz DSRC Digitally Controlled CMOS RF-SoC Transceiver for China Electronic Toll Collection

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January 24, 2018

ASP-DAC University Design Contest
Features

• Fully integrated transceiver (RF+analog+baseband)
  ➢ First RF-SoC integration for ETC systems

• Digital control adjusts operation of RF circuits
  ➢ Advanced control algorithm, immune to process variation

• Simplified system architecture
  ➢ Eliminate non-essential analog blocks (e.g. filters, DAC, voltage-current converter)

• Significant performance improvement
  ➢ 37% in peak output power, 12% in dynamic operation range, 34% in area savings, etc.
Architecture and Implementation

**Tx**
- ASK modulator (32 tuning steps)
- PA (4 gain options)

**Rx**
- LNA (4 gain options)
- Mixer (4 gain options)
- PGA₁ (2 gain options)
- PGA₂ (16 gain options)
Measurement Results

**Graph 1:**
- **Peak:** 4.23 dBm
- **Valley:** -33.28 dBm

**Graph 2:**
- **Graph Legend:**
  - PA (Gain Option #1)
  - PA (Gain Option #2)
  - PA (Gain Option #3)
  - PA (Gain Option #4)

**Graph 3:**
- **Graph Legend:**
  - Gain mode 1
  - Gain mode 2
  - Gain mode 3
  - Gain mode 4
  - Gain mode 5
## Performance Comparison

<table>
<thead>
<tr>
<th>Reference</th>
<th>[ISCAS, 2008]</th>
<th>[TMTT, 2010]</th>
<th>[ISSCC, 2012]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>CMOS180nm</td>
<td>CMOS130nm</td>
<td>CMOS130nm</td>
<td>CMOS130nm</td>
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<tr>
<td>Control</td>
<td>analog</td>
<td>analog</td>
<td>analog</td>
<td>digital</td>
</tr>
<tr>
<td>Tx output peak power (dBm)</td>
<td>+10.5 (differential)</td>
<td>+10 (differential)</td>
<td>+5 (single end)</td>
<td>+7.23 (single end)</td>
</tr>
<tr>
<td>OBW (MHz)</td>
<td>2~6</td>
<td>N/A</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>ACPR (dBc)</td>
<td>-49 (+6MHz)</td>
<td>-43 (+5MHz)</td>
<td>-53 (+5MHz)</td>
<td>-38 (+5MHz)</td>
</tr>
<tr>
<td>Tx dynamic range (dB)</td>
<td>19</td>
<td>N/A</td>
<td>34</td>
<td>37</td>
</tr>
<tr>
<td>Rx dynamic range (dBm)</td>
<td>-76 ~ -40</td>
<td>-84 ~ N/A</td>
<td>-60 ~ 0</td>
<td>-76 ~ -8</td>
</tr>
<tr>
<td>BER</td>
<td>N/A</td>
<td>10^-5</td>
<td>N/A</td>
<td>10^-6</td>
</tr>
<tr>
<td>AGC</td>
<td>Limited</td>
<td>limited</td>
<td>No</td>
<td>On-chip</td>
</tr>
<tr>
<td>Area of RF blocks (mm²)</td>
<td>N/A</td>
<td>3.31</td>
<td>2</td>
<td>1.32</td>
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<td>Current consumption of RF blocks (mA)</td>
<td>51</td>
<td>N/A</td>
<td>59</td>
<td>58</td>
</tr>
</tbody>
</table>

Advantages in design flexibility, Tx output peak power, Tx & Rx dynamic range, Rx sensitivity, BER, area