A Reconfigurable SIMO System with 10-Output Dual-Bus DC-DC Converter using the Load Balancing Function in Group Allocator for Diversified Load Condition

Se-Un Shin, Sang-Hui Park, Gyu-Hyeong Cho
sswsin@kaist.ac.kr

January 24, 2018
Issues in Diversified Load Condition

Diversified Load Condition

Fixed Freq. Control w/ Light Loads

@ Light Load

DON, DESIRED

VON

η

t

Unregulated!

Switching Loss

< Unregulated Output >

< Low Efficiency >

Efficiency of SIMO Converter

Peak Efficiency Region

Diversified Load Condition

APM Control or Pulse Skip w/ Heavy Loads

VON

IA1

Irregular Switching

Large Ripple

< Regulation Problem >

Failure

Increased

EMI spec.

< EMI Problem >
Proposed DBMO Converter

Well-balanced Condition!!

Well-defined Spectrum Satisfied to EMI Spec.

High Efficiency in Wide Load Range

Small Ripple & Well-regulation Performance

DBMO Converter

Reconfigurable SIMO system

Reconfigurable SIMO system

Heavy SIMO

Light SIMO

V_{ON}

Small Ripple !!

Heavy Loads

Light Loads

Easy to Filter out !!

Heavy Loads

Light Loads

Well-regulated Performance

Small Ripple & Well-regulation Performance

Heavy SIMO

Light SIMO

Fixed Frequency

H-bus

L-bus

APM

Group Allocator

Heavy?

Light?

Diversified Loads

Well-balanced Condition!!

Light SIMO

Heavy SIMO

Diversified Loads
Overall Structure of DBMO Converter

- **Gate Driver**
- **H-bus**
- **L-bus**
- **Group Allocator**
- **Comparator-based**
  - Detecting the polarity of $I_{ERRi}$ with $LD<i> = 1$
- **Protection block & Output SW gatedriver**
- **Maximum Error Selector**
  - Using the amplitude of $I_{ERRi}$ with $LD<i> = 0$
- **Main Duty Generator**
- **Global Controller**
  - The shared $gm$-cells
- **PFD**
- **CP**
- **VREF**
- **Vp**
- **ISAW**
- **IES,H**
- **IES,L**

Diagram showing the connections and components of the DBMO Converter, including the logic and signal flow between the various blocks.
### Measurement Results

#### Conventional SIMO Converter

- **V_{O4}(100mA)**
- **V_{O1}(5mA)**
- **V_{O2}(120mA)**

- **Unregulated!**

#### Proposed DBMO Converter

- **V_{O10}(40mA)**
- **V_{O7}(150mA)**

- **Large Ripple**

<table>
<thead>
<tr>
<th>Process</th>
<th>65nm</th>
<th>0.35μm</th>
<th>0.35μm</th>
<th>0.18μm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Topology</td>
<td>6 Buck outputs</td>
<td>4 Buck outputs</td>
<td>5 Buck outputs</td>
<td>10 DBMO outputs</td>
</tr>
<tr>
<td>Supply Voltage(V)</td>
<td>5.0</td>
<td>2.7 - 5.0</td>
<td>3.4 - 4.3</td>
<td>5.0</td>
</tr>
<tr>
<td>Frequency</td>
<td>2MHz</td>
<td>1MHz</td>
<td>1.2MHz</td>
<td>1MHz</td>
</tr>
<tr>
<td>Voltage Ripple</td>
<td>&lt; 25mV</td>
<td>&lt; 30mV</td>
<td>&lt; 40mV</td>
<td>&lt; 25mV</td>
</tr>
<tr>
<td>Load Balancing Function</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Supportable</td>
</tr>
<tr>
<td>Allowable Load Range</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>0mA - 300mA</td>
</tr>
<tr>
<td>Load Independency in Efficiency</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Reliability</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Switching Noise Dispersion</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Yes</td>
</tr>
<tr>
<td>Max. Output Power(W)</td>
<td>2.16</td>
<td>1.2</td>
<td>2.232</td>
<td>2.83</td>
</tr>
</tbody>
</table>

#### Efficiency

- **Efficiency [%]**

- **Dual Bus Multiple Output**

- **Reconfigurable SIMO System**

#### Chip Micrograph

- **2200μm**
- **4100μm**

- **Unregulated**

- **Label:** H-SIMO, L-SIMO

- **Measurements:**
  - **V_{O8}: 2.8V (I_{O8}: 70mA)**
  - **V_{O9}: 1.8V (I_{O9}: 130mA)**
  - **V_{O10}: 3.3V (I_{O10}: 40mA)**
  - **V_{O3}: 2.5V (I_{O3}: 120mA)**
  - **V_{O4}: 2.8V (I_{O4}: 150mA)**
  - **V_{O7}: 150mA**
  - **V_{O6}: 2.8V**
  - **V_{O5}: 2.8V**

- **SWs:**
  - **H-bus Main SW**
  - **L-bus Main SW**

- **Group Allocator**

- **Output SWs**

- **Controller**: Output SWs

- **Micrograph**: Chip