A Low-Power High-Speed Accuracy-Controllable Approximate Multiplier

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Outline

1. Introduction
2. Proposal
3. Experiment
4. Summary
Introduction

- Approximate multiplier with fixed accuracy
  - Low power consumption
  - High computing speed
- Why accuracy-controllable approximate multiplier?
  Application quality requirement may vary significantly,
  The above static approximate multiplier may,
  - fail to meet application quality requirement
  - waste power when high quality is not required

The objective is to control accuracy according to application requirements at runtime.
**Proposal**

### Approximate Tree Compressor

- **Accurate half adder**

  \[
  \{c,s\} = a + b = 2c + s = (c + s) + c;
  \]

- **Incomplete Adder Cell (iCAC)**

  \[
  p = c + s; \quad q = c;
  \]

  **Sum:** \[\{c,s\} = p + q\]
Approximate Tree Compressor

- **Structure of multi-bit iCACs**

  \[ A = \{a_n, \ldots, a_1, a_0\};\ B = \{b_n, \ldots, b_1, b_0\} \]

  \[ P = \{p_n, \ldots, p_1, p_0\};\ Q = \{q_n, \ldots, q_1, q_0\} \]

  \[ S = P + Q \]
Structure of an ATC with eight inputs (ATC-8)

ATC for partial product reduction (PPR)

\[ n \text{ inputs can be reduced to } n/2 \text{ } P \text{s and one } V. \]
Equivalent circuit of a half adder

- a half adder
- equivalent circuit of a half adder

Proposition
Carry-maskable Adder

- Carry-maskable half adder (CMHA)

- mask_x = 0 (Approximate)
  - $s = a \ OR b$;
  - $Cout = 0$;

- mask_x = 1 (Accurate)
  - $s = a \ XOR b$;
  - $Cout = a \ AND b$;
Carry-maskable Adder

- Carry-maskable full adder (CMFA)

Approximate condition: \( \text{mask}_x = 0, \ \text{Cin} = 0 \)

\[ S = a \ OR \ b; \ \text{Cout} = 0; \]
Carry-maskable Adder

- Carry-maskable adder (CMA)

  CMA for accuracy controllability

If $m_{x0}, m_{x1}, ..., m_{x7}$ are all “0”, carry chain is masked to “0”
8-bit Accuracy-Controllable Multiplier

Stage 1: ATC for PPR
Proposal

Accuracy-Controllable Multiplier

- **8-bit Accuracy-Controllable Multiplier**

  **Stage2**
  - OR gates for PPR

  **Stage3**
  - Adders for PPR

  **Stage4**
  - CMA for accuracy controllability
Experimental setup

For power, delay, and area
- Library: NanGate 45nm
- RTL language: Verilog HDL
- Simulator: Synopsys VCS
- Synthesis: Synopsys Design Compiler
- Power Consumption: Synopsys Power Compiler
- Test pattern: 65,536
- Data changing rate: 0.5GHz

For accuracy
- NMED: Normalized Mean Error Distance
- RMED: Relative Mean Error Distance
- ER: Error Rate
unmasked $u$ bits for accurate result
masked $(7 - u)$ bits for approximate result

Bits of CPA: 3 + u
Bits of OR gates: 3 + (7 - u)

<table>
<thead>
<tr>
<th>$u$</th>
<th>Bits of CPA</th>
<th>Bits of OR gates</th>
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<tbody>
<tr>
<td>m_7b</td>
<td>10</td>
<td>3</td>
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<tr>
<td>m_6b</td>
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<td>4</td>
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<tr>
<td>m_5b</td>
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<td>5</td>
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<tr>
<td>m_4b</td>
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<td>6</td>
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<td>m_3b</td>
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<td>7</td>
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<td>8</td>
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<tr>
<td>m_1b</td>
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<td>9</td>
</tr>
<tr>
<td>m_0b</td>
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<td>10</td>
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<td>Multipliers</td>
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<tr>
<td>------------</td>
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<tr>
<td>m_7b</td>
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<td>AMER_4b</td>
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<tr>
<td>ACCI_M2</td>
<td>0.04</td>
<td>0.62</td>
</tr>
</tbody>
</table>
Power results relative to MRED

- Proposed
- AMER
- ACCI_M2
- Wallace
Delay results relative to MRED

- Proposed
- AMER
- ACCI_M2
- Wallace

Critical Path Delay

Experiment

Delay (ns) vs. MRED
Accuracy setting no any effect on area of proposed multiplier.
Average PSNR from eight images

Experiment

Image Processing

Accuracy Controlled

Proposed multiplier

AMER

ACCI_M2

45dB
Summary

- **Objectives**
  - Low-power, High-speed multiplier
  - Accuracy-controllable multiplier

- **Solutions**
  - Approximate Tree Compressor (*ATC*)
  - Carry-maskable Adder (*CMA*)

- **Results**
  - 47.3% ~ 56.2% power reduction
  - 29.9% ~ 60.5% delay reduction
  - 19.7 ~ 52.5 PSNR controllability
Thank you!