Mechanical Strain and Temperature Optimization for Thin-Film Transistor Based Pseudo-CMOS Logic Array

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Outline

- Background and Motivation
- TFT based pseudo-CMOS logic array
  - Array circuit
  - Interconnect architecture
- Mapping problem formulation of logic array
- Mapping algorithms for logic array
- Experiments
- Conclusion
Background: Thin-film Transistor (TFT)

Fever alarm armband
F. Fuketa et al., ISSCC 2015

RFID tag
K. Myny et al., ISSCC 2017

E-skin
B. Tee et al., Science 2015

TFTs are essential to flexible and sensing applications.

However, TFTs have yield problem and are sensitive to temperature and strain...

Temperature for OTFT: >100% change @200K range

Bending for OTFT: ~20% change@15mm radius
Temp and strain effects on TFTs

Range of change in mobility of TFT technologies [11]

<table>
<thead>
<tr>
<th>TFT technology</th>
<th>Compressive strain</th>
<th>Tensile strain</th>
</tr>
</thead>
<tbody>
<tr>
<td>a-Si TFT</td>
<td>-26%</td>
<td>7.6%</td>
</tr>
<tr>
<td>OTFT</td>
<td>20%</td>
<td>-30%</td>
</tr>
<tr>
<td>poly-Si TFT</td>
<td>44%</td>
<td>-44%</td>
</tr>
</tbody>
</table>

Many works study the TFT mobility under temp & strain

Circuit level optimization to release some of these problems?

\[
\mu_{\text{eff}} = \mu_0 \exp\left(\frac{-E_A}{kT}\right)
\]

\[
\mu/\mu_0 = 1 + 26 \varepsilon
\]

\(\mu_0\): original mobility
\(T\): temperature
\(E_A\): energy difference between trap state and conduction band edge

Letizia J A et al., Advanced Functional Materials 2010
Gleskova, H et al., J. Non-Cryst 2004
Motivation: TFT logic array challenges

Inkjet-configurable gate array (IGA)
- Transistor level implementation
- Pre-fabricated interconnections
- Large area overhead

J. Carrabina et al., TETC 2016

Sea-Of-Transmission Gates (SOTG)
- Gate level implementation
- Complementary devices
- Routability problem

K. Ishida et al, JSSC 2011

Logic array of TFT
- Low cost: print wire with inkjet printer and metallic inks “at home”
- Customizable: similar to the concept of FPGAs
- Robust: programmability to overcome yield problem

Mapping algorithms for logic array are still missing.
Pseudo-CMOS logic array cell

<table>
<thead>
<tr>
<th>Logic cell</th>
<th>Program method</th>
<th>Unused TFTs</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAND/INV1</td>
<td>P₂-P₄, P₅-P₈, P₃/7-V_DD</td>
<td>-</td>
</tr>
<tr>
<td>NOR/INV2</td>
<td>P₂-P₃, P₅-P₇</td>
<td>-</td>
</tr>
<tr>
<td>INV3</td>
<td>P₃/7-V_DD</td>
<td>M₁, M₄</td>
</tr>
<tr>
<td>INV4</td>
<td>P₂-P₄, P₅-P₈</td>
<td>M₂, M₅</td>
</tr>
</tbody>
</table>

Qinghang Zhao et al., DAC 2016
Pre-fabricated wires (GWs) ensure the routability.

Printed wires (PWs) reduce the area overhead.

Qinghang Zhao et al., DAC 2016
Array architecture comparison

- Noise margin is improved by pseudo-CMOS logic with unipolar devices
- Compared with IGA, 80% area is reduced with pseudo-CMOS logic array.
- Compared with SOTG, the routability is ensured.

NM of zero-$V_{GS}$ and pseudo-CMOS inverter

Area and routability comparison with IGA and SOTG

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TFT</td>
<td>Area $^1$</td>
<td>TFT</td>
</tr>
<tr>
<td>RO15</td>
<td>60</td>
<td>1344</td>
<td>90</td>
</tr>
<tr>
<td>Counter4</td>
<td>200</td>
<td>4375</td>
<td>144</td>
</tr>
<tr>
<td>MUL3</td>
<td>414</td>
<td>20400</td>
<td>_2</td>
</tr>
</tbody>
</table>

$^1$ mm$^2$. $^2$ not routable.

Qinghang Zhao et al., DAC 2016
The defects and performance of TFTs/array cells are identified through test & characterization, hence improving circuit yield.
Mapping problem formulation

- **Assumption**
  - Logic array has been tested and characterized
  - Strain & temp condition are pre-determined

- **Input**
  - Gate level circuit netlist represented by a graph $G(V, E)$
  - Parameters of logic array including
    - Array sizes and H-wire number
    - Size of pads and vias, pitch between pads
    - Capacity of each rows $|R_i|$ determined by test
    - Mobility weights $w_{ij}$ evaluated by strain and temperature ($w_{ij}$ shows average mobility of one cell)
Problem formulation in 2 steps

- **Inter-row problem (clustering)**
  - Minimum Cut: Given $G = (V, E)$, partition $V$ into $k$ disjoint sets $\{G_1, ..., G_k\}$ such that the sum of $e(G_i, G_k)$, i.e., the number of edges in $\{(x, y) \in E | x \in G_i, y \in G_k\}$, is minimized
  - Capacity Constraints: $|G_i| < |R_i|$

- **Intra-row problem (mapping)**
  - MAP: $G \rightarrow R, MAP(g_i) = r_j, \forall g_i \in G, \exists r_j \in R$
  - Maximum flow: find a mapping function to maximum circuit performance
  - Minimum cost: find a mapping function to minimize routing cost

Goal: Maximum circuit performance with temp & strain consideration and enable routability.
Algorithm for inter-row clustering

Add image

Simply minimize cut cost Spectral clustering

| 𝑅𝑅1 | =5
| 𝑅𝑅2 | =3

Goal of spectral clustering:

\[
\text{Minimize RatioCut} = \sum_{i=1}^{k} \frac{\text{cut}(A_i, \overline{A_i})}{|A_i|}
\]

Adjusted spectral clustering

1. Describe circuit with undirected graph
2. Compute normalized graph Laplacians
3. Compute first \( k \) eigenvectors as \( U \in R^{n \times k} \)
4. Let \( y_i \) be the \( i \)-th row of \( U \), cluster points \( y_i \) with \( k \)-means algorithm into \( k \) clusters
5. Adjustment according to row capacity, i.e., remove one farthest point in one cluster to another if needed

Q: How to improve circuit performance with mobility variation
Algorithm for intra-row mapping

Critical path (cp):
1 → 2 → 4 → 6 → 5 → 7 → 8
1 → 3 → 4 → 6 → 5 → 7 → 8

Sub-critical path (sp):
1 → 2 → 4 → 5 → 7 → 8
1 → 3 → 4 → 5 → 7 → 8
1 → 2 → 4 → 6 → 7 → 8
1 → 3 → 4 → 6 → 7 → 8

Define important degree of gate $g_i$

$$d(g_i) = a|\{cp_k|g_i \in cp_k\}| + b|\{sp_k|g_i \in sp_k\}|, a > b$$

$$d(g_1) = d(g_4) = d(g_7) = d(g_8)$$
$$> d(g_5) = d(g_6) > d(g_2) = d(g_3)$$

Key idea: improve circuit performance with limited routing resource
Algorithm flow and a design case

Circuit netlist, Logic array information

Initial static timing analysis

Mechanical and thermal aware mapping algorithm

Inter-row Mapping
- Spectral clustering
- Adjustment

Intra-row Mapping
- Simple matching algorithm
- Adjustment

Mobility and routing aware mapping

Array test, temp & strain evaluate...

(Sub-)Critical path in circuit

Inter-row step: clustering according to capacity

Intra-row step: mapping according to mobility variation

Adder circuit with 16 gates map to a 2x8 logic array

(a) Circuit input

(b) Inter-row mapping

Cluster 1 (9 cells): remove one cell

Cluster 2

Nearest cell in cluster 2

(c) Intra-row mapping

Simple matching

Adjustment: 2 H-wires (7-8, 9-10)
Experiment setup

- Level 40 HP TFT model
- Printed & all solution process
- VSS=-10 & VDD=5V
- p-type
- μ: 0.6cm²/Vs

The structure and photo of fabricated SAM OTFT

Mobility distribution in experiment

Mobility effect on inv cell delay
Experiment

Comparison with [9] (DAC2017’s work) and this work

<table>
<thead>
<tr>
<th>Circuit</th>
<th>H-wires</th>
<th>HPWL($\times 10^5 \mu m$)</th>
<th>Critical Path Delay($\mu s$)</th>
<th>PI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Adder2</td>
<td>1 3</td>
<td>0.53</td>
<td>0.58</td>
<td>31.14</td>
</tr>
<tr>
<td>Counter4</td>
<td>4 8</td>
<td>1.11</td>
<td>2.70</td>
<td>76.12</td>
</tr>
<tr>
<td>Mul3</td>
<td>4 13</td>
<td>8.56</td>
<td>10.92</td>
<td>69.20</td>
</tr>
</tbody>
</table>

*Performance Improvement (PI): $\left(\frac{\text{Delay of [9]}}{\text{Delay of this work}} - 1\right) \times 100%$

*HPWL: Half perimeter wire length of printed wires
*VDD/VSS/GND/INPUT/OUTPUT terminals are not included in H-wire number

Information of benchmark circuits

<table>
<thead>
<tr>
<th>Circuit</th>
<th># of INV</th>
<th># of NAND</th>
<th># of NOR</th>
<th>Array size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Adder2</td>
<td>8</td>
<td>4</td>
<td>4</td>
<td>$2 \times 10$</td>
</tr>
<tr>
<td>Counter4</td>
<td>8</td>
<td>24</td>
<td>4</td>
<td>$4 \times 10$</td>
</tr>
<tr>
<td>Mul3</td>
<td>36</td>
<td>33</td>
<td>12</td>
<td>$9 \times 10$</td>
</tr>
</tbody>
</table>

*#: Number of

Trade off the routing resources and circuit performance effectively

Implement of 3-bit multiplier with different H-wire numbers

Nearly same HPWL of printed wire but 38% PI
Conclusion

- Architecture of pseudo-CMOS logic array based on TFTs is reviewed
- 2-steps mapping algorithms considering mechanical strain and temperature effect on TFTs are proposed for a pseudo-CMOS logic array
  - Inter-row clustering algorithm to overcome the defected cells effect
  - Intra-row mapping algorithm to deal with the mobility variation problem
- Experiment shows this work can effectively improve circuit performance while enable routability


Q & A