

Collaborative Accelerators for In-Memory MapReduce on Scale-up Machines

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Data-intensive applications challenges



Data-intensive applications challenges



Challenge #1 :



- Complex parallel programming models (e.g. Pthreads, OpenCL, OpenMP)

Solution: ↓

- Simplified parallel programming models (e.g. MapReduce)

Data-intensive applications challenges



Challenge #1 :

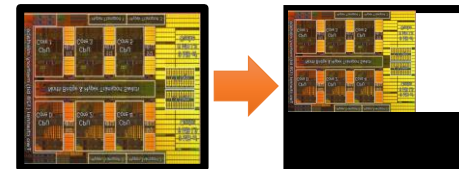


- Complex parallel programming models (e.g. Pthreads, OpenCL, OpenMP)

Solution: ↓

- Simplified parallel programming models (e.g. MapReduce)

Challenge #2 :



New features
Dark silicon

- Inefficiency in new hardware systems due to poor device scaling

Solution: ↓

Accelerator-rich architectures

MapReduce – WordCount example

Input

car bus
car car
bus

car bus
bus car
bus

car car
car car

MapReduce – WordCount example

Input

Split

car bus
car car
bus

car bus
car car
bus

car bus
bus car
bus

car bus
bus car
bus

car car
car car

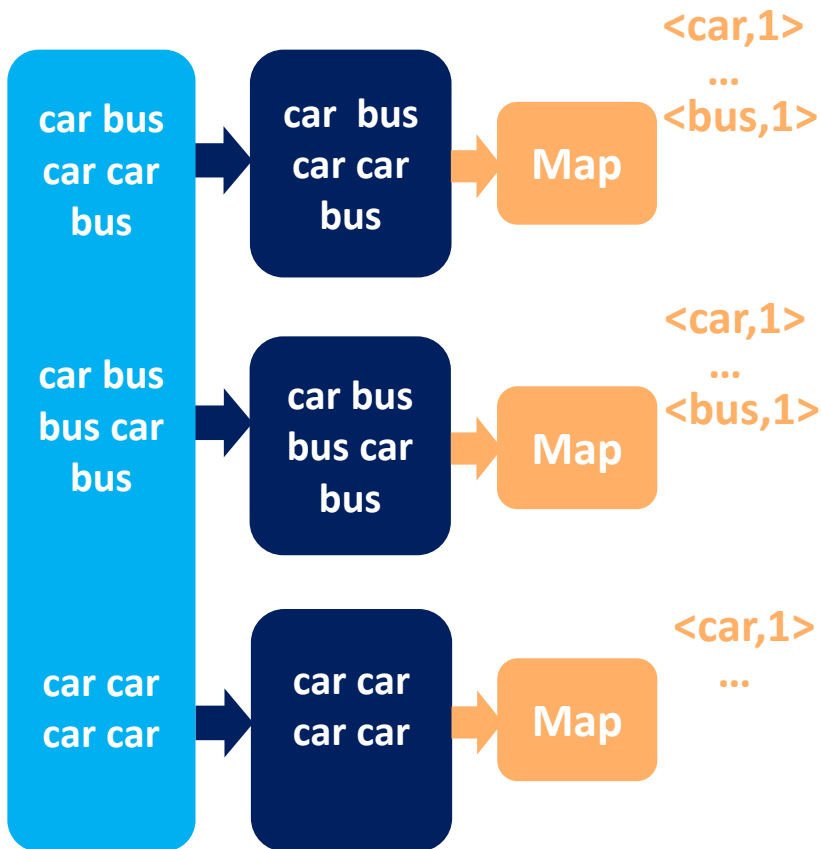
car car
car car

MapReduce – WordCount example

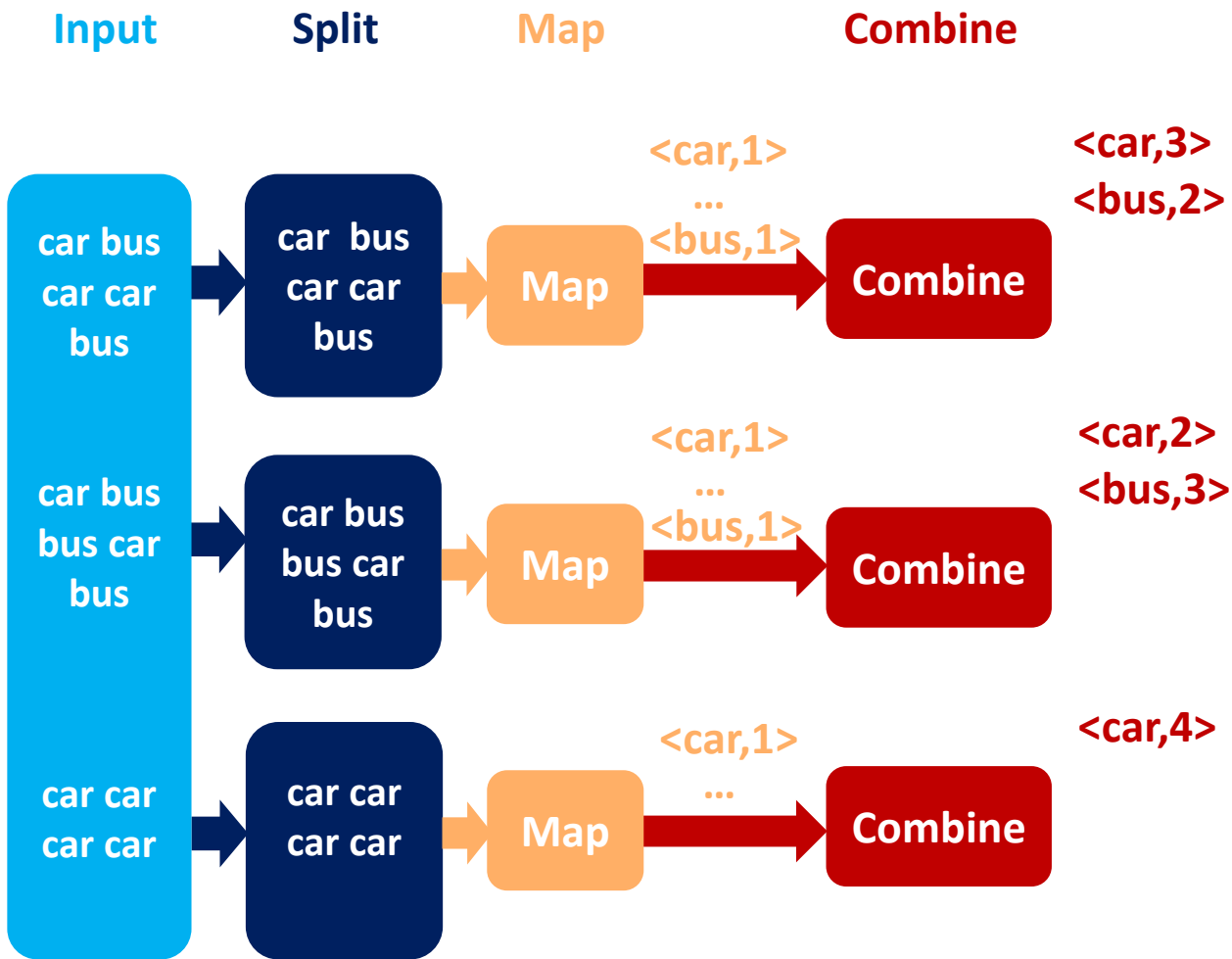
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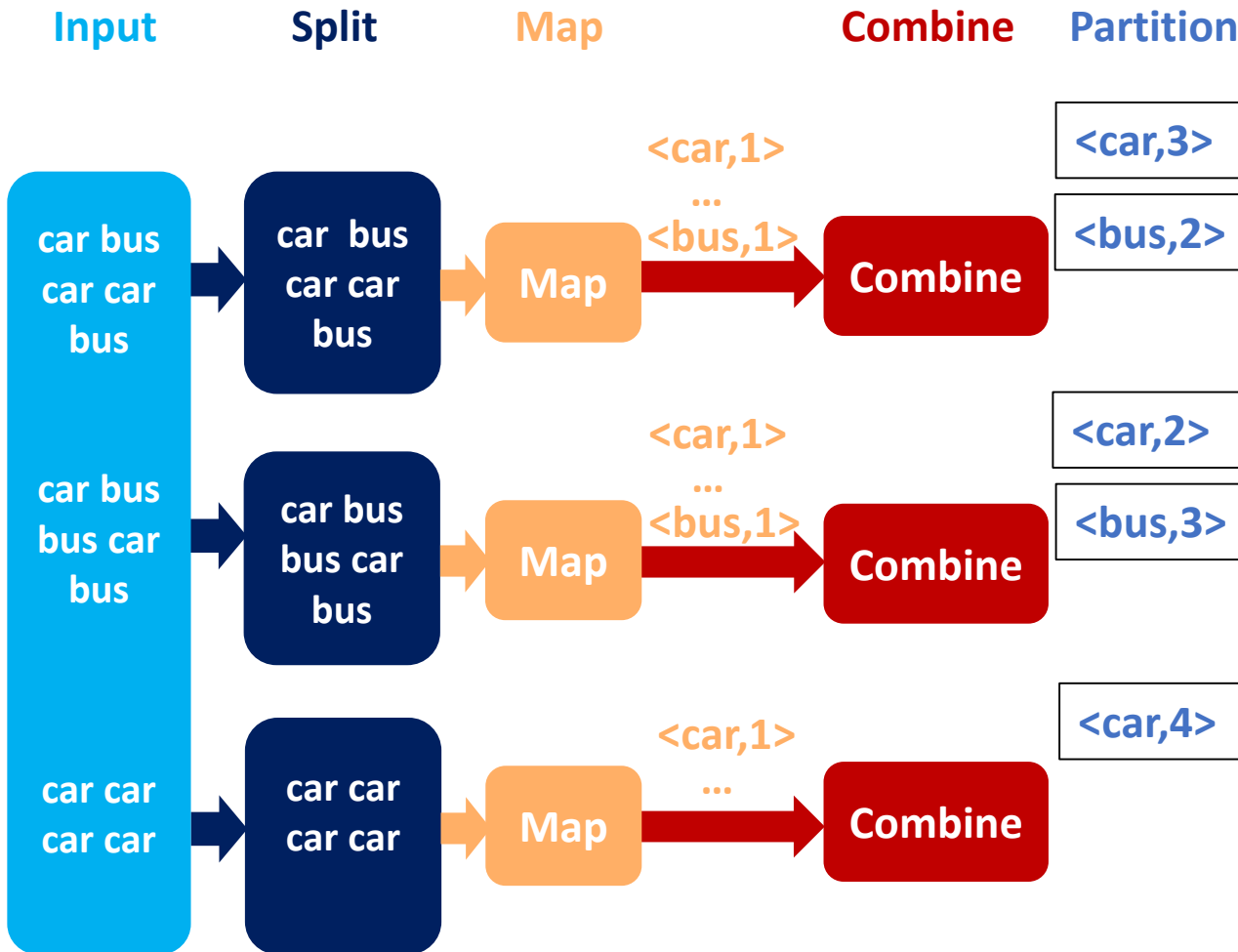
Map



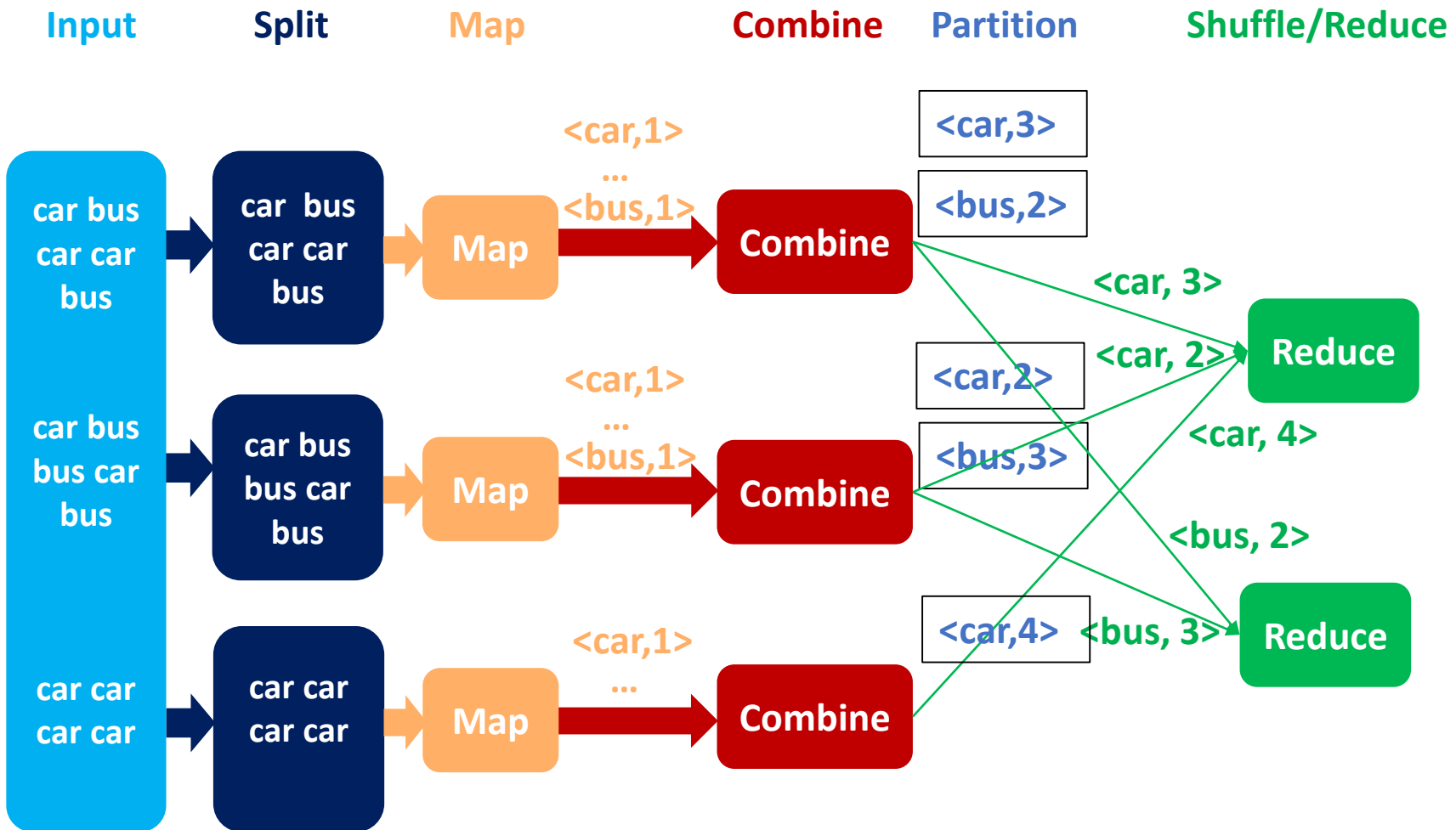
MapReduce – WordCount example



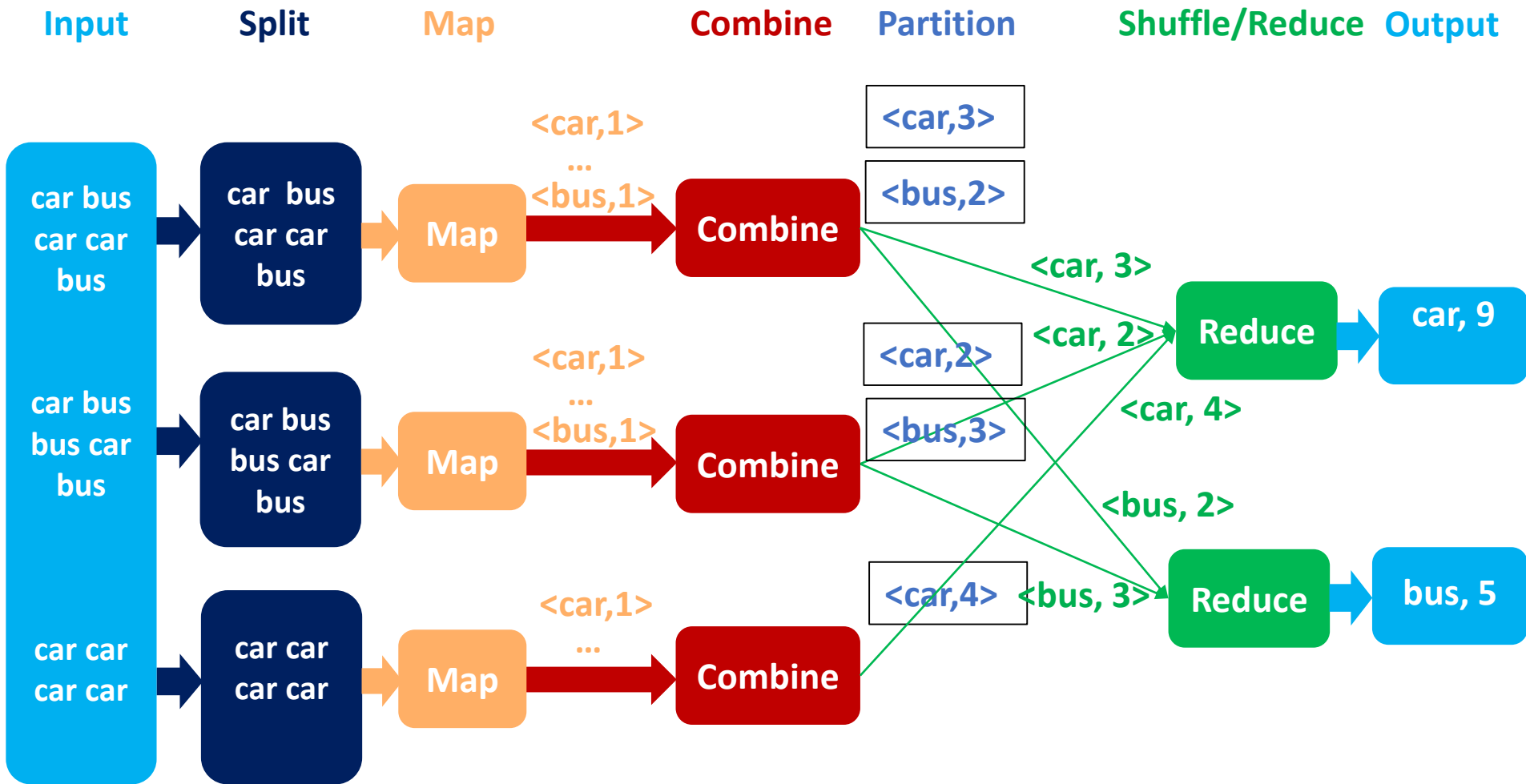
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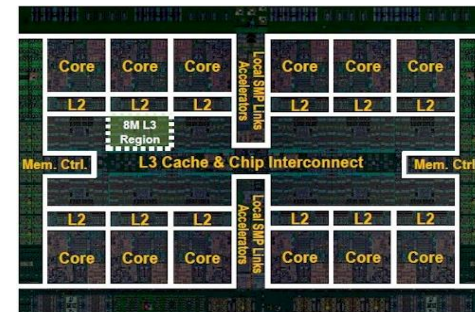
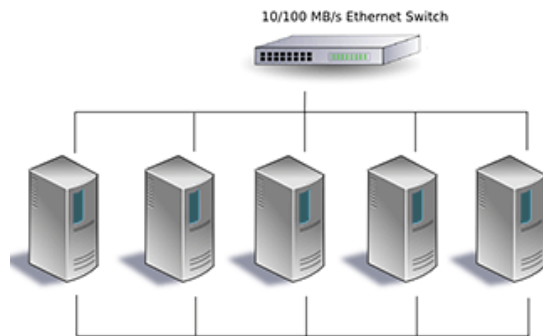
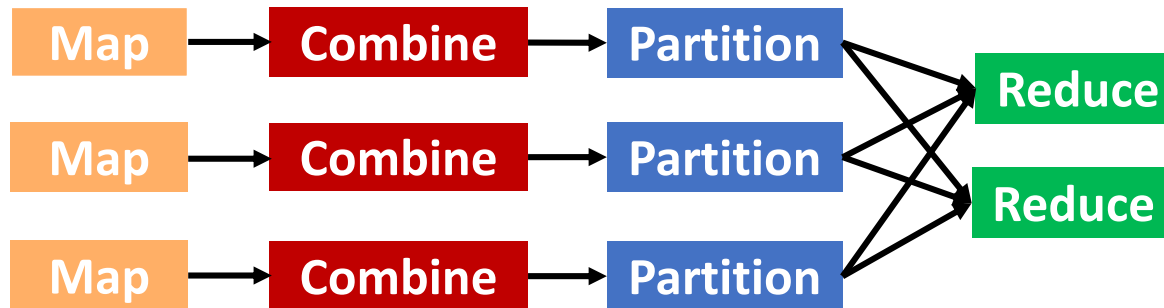
MapReduce – WordCount example



MapReduce – WordCount example



MapReduce implementations

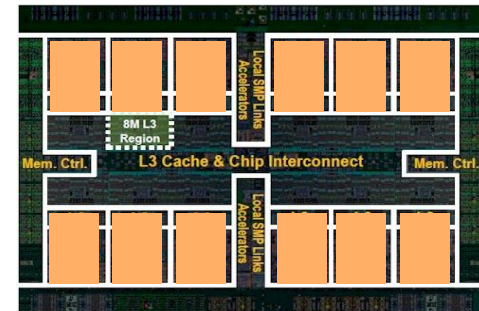
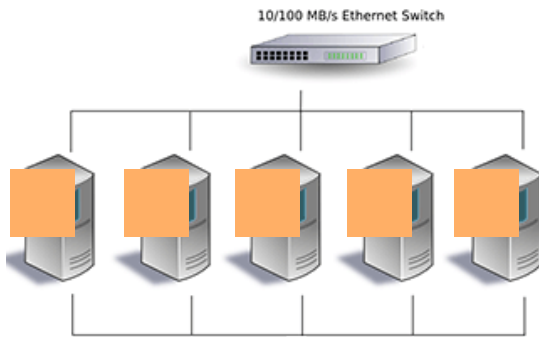
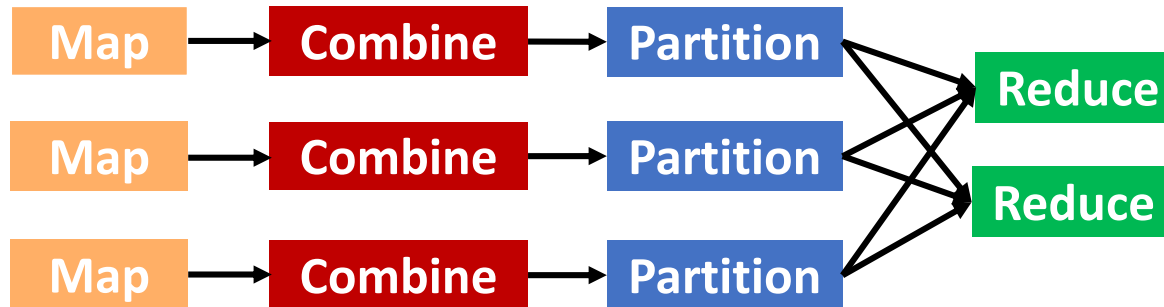


Scale-out:
Hadoop @ Yahoo

GPU:
Mars @ HKUST

CMP/Scale-up:
Phoenix++ @ Stanford

MapReduce implementations

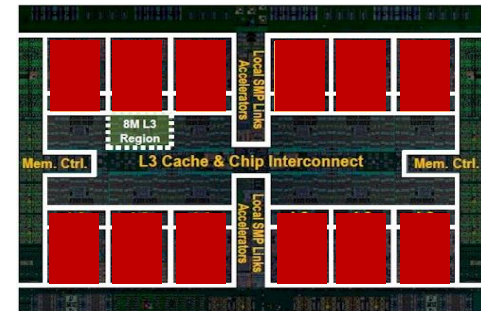
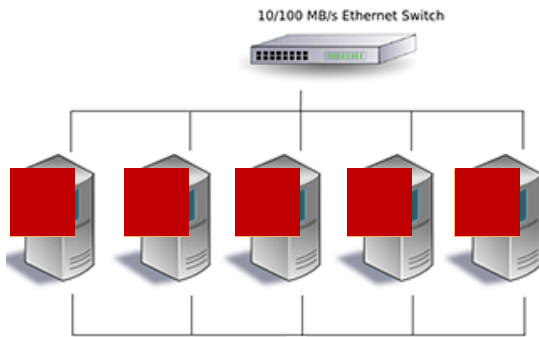
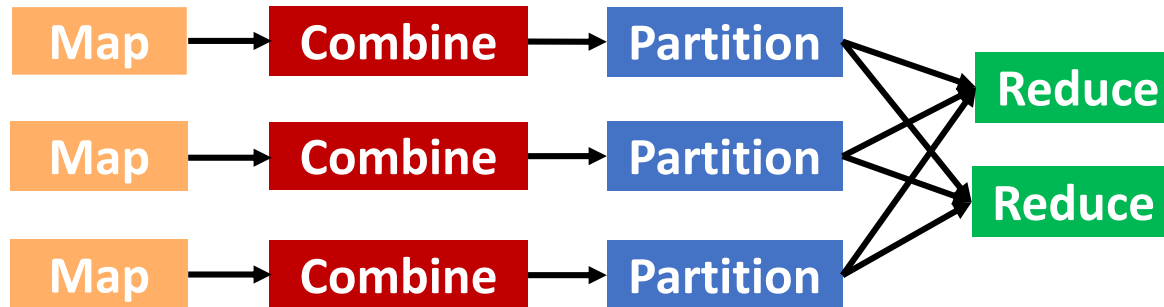


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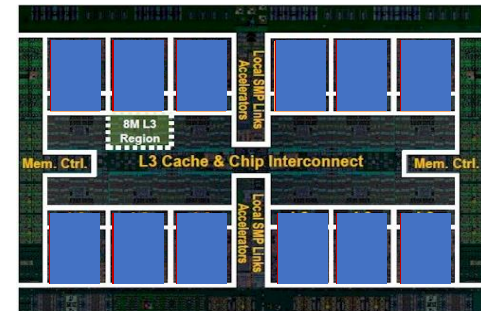
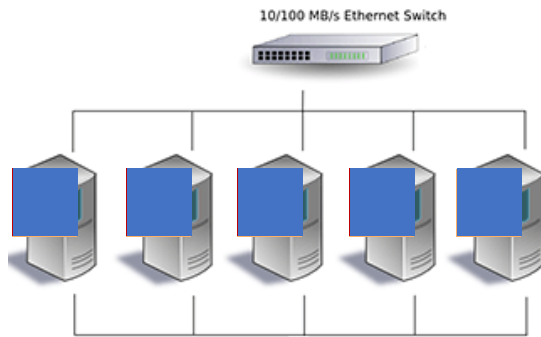
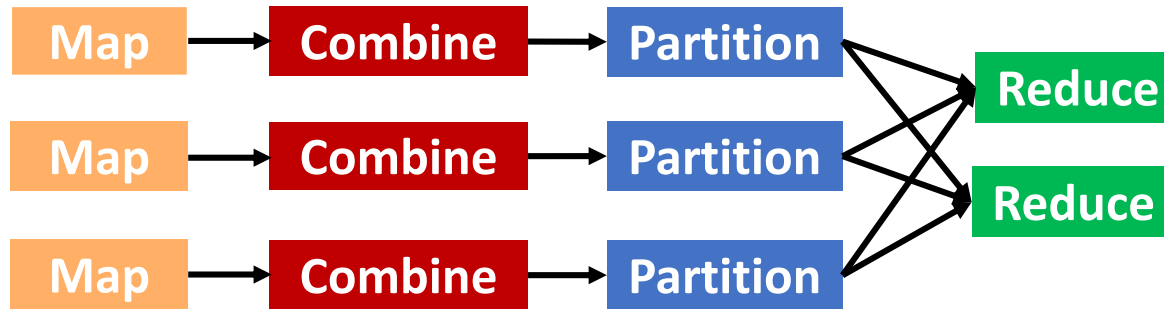


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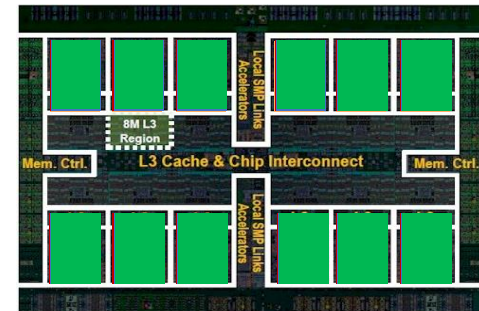
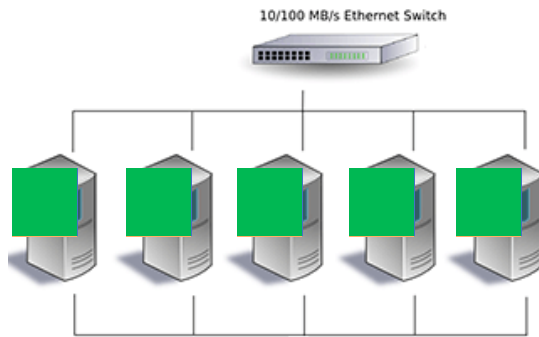
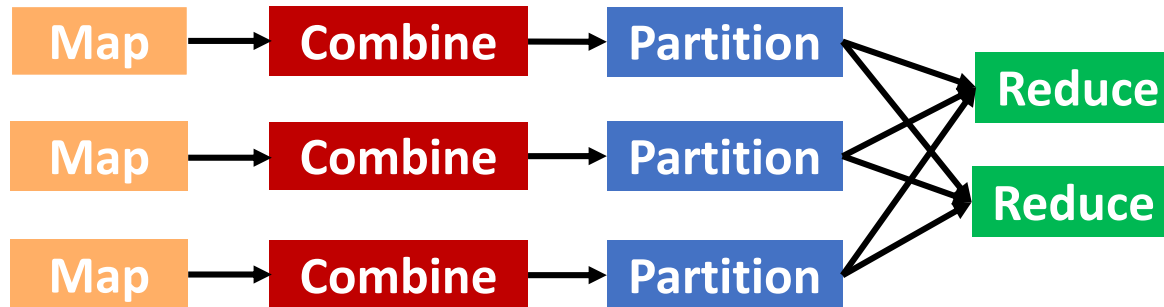


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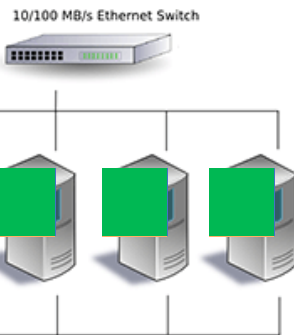
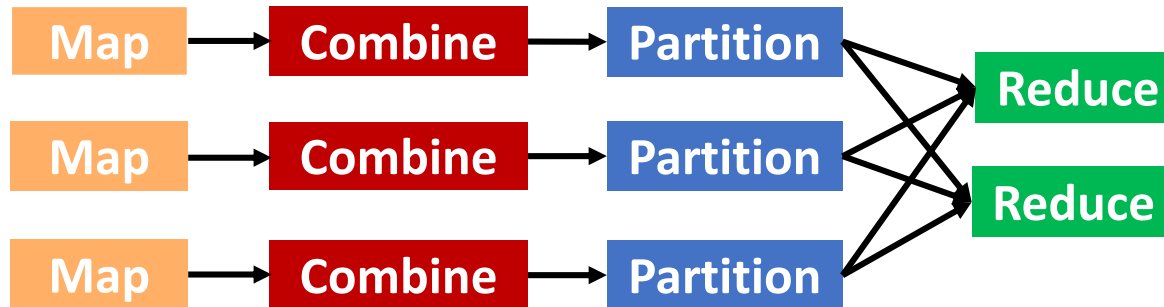


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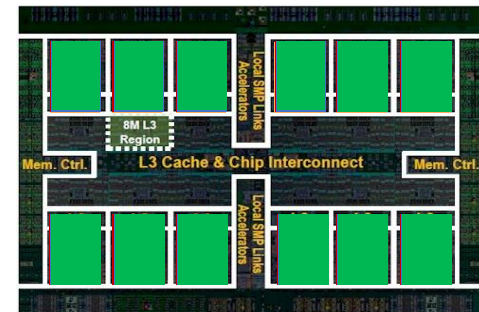
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MapReduce implementations



focus of this work



Scale-out:
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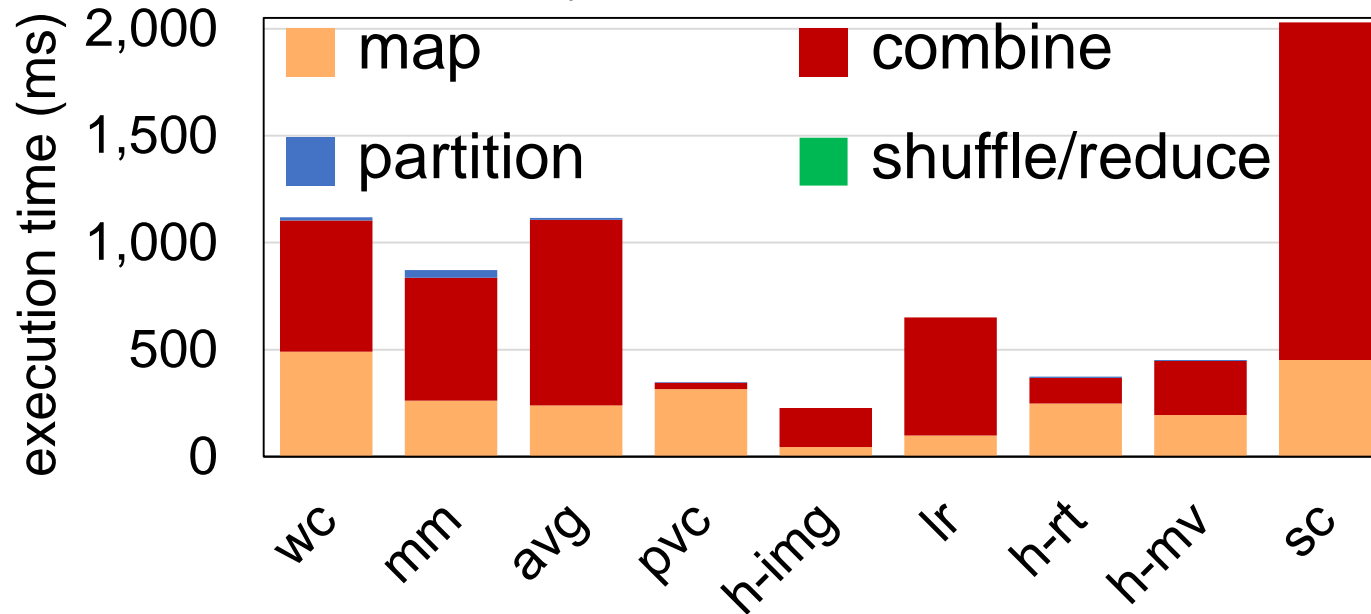
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Phoenix++ studies

- Execution breakdown

16-core, Intel Xeon E5-2630 Server



Workload description

wc: word count

mm: min-max

avg: average

pvc: page view count

h-img: histogram image

h-rt: histogram user

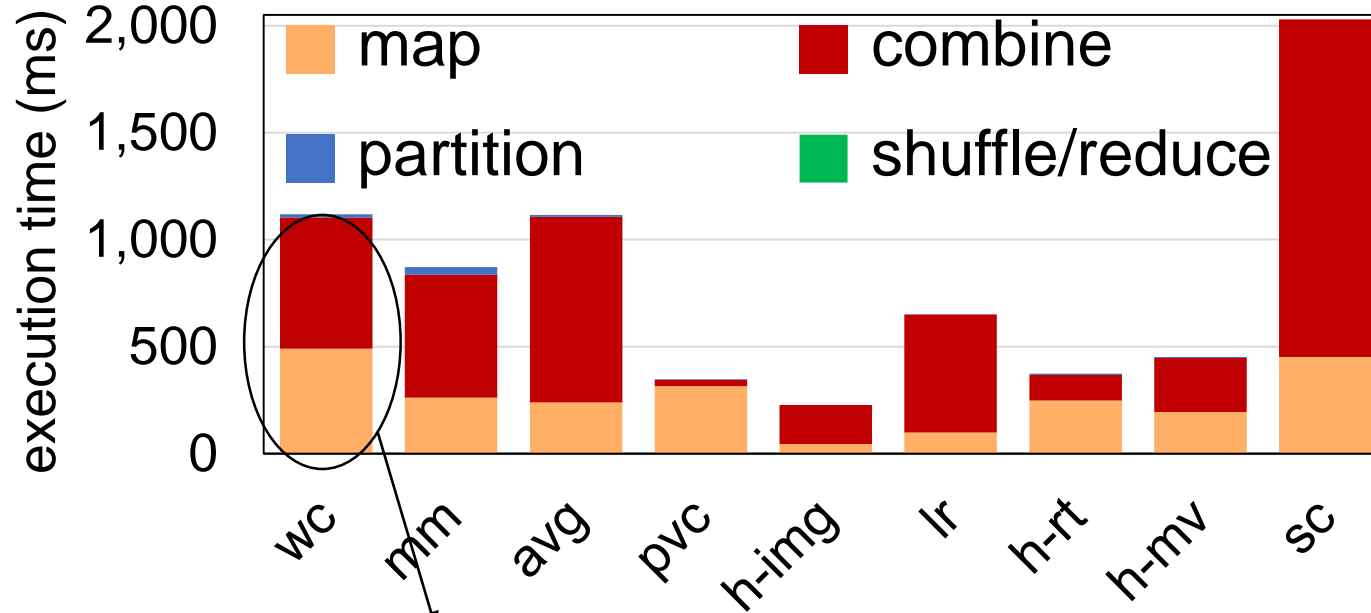
h-mv: histogram movie

sc: sequence count

Phoenix++ studies

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map & combine dominate

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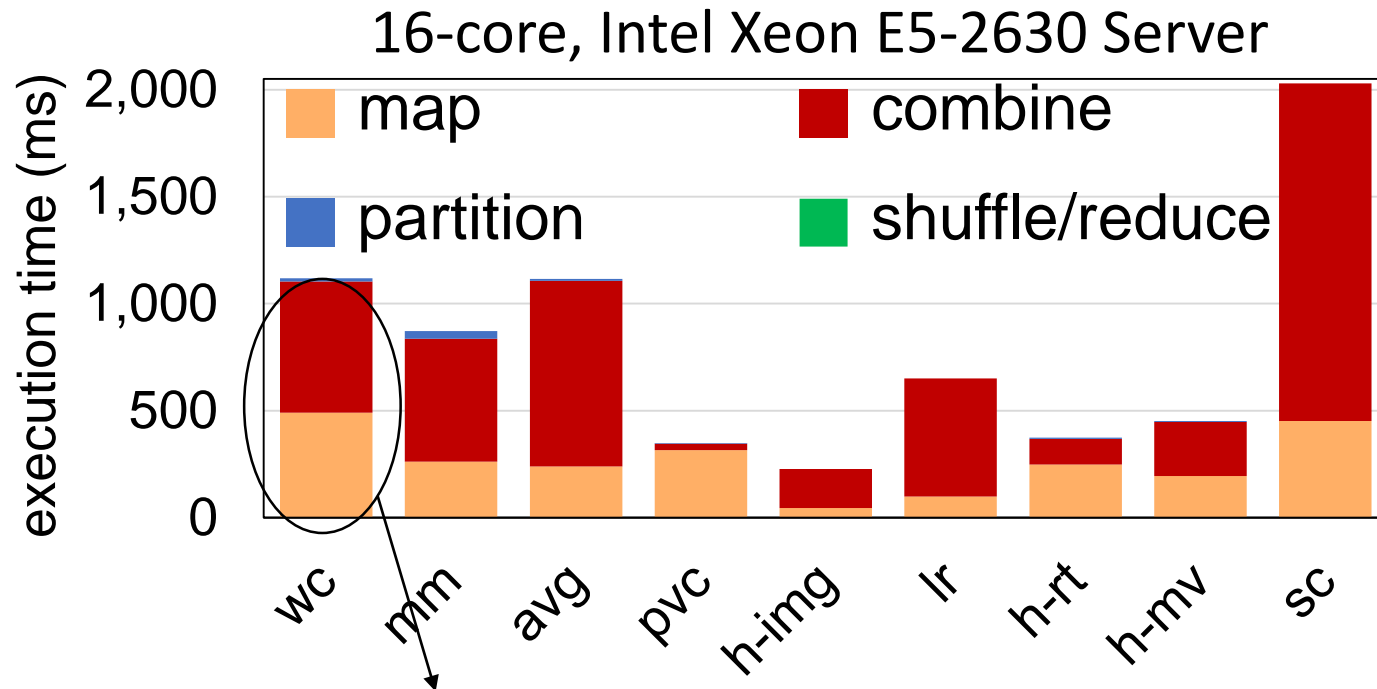
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map & combine dominate

- Inefficiencies:

- **Serial execution** of map and combine phases
- **Inefficient key-value lookup** during combine phase

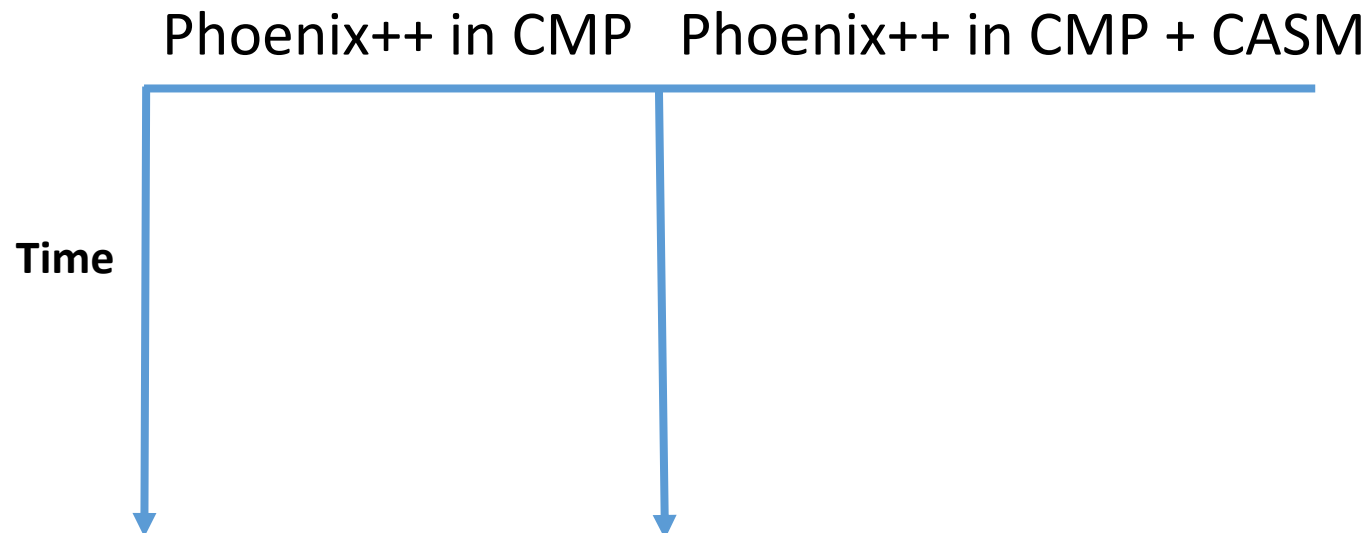
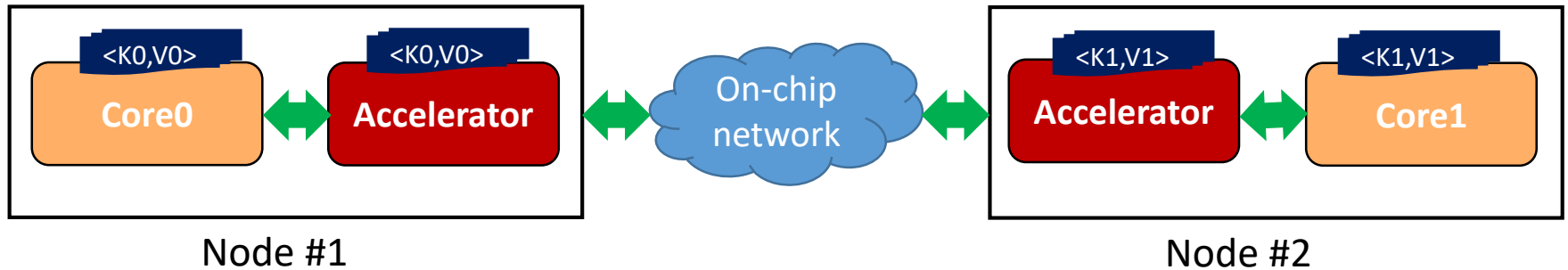
CASM overview

- Execution flow



CASM overview

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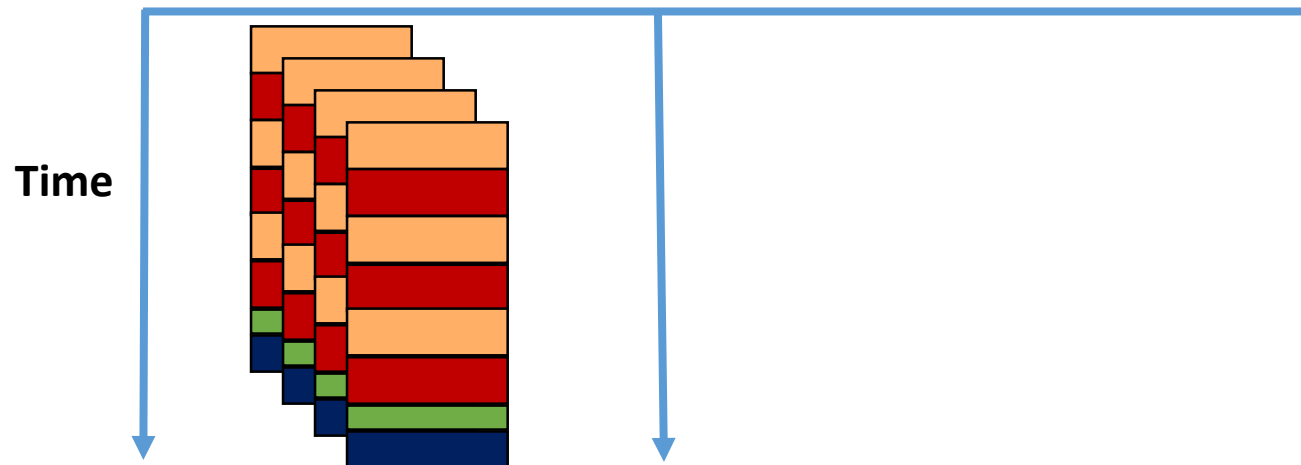


CASM overview

- Execution flow



Phoenix++ in CMP Phoenix++ in CMP + CASM

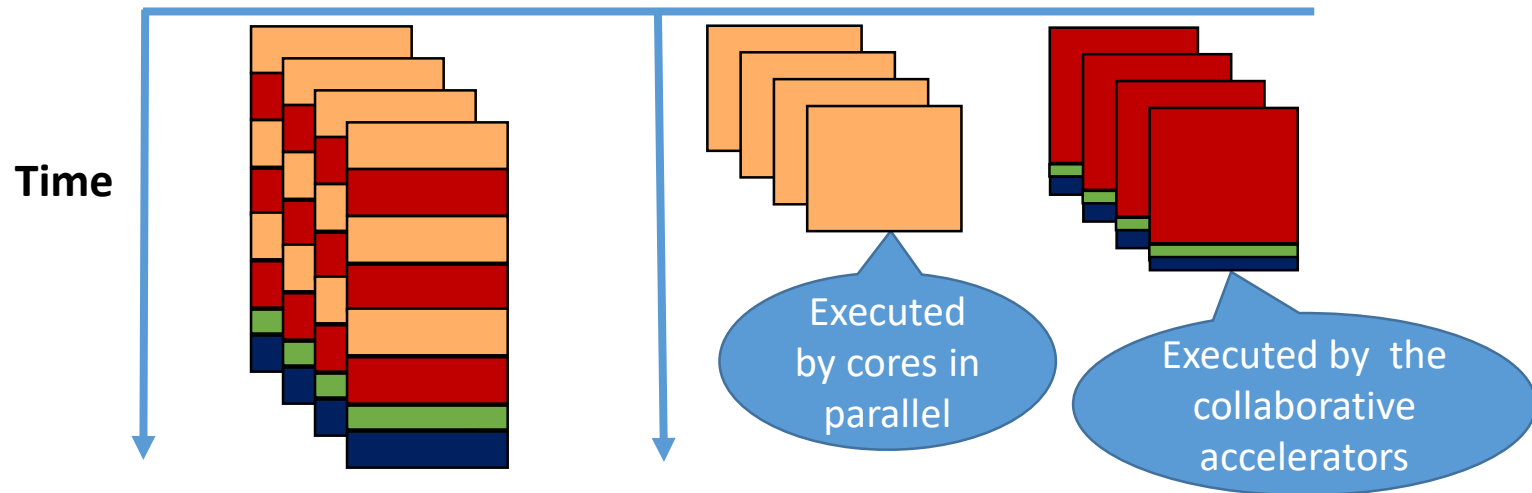


CASM overview

- Execution flow

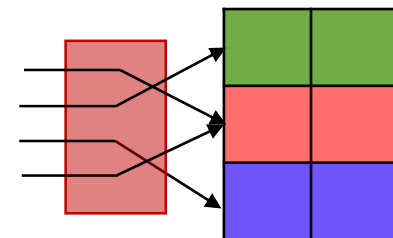
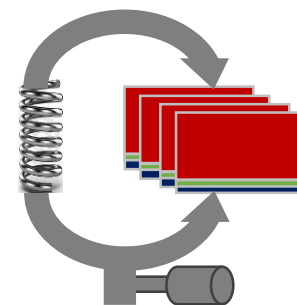
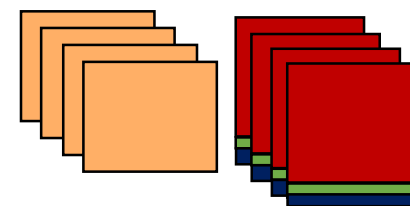
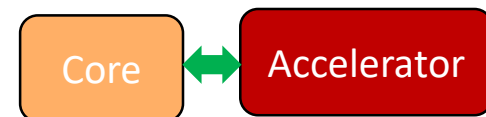


Phoenix++ in CMP Phoenix++ in CMP + CASM



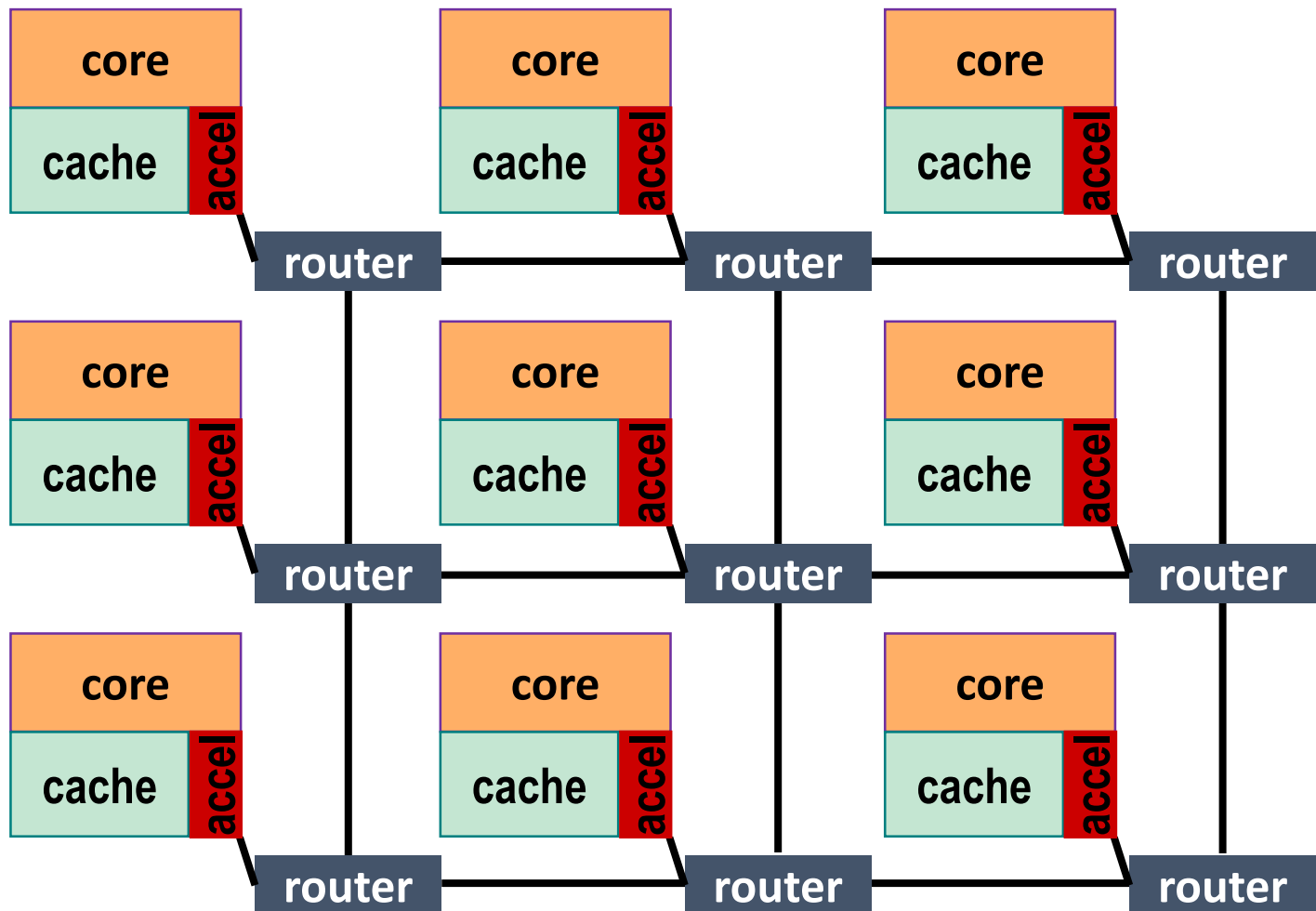
Key contributions

- **Scalable** and **collaborative** accelerators
- **Parallel execution** of map and combine phases
- **Faster execution** of combine phase by the accelerators
- **In-hardware hash function**



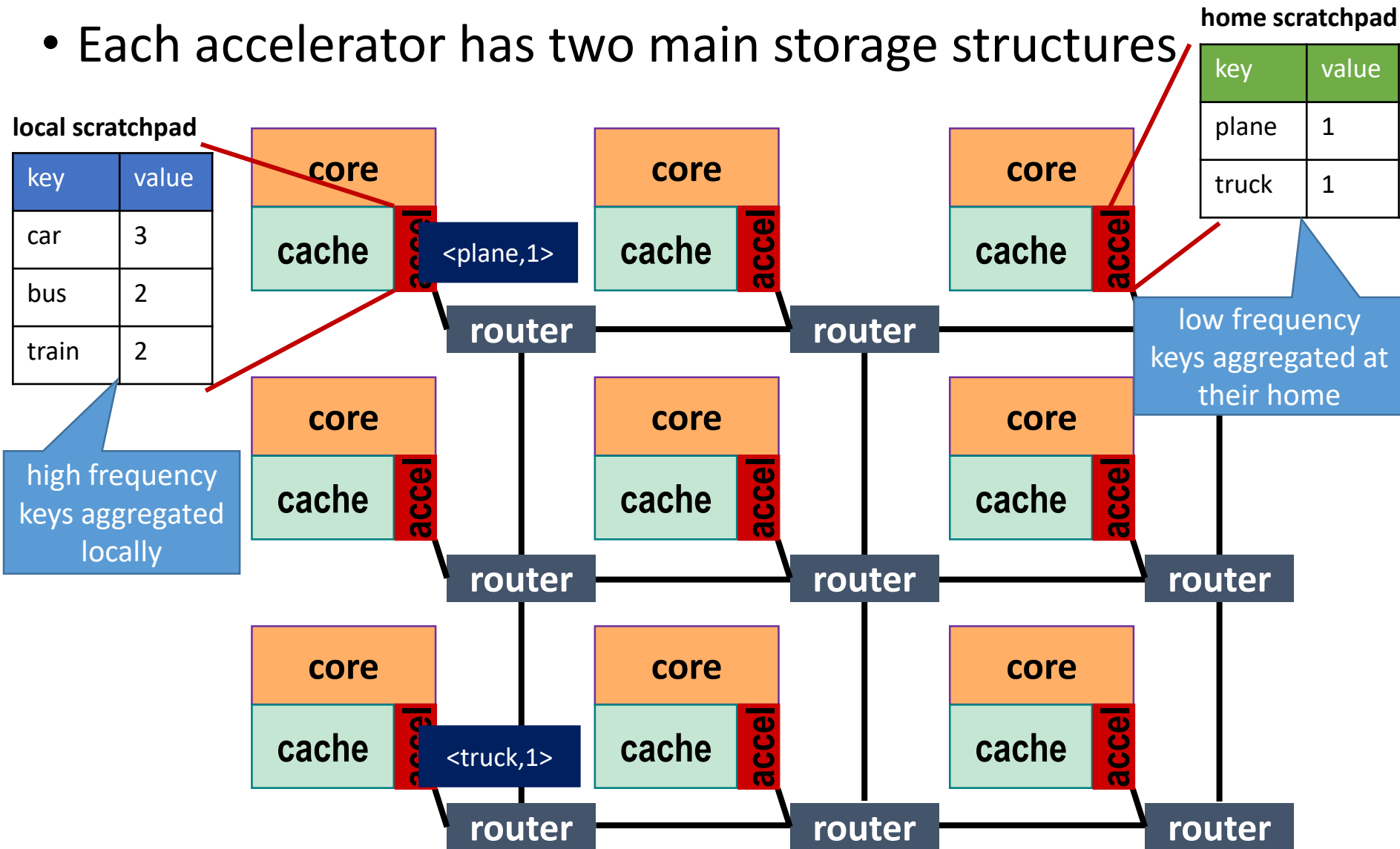
CASM high-level architecture

- Each accelerator has two main storage structures



CASM high-level architecture

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Storage design space exploration

- **Option one: local-only**
key-value pairs replicated across multiple accelerators

accel0		accel1		accel2	
key	value	key	value	key	value
car	3	car	3	car	3
bus	2	bus	2	bus	2
train	2	train	2	train	2

- **Option two: home-only**
a key-value pair exists only in one location

accel0		accel1		accel2	
key	value	key	value	key	value
car	3	train	2	bus	2
truck	1	ship	1	motor	1
plane	1	bicycle	2	rocket	1

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key	value
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truck	1
plane	1
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ship	1
bicycle	2
bus	2
motor	1
rocket	1

unified large memory
with no replication

Storage design space exploration

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storage options	network traffic	memory traffic
local-only	low	high
home-only	high	low
local + home	low	low



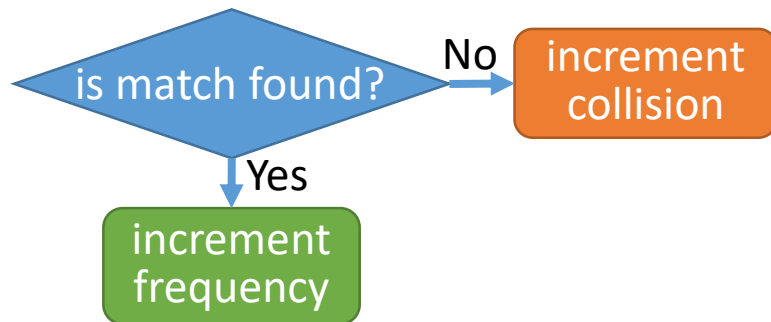
Key-value pair eviction policy

- “frequency” and “collision” bits are stored in scratchpads

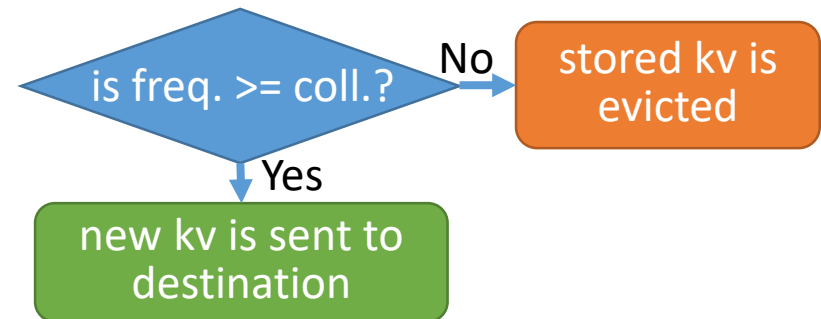
Scratchpad structure:



- Frequency and collision update units:



- Simple heuristic function to identify frequently occurring keys:



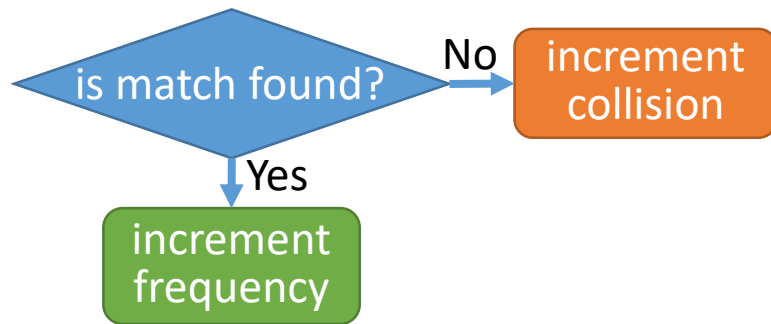
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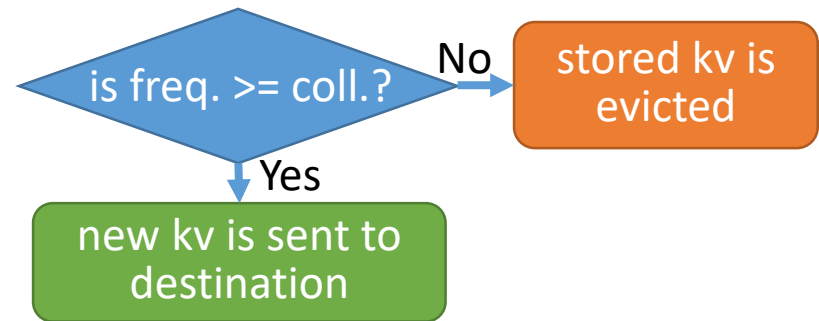
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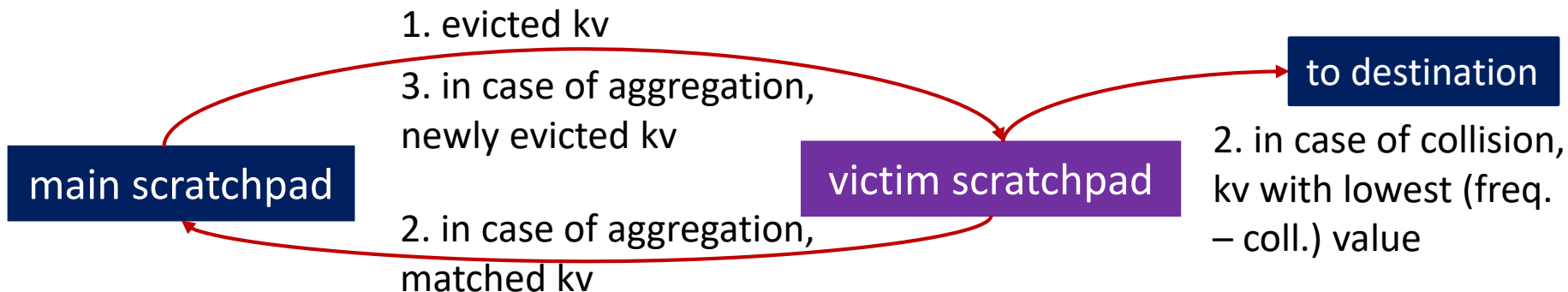
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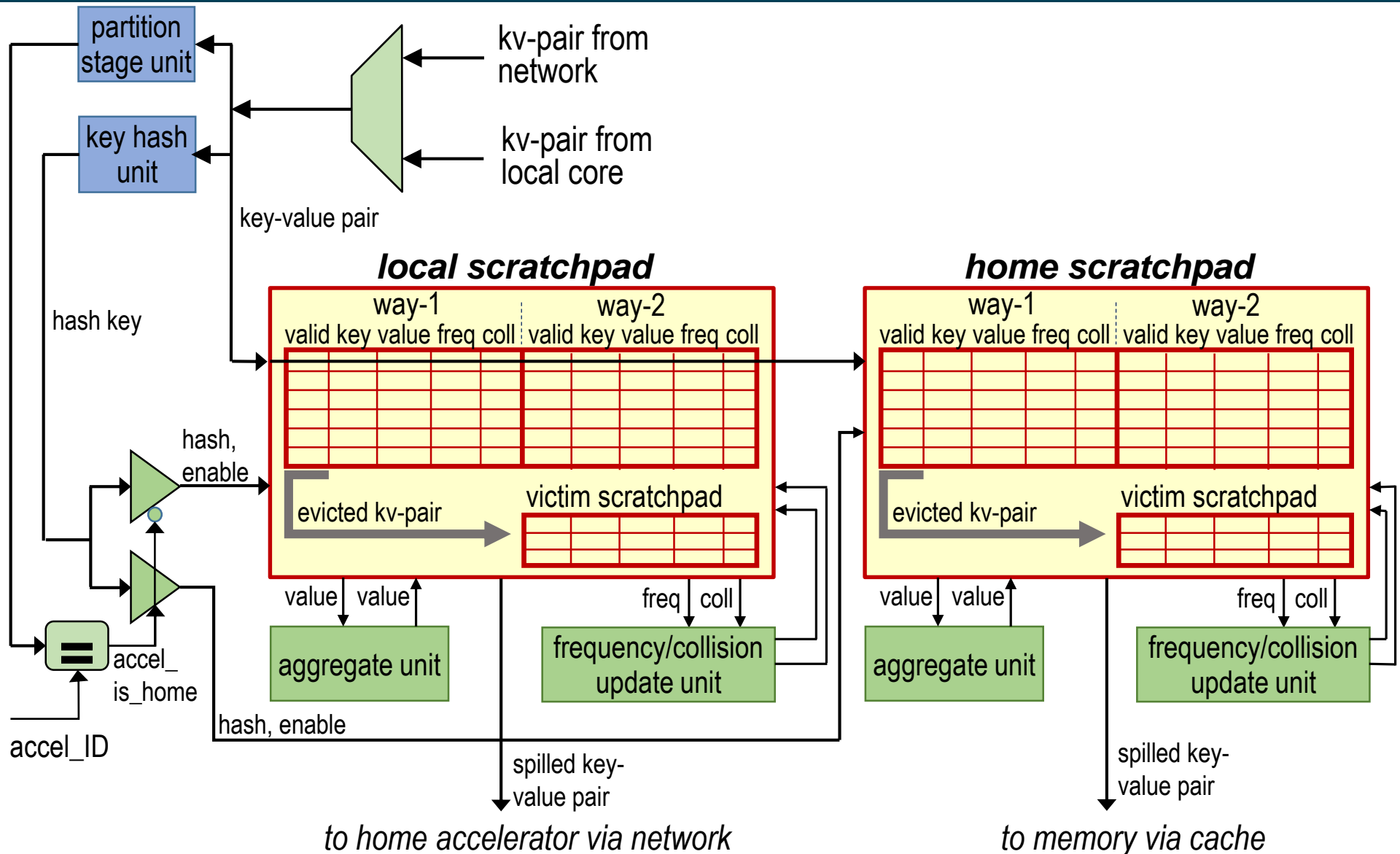
- Simple heuristic function to identify frequently occurring keys:



- Each scratchpad is augmented with victim scratchpad



Accelerator architecture



Experimental framework

- **Scale-up CMP** configuration (Gem5/Garnet)

Parameter	Value
Core	64 cores, OoO, 8-wide
L1 D&I caches	16KB
L2 cache (shared)	128KB per core/slice
Coherence	MOESI directory-based
Memory	4xDDR3-1600, 12GB/s

- **CASM** configuration (Gem5/Garnet)

Parameter	Value
Scratchpad size	16KB
#entries per victim scratchpad	8
Max. key size	64 bits
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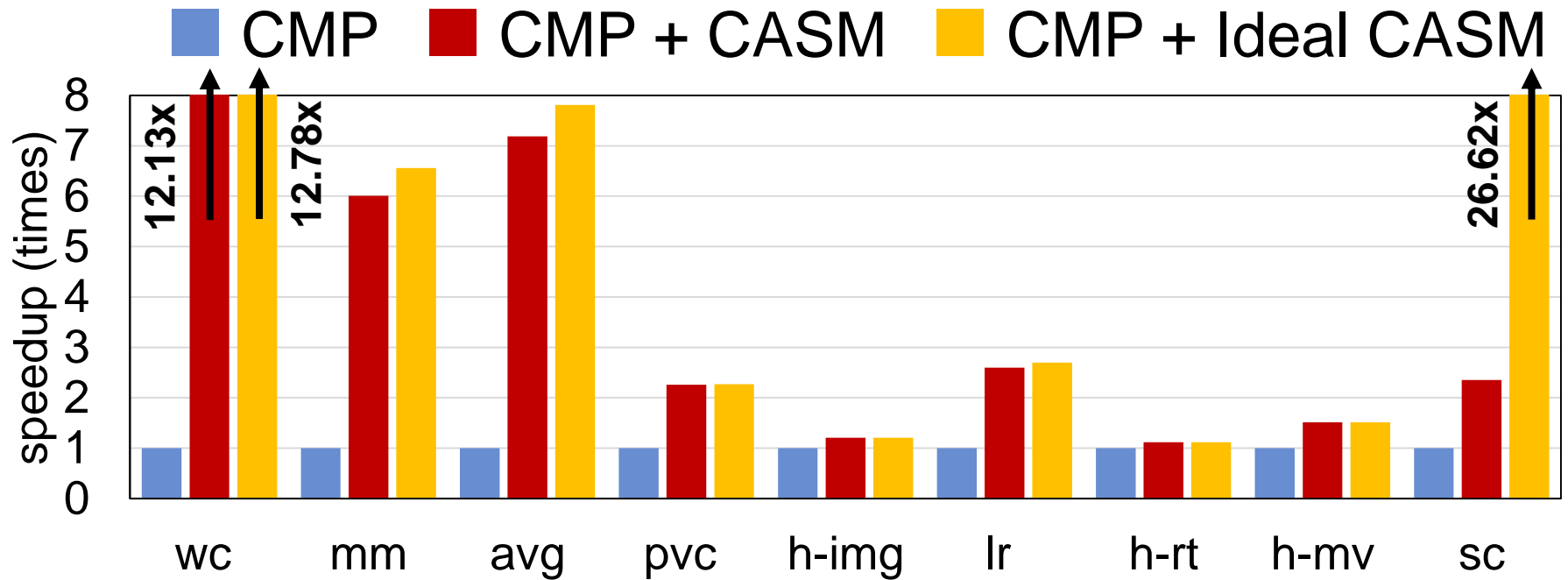
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- **Workload** characteristics

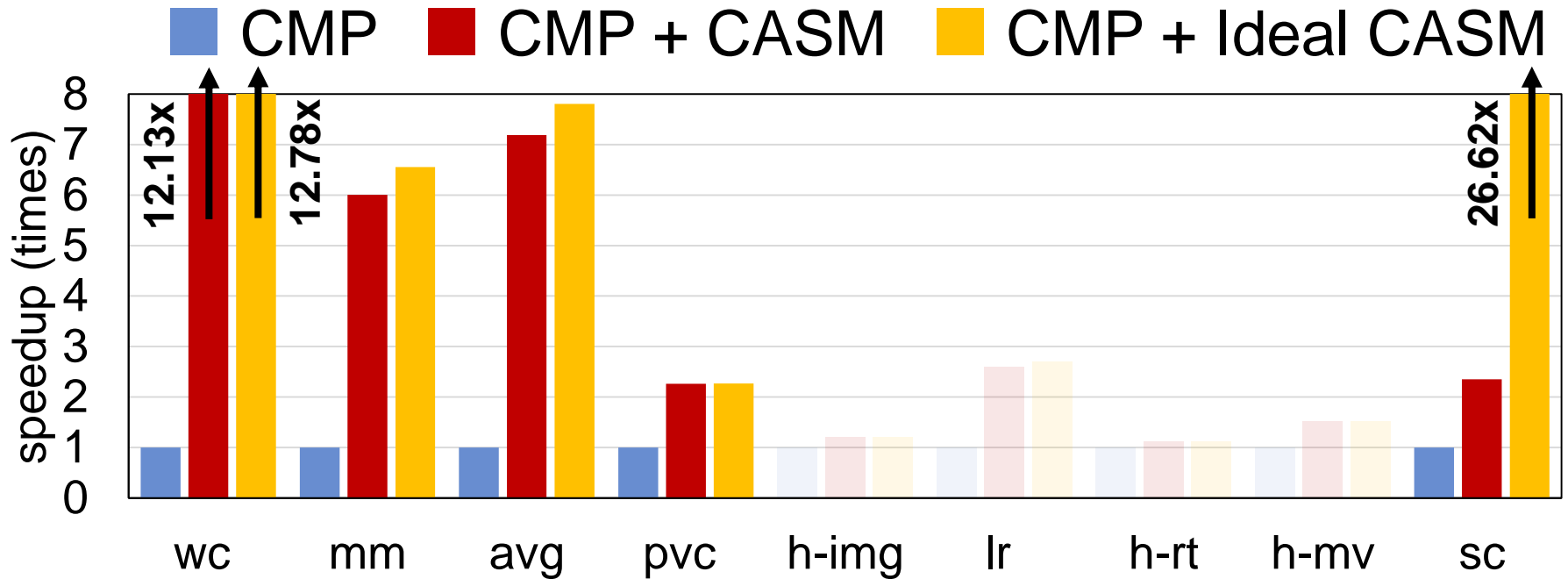
workload	wc	mm	avg	pvc	h-img	lr	h-rt	h-mv	sc
#unique keys	257K	28K	28K	10K	768	5	5	20K	3.5M
cache locality	low	low	low	low	high	high	high	high	low

Performance and energy analysis



- > 4x speedup on average
- > 3.5x energy saving on average

Performance and energy analysis

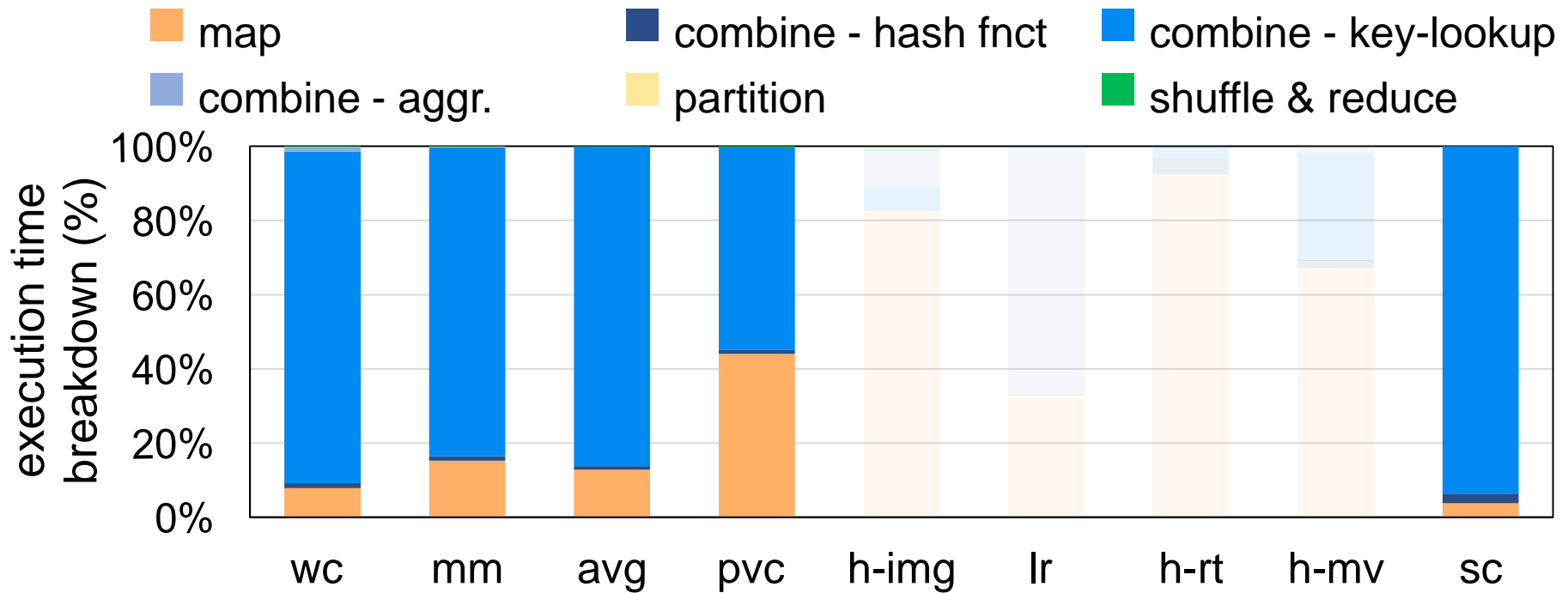


- > 4x speedup on average
- > 3.5x energy saving on average

Large #unique keys & no cache locality → high speedup

Sources of performance benefits

- Mainly due to offloading the **combine phase** to CASM

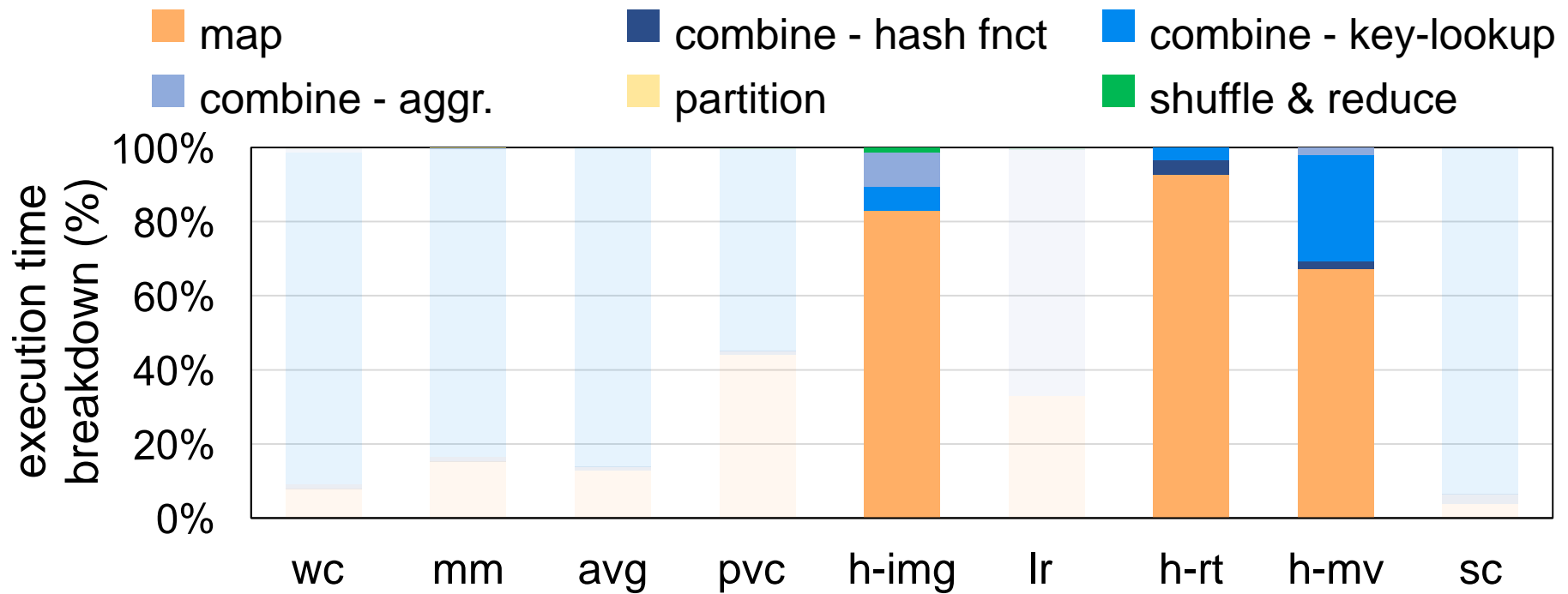


Dominant phase:

combine – key-lookup

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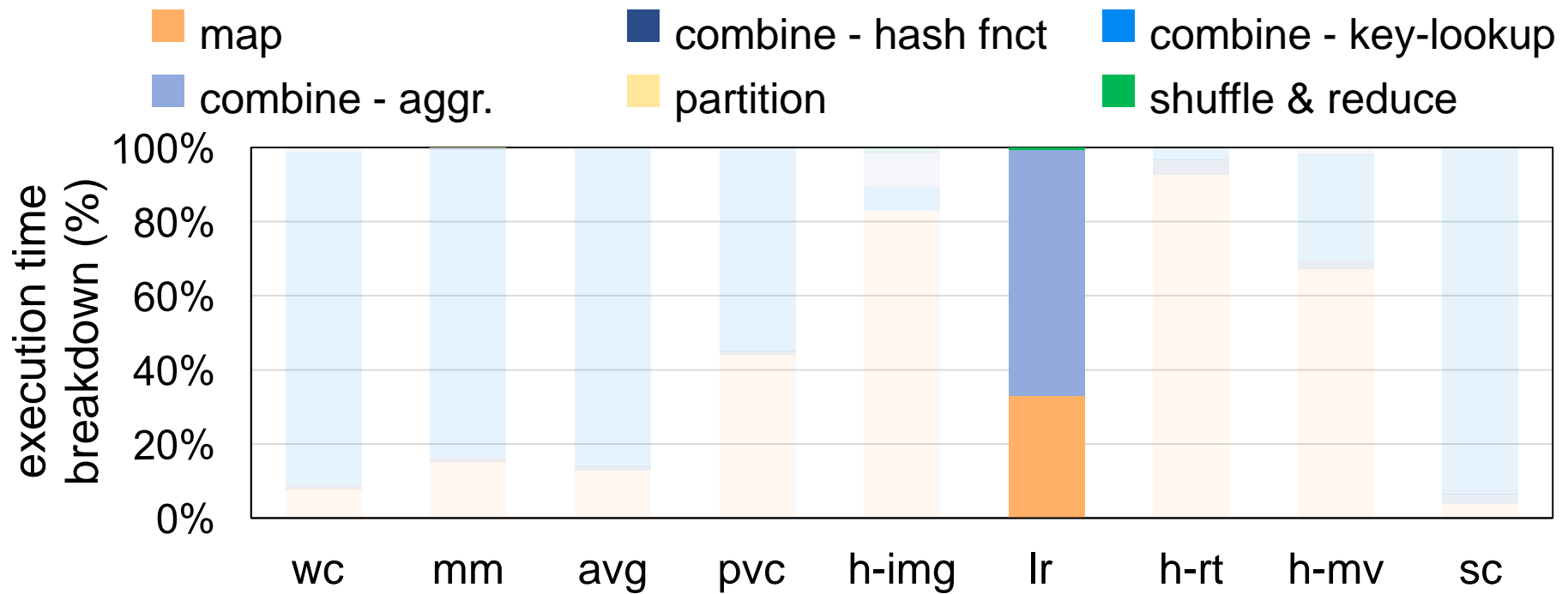


Dominant phase:

map

Sources of performance benefits

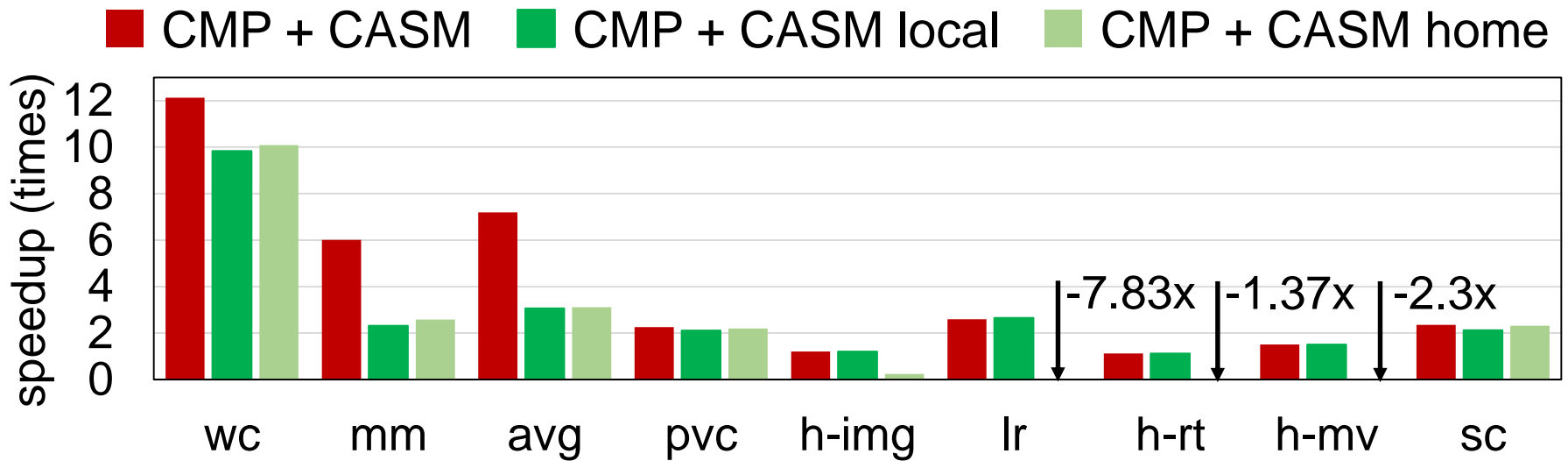
- Mainly due to offloading the **combine phase** to CASM



Dominant phase:

combine – aggregation

Speedup contribution: local vs home



- A hybrid of local and home accelerators provides significant benefits across applications

Conclusion

- MapReduce on scale-up machines suffers from:
 - serial execution of map and combine phases
 - inefficient key-value lookup
- Solution:
 - Parallel execution of map and combine phases
 - Local/home partitioned on-chip storage
 - Aggregation near on-chip storage
- CASM provides:
 - >4x in performance on average
 - >3.5x in energy saving on average
 - < 6% of area overhead