FPGA Laboratory System supporting Power Measurement for Low-Power Digital Design

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FPGA Laboratory System

- The FPGA laboratory systems with Intel Cyclone IV respectively Cyclone V FPGAs are unique in offering:
  - HDMI input and output
  - Power measurement
  - Comparison of two different CMOS technologies
  - Available as a remote lab

- Various design experiments possible, e.g.
  - CMOS technology
  - Temperature
  - Lane Detection
Design Experiment “Lane Detection”

- Original algorithm for lane detection:
  - 24-bit memory
  - 12 x RGB-to-Y

- First optimization of lane detection algorithm:
  - Shifting luminance conversion before line-memory
  - 1 x RGB-to-Y
  - 12-bit memory
Original Algorithm vs. Optimized Algorithm

• Original algorithm for lane detection
  • 41.30 mA core current
  • 49.56 mW core power

• Optimized algorithm for lane detection
  • 30.11 mA core current
  • 36.13 mW core power

\( \Rightarrow \) 27% power saving
\( \Rightarrow \) Identical output image

Power measurement enables understanding of circuit design