# ASP-DAC 2020

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Tuesday, January 14, 2020, 9:00-10:30

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" Skin electronics for continuous health monitoring "

### Keynote III

Wednesday, January 15, 2020, 9:00-10:00

**Jason Cong (University of California, Los Angles)**
" Design automation for customizable computing "

# Keynote Speeches From Industry

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Tuesday, January 14, 2020, 12:00-12:40

**Xiaoning Qi (Alibaba Group)**
" Edge-to-Cloud Innovations for Inclusive AI "

### Keynote IV (Industry)

Wednesday, January 15, 2020, 11:30-12:10

**Zhang Yingwu (GigaDevice Semiconductor (Beijing) Inc)**
" Huge development of RISC-V arising from IOT spurt "

### Keynote V (Industry)

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**Michael Wang (Synopsys)**
" Emulation View of Synopsys Verification Continuum Platform "

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**Lifeng Wu (Empyrean Software)**
" Explore the next tides of EDA "

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Tuesday, January 14, 2020, 10:45-12:00

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## Designers' Forum

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**6D (DF-2): Emerging Design**
Wednesday, January 15, 2020, 15:45-17:00

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Thursday, January 16, 2020, 15:45-17:00

# Tutorials

ASP-DAC 2020 offers attendees a set of two and a half hours intense introductions to specific topics. (This year, each tutorial will be presented once.)

## Tutorial-1: AI Chip Technologies and DFT Methodologies

Monday, January 13, 2020, 9:00-11:30

Organizer:

Yu Huang (Mentor, A Siemens Business)

Speakers:

Rahul Singhal (Mentor, A Siemens Business)

Yu Huang (Mentor, A Siemens Business)

## Tutorial-2: A Journey from Devices to Systems with FeFETs and NCFETs

Monday, January 13, 9:00-11:30

Organizers:

Prof. X.Sharon Hu (University of Notre Dame)

Dr. Hussam Amrouch (Karlsruhe Institute of Technology)

Speakers:

Prof. X.Sharon Hu (University of Notre Dame) or Prof. Xunzhao Yin (Zhejiang University)

Dr. Hussam Amrouch (Karlsruhe Institute of Technology)

## Tutorial-3: Comparison and Summary of Impulse-Sensitivity-Function (ISF) Extraction for Oscillator Phase Noise Optimization

Monday, January 13, 9:00-11:30

Organizer:

Dr. Yong Chen(Nick) (University of Macau)

Speakers:

Dr. Yong Chen(Nick) (University of Macau)

## Tutorial-4: General Trends of Security Engineering for In-vehicle Network Architecture in Modern Electric Vehicle

Monday, January 13, 9:00-11:30

Organizer:

Dr. Yi (Estelle) Wang (Continental Automotive Singapore)

Speakers:

Dr. Yi (Estelle) Wang (Continental Automotive Singapore)

Prof. Naehyuck Chang (Korea Advanced Institute of Science and Technology)

## Tutorial-5: Machine Learning for Reliability of ICs and Systems

Monday, January 13, 15:30 -18:00@Room306A

Organizer:

Mehdi B. Tahoori (Karlsruhe Institute of Technology)

Speakers:

Krishnendu Chakrabarty (Duke University)

Mehdi B. Tahoori (Karlsruhe Institute of Technology)

## Tutorial-6: Compression and Neural Architecture Search for Efficient Deep Learning

Monday, January 13, 13:00-15:20

Organizer:

Song Han (MIT EECS)

Speakers:

Song Han (MIT EECS)

## Tutorial-7: Designing Application-Specific AI Processors

Monday, January 13, 15:30-18:00

Organizer:

Zhiru Zhang (Cornell University)

Speakers:

Manish Pandey (Synopsys, Inc.)
Claudionor Coelho (Google, Inc. )
Zhiru Zhang (Cornell University)

## Tutorial-8: Hardware-based Security Solutions for the Internet of Things

Monday, January 13, 14:00-18:00

Organizer:

Dr. Basel Halak (University of Southampton)

Speakers:

Prof. Gang Qu,
Dr. Yier Jin
Dr. Chongyan Gu
Dr. Basel Halak

## Tutorial-9: An Emerging Trend in Post Moore Era: Monolithic 3D IC Technology

Monday, January 13, 14:00 -18:00@Room307B

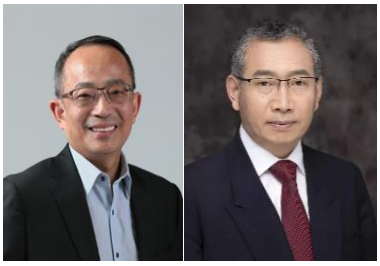
Organizer:

Yuanqing Cheng (Beihang University)

Speakers:

Sébastien Thuries (CEA-Leti)
Mohamed M. Sabry Aly (Nanyang Technological University)
Aida Todri-Sanial (LIRMM/University of Montpellier)
Ricardo Reis (UFRGS)
Yuanqing Cheng (Beihang University)

## Welcome to ASP-DAC 2020



On behalf of the Organizing Committee, it is our pleasure to welcome you to the 25th Asia and South Pacific Design Automation Conference (ASP-DAC), in Beijing, China on 13-16 January 2020! As the capital of China, Beijing is home to a great number of universities and colleges, including several world-class universities and research organizations of international stature; together with the large population of IC designers in China and the sound support from the Chinese government for the development of IC Industry, making Beijing a perfect place for hosting ASP-DAC 2020.

Since 1995, ASP-DAC has been served as a great platform for researchers, academics, industrial participants and students to exchange and share their ideas and the latest advanced technologies on LSI design and design automation areas.

ASP-DAC 2020 received 279 submissions from all over the world. Based on rigorous and thorough reviews by the Technical Program Committee, 86 papers have been accepted and 25 technical sessions have been organized. Seven Special Sessions have also been organized based on invited talks by the Technical Program Committee.

We have arranged 6 Keynote sessions to discuss the future directions of this area. The first keynote address is “Skin electronics for continuous health monitoring” by Prof. Takao Someya of University of Tokyo. The second one is “Design automation for customizable computing” by Prof. Jason Cong of University of California, Los Angeles. Four keynote speeches come from industry to share the opinions on this area from a different angle. They are “Explore the next tides of EDA” by Dr. Lifeng Wu, Empyrean Software, “Edge-to-cloud innovations for inclusive AI” by Dr. Xiaoning Qi, Alibaba Group, “Huge development of RISC-V arising from IOT spurt” by Dr. Zhang Yingwu, GigaDevice Semiconductor, “Emulation View of Synopsys Verification Continuum Platform” by Dr. Michael Wang, Synopsys.

The Designers' Forum is a unique program that will share design experience and solutions of real product developments among LSI designers and EDA developers, which will be held on January 15th and 16th. The topics discussed in this forum include “Trends in EDA”, “Emerging Design” and “AI Accelerators”. The University Design Contest is also an important annual event of ASP-DAC and 6 high-quality designs were selected for presentation in the morning, January 14th.

Seven tutorials have been arranged on Monday, January 13rd. Registrants can choose any topic depending on their interests and can obtain wider perspective on the recent hot topics.

There are thirteen enterprises joining in ASP-DAC2020 exhibition. They are leaders in the specific industry and will share the state-of-the-art products and systems.

Taking this opportunity, we would like to express our sincere appreciation to those who have contributed to ASP-DAC 2020, including authors, speakers, reviewers, session organizers, moderators, panelists, session chairs, keynote speakers, sponsors and committee members. We hope all attendees have an enjoyable and productive experience at ASP-DAC 2020.

**Tim Cheng and Huazhong Yang**

General Co-Chairs ASP-DAC 2020

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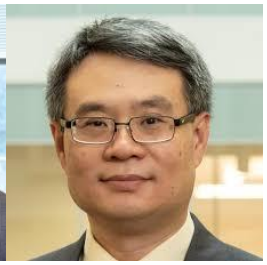
## Message from the Technical Program Committee


Tsun-Yi Ho


Sheldon Tan


Yiran Chen

On behalf of the Technical Program Committee of the 25th Asia and South Pacific Design Automation Conference (ASP-DAC) 2020, we would like to welcome all of you to the conference scheduled from January 13 to 16, 2020 at Beijing, China.

This year, we received 263 submissions from 23 countries/regions, with the majority of them from Asia, North America, and Europe. Paper selection was really a challenge. Different from the call-for-paper of last few years, we re-organize the themes of several tracks especially by adding Track 4 (Memory architecture and near/in memory computing) and Track 5 (Neural network and neuromorphic computing). To conduct the selection process, we formed the Technical Program Committee (TPC) into 14 subcommittees with 116 TPC members from 14 countries/regions who are leading experts on EDA, IC design, embedded system, memory architecture, machine learning, hardware security, and emerging technologies/applications. The review process ensured fairness through a rigorous double-blind review process to resolve any possible conflict of interest. The full day TPC meeting was held at Academia Sinica in Taipei, Taiwan on August 26, 2019, with the EDA Workshop afterwards. Almost all TPC members physically attended the TPC meeting, and some joined via teleconferencing due to several sudden emergencies. As the result of hard discussion on 263 submissions, 86 high-quality regular papers were selected, which corresponds to a very competitive acceptance rate of 32.6%.

The complete conference program consists of the regular papers, keynote speeches, as well as special and design contest sessions. They are compiled into a three-day, four parallel-session programs. The regular papers are presented in 25 sessions. Also, we have 7 special sessions and 3 design forum sessions. The keynotes are held every morning to kick off the technical sessions.

Among the accepted regular papers, 12 were nominated for the best paper candidates. These best paper candidates went through a thorough evaluation process by the Best Paper Award Committee chaired by Vice Technical Program Chair Sheldon Tan and composed of 14 committee members, and finally two papers were selected for the ASP-DAC 2020 Best Paper Awards.

The Technical Program of ASP-DAC 2020 is the fruit of the hard work of all the authors, reviewers, and TPC members. Special thanks go to TPC secretaries for their excellent support. Thanks to the generous financial support from Synopsys, Cadence, Mediatek, Kneron, Footprintku, and IEEE/CEDA, the TPC meeting provided high-quality supplements in both academic and social programs. Finally, we also would like to thank the members of the Organizing Committee for their excellent services.

We hope that you will enjoy the ASP-DAC 2020 technical program.

**Tsung-Yi Ho** (National Tsing Hua University)
TPC Chair, ASP-DAC 2020

**Sheldon Tan** (University of California Riverside)
TPC Vice Chair

**Yiran Chen** (Duke University)
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__Jaehyun Park__ (University of Ulsan, Korea)
__Chung-Wei Lin__ (National Taiwan University, Taiwan)
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__Deliang Fan__ (University of Central Florida, USA)
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**Sébastien LeBeux** (Lyon Institute of Nanotechnology, France)
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**Martin D. F. Wong** (University of Illinois at Urbana-Champaign, USA / Chinese Univ. of Hong Kong, China)
**Hung-Ming Chen** (National Chiao Tung University, Taiwan)
**Jianli Chen** (Fuzhou University, China)
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### [10] Design for Manufacturability and Reliability

*__Ulf Schlichtmann__ (Technical University of Munich, Germany)
**Evangeline Young** (Chinese University of Hong Kong, Hong Kong)
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*__Masanori Hashimoto__ (Osaka University, Japan)
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**Takashi Sato** (Kyoto University, Japan)
**Umamaheswara Rao Tida** (North Dakota State University, USA)
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### [12] Testing, Validation, Simulation, and Verification

*__Kohei Miyase__ (Kyushu Institute of Technology, Japan)
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**Paul Ampadu** (Virginia Tech.)
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# University LSI Design Contest

The University LSI Design Contest has been conceived as a unique program at ASP-DAC. The purpose of the contest is to encourage research in LSI design at universities and its realization on a chip by providing opportunities to present and discuss the innovation and state-of-the-art design. The scope of the contest covers circuit techniques for (1) Analog / RF / Mixed-Signal Circuits, (2) Digital Signal Processor, (3) Microprocessors, and (4) Custom Application Specific Circuits / Memories, and methodologies for (a) Full-Custom / Cell-Based LSIs, (b) Gate Arrays, and (c) Field Programmable Devices.

This year, the University LSI Design Contest Committee received 7 designs from four countries/areas, and selected 6 designs out of them. The selected designs will be discussed in Session 1A at three-minute presentations, followed by interactive discussions in front of their posters. For one outstanding design, the Best Design Award will be awarded in the opening session. We sincerely acknowledge the other contributions to the contest, too. It is our earnest belief to promote and enhance research and education in LSI design in academic organizations. Please come to the University LSI Design Contest and enjoy the stimulating discussions.

**Date: Tuesday, January 14, 2020**
**Place: China National Convention Center**

Oral Presentation: Room 310 (10:45—11:30)
Poster Presentation: Room 310 (11:30-12:00)

University LSI Design Contest Commitee Co-chairs:

Xiaoyang Zeng
(Fudan University)

Shouyi Yin
(Tsinghua University)

## Designers' Forum

The Designers'Forum is conceived as a unique program that shares the design experience and solutions of real product developments among LSI designers and EDA tool providers. The topics discussed in this forum include:

Oral Sessions:

(4A) Trends in EDA

The golden age of EDA — clock design, machine learning and A-I collaboration, Zhuo Li, Cadence

New Trend on High-Level Synthesis and Customized Compiler for Edge Intelligence, Deming Chen, UIUC

Data-driven Instant Model Synthesis Enhanced by Learning Algorithms For DTCO Enablement In the FinFET Era, Yanfeng li, Platform DA

(6D) Emerging Design

Recent advances in hardware security and testing tools, Junfeng Fan, OSR

Design of energy-efficient dynamic reconfigurable cryptographic chip, Jinjiang Yang, Tsinghua

Cognitive SSD controller: A case for agile domain-specific SoC design, Ying Wang, ICT

(9D) AI Accelerators

AI chips, what's next: architecture, tools, and methodology, Shan Tang

Computing-in-memory SoC chip for neural network inference, Shaodi Wang, Witin Tech

Enabling Data Center-Wide Accelerator Resource Pools for AI Applications, Kun Wang, VirtAI Tech

Session 4A (10:15-11:30, Jan. 15th)

[**Trends in EDA**]

The purpose of this session is to share and discuss recent advancements and trends in the EDA field. The first talk highlights some new trends and challenges in EDA design and discusses academic and industry collaboration during this new age. The second presentation discusses how to implement Edge intelligence with domain-specific high-level synthesis tools. The third talk presents a complete device modeling system with super-fast device characterization capability based on learning algorithms.

Session 6D (15:45-17:00, Jan. 15th)

**[Emerging Design]**

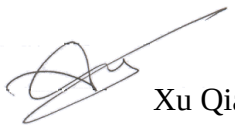
The purpose of this session is to share latest LSI designs and design methodologies. The first talk presents leading industry equipment and tools on security test. The second presentation introduces a coarse-grained dynamic reconfigurable cryptographic chip for high-throughput secure network processing and cloud computing. The third talk presents a case study on the so-called Cognitive SSD controller, a flexible and energy-efficient solution to unstructured data analysis.

Session 9D (15:45-17:00, Jan. 16th)

**[AI accelerators]**

The purpose of this session is to share and discuss latest advancements in AI accelerators. The first talk gives a visionary perspective on how the future AI chips will be designed, as the first generation of AI chips is getting mature. The second presentation introduces edge neural processing chips with analog computing-in-memory technology simultaneous achieving low-power, high-performance, and low-cost. The third talk discusses how innovative accelerator virtualization technologies can significantly increase accelerator utilization and ease AI application deployment.

Designers' Forum Chair:



Xu Qiang（The Chinese University of Hong Kong)

# ACM SIGDA Student Research Forum at ASP-DAC 2020

The Student Research Forum at the ASP-DAC is renovated from a traditional poster session hosted by ACM SIGDA for Ph.D. students to present and discuss their dissertation research with experts in system design and design automation community. Starting from 2015, the forum includes both Ph.D. and M.S. students, offering great opportunity for the students to establish contacts for their future career. In addition, the forum helps the companies and academic institutes to get an overview of the latest research and discover the extraordinary candidates for their employment. The forum is open to all students of the relevant research community and is free-of-charge.

**Date and Time: 18:15-20:00, January 14, 2020**
**Location: Room 308** [Food will be served.]

We would like to thank the following committee members for their support and contribution to this forum.

Technical Committee:

**Hiromitsu Awanon** (The University of Tokyo, Japan)
**Luan Huu Kinh Duong** (Nanyang Technological University, Singapore)
**Liang Shi** (East China Normal University, China) **Xianzhang Chen** (Chongqing University, China)
**Chun-Han Lin** (National Taiwan Normal University, Taiwan)
**Sicheng Li** (Hewlett Packard Labs, USA) **Wanli Chang** (University of York, UK)
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**Muhammad Shafique** (Vienna University of Technology, Austria)
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**Ming-Chang Yang** (The Chinese University of Hong Kong, China)
**Yukihide Kohira** (The University of Aizu, Japan) **Hoeseok Yang** (Ajou University, Korea)
**Shao-Yun Fang** (National Taiwan University of Science and Technology, Taiwan)
**Qian Zhang** (University of California, Los Angeles, USA)

ASP-DAC Liaison:

**Jiang Xu** (Hong Kong University of Science and Technology, Hong Kong)

The sponsors of this forum are ACM SIGDA and Cadence Design Systems, Inc. We would also like to thanks ASP-DAC 2020 for supporting this forum.

ACM SIGDA Student Research Forum Chair:

**Hyung Gyu Lee**
(Daegu University, Korea)

ACM SIGDA Student Research Forum Co-Chair:

**Weichen Liu**
(Nanyang Technological University, Singapore)

**Lei Jiang**
(Indiana University Bloomington, USA)

## Best Paper Award

### Award Winners

**2D-1: "Equivalent Capacitance Guided Dummy Fill Insertion for Timing and Manufacturability"**
Sheng-Jung Yu, Chen-Chien Kao, Chia-Han Huang, Iris Hui-Ru Jiang (National Taiwan Univ., Taiwan)

**7B-3 : "Towards Area-Efficient Optical Neural Networks: An FFT-based Architecture"**
Jiaqi Gu, Zheng Zhao, Chenghao Feng, Mingjie Liu, Ray T. Chen, David Z. Pan (Univ. of Texas, Austin, USA)

### Candidates

**1C-1: "Integrated Airgap Insertion and Layer Reassignment for Circuit Timing Optimization"**
*Younggwang Jung, Daijoon Hyun, Youngsoo Shin (KAIST,Republic of Korea)

**1D-1: "Analyzing The Security of The Cache Side Channel Defences With Attack Graphs"**
*Limin Wang, Ziyuan Zhu, Zhanpeng Wang, Dan Meng (Chinese Academy of Sciences, China)

**2B-1: "Co-Exploring Neural Architecture and Network-on-Chip Design for Real-Time Artificial Intelligence"**
Lei Yang (Univ. of Pittsburgh, USA), Weiwen Jiang (Univ. of Notre Dame, USA), Weichen Liu (Nanyang Technological Univ., Singapore), Edwin Sha (East China Normal Univ., China), Yiyu Shi (Univ. of Notre Dame, USA), Jingtong Hu (Univ. of Pittsburgh, USA)

**2D-1: "Equivalent Capacitance Guided Dummy Fill Insertion for Timing and Manufacturability"**
Sheng-Jung Yu, Chen-Chien Kao, Chia-Han Huang, Iris Hui-Ru Jiang (National Taiwan Univ., Taiwan)

**3C-1: "S3 DET: Detecting System Symmetry Constraints for Analog Circuits with Graph Similarity"**
Mingjie Liu, Wuxi Li, Keren Zhu, Biying Xu, *Yibo Lin, Linxiao Shen, Xiyuan Tang, Nan Sun, David Z. Pan(Univ. of Texas, Austin, USA)

**5A-1: "Towards Design Methodology of Efficient Fast Algorithms for Accelerating Generative Adversarial Networks on FPGAs"**
Jung-Woo Chang, *Saehyun Ahn, Keon-Woo Kang, Suk-Ju Kang (Sogang Univ., Republic of Korea)

**5B-1: "Towards Read-Intensive Key-Value Stores with Tidal Structure Based on LSM-Tree"**
Yi Wang, Shangyu Wu, Rui Mao (Shenzhen Univ., China)

**5C-1: "Unified Redistribution Layer Routing for 2.5D IC Packages"**
Chun-Han Chiang, *Fu-Yu Chuang, Yao-Wen Chang (National Taiwan Univ., Taiwan)

**7B-3 : "Towards Area-Efficient Optical Neural Networks: An FFT-based Architecture"**
Jiaqi Gu, Zheng Zhao, Chenghao Feng, Mingjie Liu, Ray T. Chen, David Z. Pan (Univ. of Texas, Austin, USA)

**8B-1: "Reliability-Oriented IEEE Std. 1687 Network Design and Block-Aware High-Level Synthesis for MEDA Biochips"**
Zhanwei Zhong, Tung-Che Liang, *Krishnendu Chakrabarty (Duke Univ., USA)

**8C-1: "Modulo Scheduling with Rational Initiation Intervals in Custom Hardware Design"**
*Patrick Sittel (Univ. of Kassel, Germany), John Wickerson (Imperial College London, UK), Martin Kumm (Univ. of Applied Sciences Fulda, Germany), Peter Zipf (Univ. of Kassel, Germany)

**8D-1: "WEID: Worst-Case Error Improvement in Approximate Dividers"**
*Hassaan Saadat (Univ. of New South Wales, Sydney, Australia), Haris Javaid (Xilinx, Singapore), Aleksandar Ignjatovic, Sri Parameswaran (Univ. of New South Wales, Sydney, Australia)

## University LSI Design Contest Award

### Best Design Award

**1A-1: "Design of a Single-Stage Wireless Charger with 92.3%-Peak-Efficiency for Portable Devices Applications"**

Lin Cheng (University of Science and Technology of China, China), Xinyuan Ge, Wai Chiu Ng, Wing-Hung Ki, Jiawei Zheng, Tsz Fai Kwok, Chi-Ying Tsui (The Hong Kong University of Science and Technology, China), Ming Liu (Institute of Microelectronics, Chinese Academy of Sciences, China)

## 10 year retrospective most influential paper award

### Award Winner

(ASP-DAC 2010)

A. B. Kahng, S. Kang, R. Kumar and J. Sartori, "Slack redistribution for graceful degradation under voltage overscaling," *2010 15th Asia and South Pacific Design Automation Conference (ASP-DAC),* Taipei, 2010, pp. 825-831.

### Candidates

A. B. Kahng, S. Kang, R. Kumar and J. Sartori, "Slack redistribution for graceful degradation under voltage overscaling," *2010 15th Asia and South Pacific Design Automation Conference (ASP-DAC),* Taipei, 2010, pp. 825-831.

J. H. Anderson, "A PUF design for secure FPGA-based embedded systems," *2010 15th Asia and South Pacific Design Automation Conference (ASP-DAC),* Taipei, 2010, pp. 1-6.

J. Yang, K. Lu, M. Cho, K. Yuan and D. Z. Pan, "A new graph-theoretic, multi-objective layout decomposition framework for Double Patterning Lithography," *2010 15th Asia and South Pacific Design Automation Conference (ASP-DAC),* Taipei, 2010, pp. 637-644.

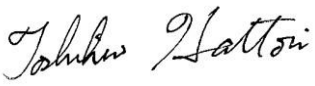
## Invitation to ASP-DAC 2021

On behalf of the Organizing Committee, it is my great pleasure and honor to invite you to the 26th ASP-DAC, to be held in Tokyo, Japan, January 18-21, 2021. Currently we are planning to come back to Odaiba, same venue with ASP-DAC 2019. As ASP-DAC 2019 attendees realized that Odaiba is an artificial island acting as a major commercial, residential and leisure area in the heart of the city. It is easily reachable from Narita and Haneda Airports, both international hubs connecting Tokyo to all the major cities of the world. In January you can be sure to enjoy a crisp Tokyo is famous for its rich culture, incredible cuisine and efficient transportation and this of course applies to Odaiba as well. Some of its touristic venues include the Odaiba Marine Park which features one of the two beaches in mainland Tokyo or the Oedo-Onsen-Monogatari which is a hot spring complex built in Edo-era style, ideal for experiencing part of the Japanese lifestyle. If possible, we recommend you to not limit your exploration to Odaiba and to visit other famous spots in Tokyo such as the Sensoji temple in Asakusa for cultural tourism, or the Omote Sando avenue for shopping.

Conference venue, we are currently planning, is famous for constantly presenting new technologies in fields such as robotic and astronomy which embody the future of society as the name of the venue implies in Japanese. It is conveniently located close to many hotels and will offer you an incredible night view of the famous Rainbow Bridge.

ASP-DAC 2021 offers you an ideal opportunity to touch the recent technologies and the future directions on electronic design automation areas. You will be able to meet and discuss with researchers and designers from all over the world, so please do not miss ASP-DAC 2021.

We are looking forward to seeing you in Tokyo during ASP-DAC 2021



**Toshihiro Hattori**

General Chair, ASP-DAC2021

# Tutorials

ASP-DAC 2020 offers attendees a set of two and a half hours intense introductions to specific topics. (This year, each tutorial will be presented once.)

| | Monday, January 13 | | | |
|---|---|---|---|---|
| | Room 306A | Room 306B | Room 307A | Room 307B |
| 9:00 | Tutorial-1<br>AI Chip Technologies and DFT Methodologies<br>[9:00-11:30] | Tutorial-2<br>A Journey from Devices to Systems with FeFETs and NCFETs<br>[9:00-11:30] | Tutorial-3<br>Comparison and Summary of Impulse-Sensitivity-Function (ISF) Extraction for Oscillator Phase Noise Optimization<br>[9:00-11:30] | Tutorial-4<br>General Trends of Security Engineering for In-vehicle Network Architecture in Modern Electric Vehicle<br>[9:00-11:30] |
| 11:30 | | | | |
| | Tutorial-5<br>Machine Learning for Reliability of ICs and Systems<br>[15:30-18:00] | Tutorial-6<br>Compression and Neural Architecture Search for Efficient Deep Learning<br>[13:00-15:20]<br><br>Tutorial-7<br>Designing Application-Specific AI Processors<br>[15:30-18:00] | Tutorial-8<br>Hardware-based Security Solutions for the Internet of Things<br>[14:00-18:00] | Tutorial-9<br>An Emerging Trend in Post Moore Era: Monolithic 3D IC Technology<br>[14:00-18:00] |

## Tutorial-1 Monday, January 13, 9:00-11:30@Room306A

**AI Chip Technologies and DFT Methodologies**

Organizer:

**Yu Huang** (Mentor, A Siemens Business)

Speakers:

**Rahul Singhal** (Mentor, A Siemens Business), **Yu Huang** (Mentor, A Siemens Business)

**Abstract:**

Hardware acceleration for Artificial Intelligence (AI) is now a very competitive and rapidly evolving market. In this tutorial, we will start by covering the basics of deep learning. We will proceed to give an overview of the new and exciting field of using AI chips to accelerate deep learning computations. It will cover the critical and special characteristics and the architecture of the most popular AI chips. Next we will summarize the features of the AI chips from design-for-test (DFT) perspective and introduce the DFT technologies that can help testing AI chips and speeding up time-to-market. Finally, we will present a few case studies on how DFT is implemented on the real AI chips.

**Biography:**

**Dr. Yu Huang** is a Senior Key Expert in the Silicon Test Systems Division of Mentor, A Siemens Business. His research interests include VLSI SoC testing, ATPG, compression and diagnosis. He holds 38 US patents. He has published more than 110 papers in leading IEEE Journals, conferences and workshops. He is a senior member of the IEEE. He has served as technical program committee member for DAC, ITC, SOCC, ATS, ETS, ASPDAC, NATW and other conferences and workshops in the testing area. He received a Ph.D. from the University of Iowa in 2002.

**Mr. Rahul Singhal** is a Technical Marketing Engineer with Tessent Solutions group of Mentor, A Siemens Business. His focus is on the industry requirements in the areas of ATPG, compression, low pin count testing and DFT for AI chips architectures. He is currently a program committee member of NATW. Rahul received his M.S. in Electrical and Computer Engineering from Portland State University in 2011.

## Tutorial-2 Monday, January 13, 9:00-11:30@Room306B

### A Journey from Devices to Systems with FeFETs and NCFETs

Organizers:

**Prof. X.Sharon Hu** (University of Notre Dame), **Dr. Hussam Amrouch** (Karlsruhe Institute of Technology)

Speakers:

**Prof. X.Sharon Hu** (University of Notre Dame) **or Prof. Xunzhao Yin** (Zhejiang University), **Dr. Hussam Amrouch** (Karlsruhe Institute of Technology)

**Abstract:**

FeFETs for In-Memory Computing:

Data transfer between a processor and memory is a major bottleneck in improving application-level performance. This is particularly the case for data intensive tasks such as some machine learning applications. In-memory computing, where certain data processing is performed in memory, can be an effective solution to address this bottleneck. Thus, compact, low-power, fast and non-volatile in-memory computing is highly desirable. This talk presents a cross-layer effort of designing in-memory computing modules based on ferroelectric field effect transistors (FeFETs), an emerging, non-volatile device. An FeFET is made by integrating a ferroelectric material layer in the gate stack of a MOSFET, and can behave as both a transistor and a non-volatile storage element. This unique property enables area efficient and low-power finely integrated logic and memory. After introducing the basics of FeFETs, this talk will focus on two major topics on FeFET based circuit and architecture designs: (i) FeFET based ternary content addressable memory (TCAM), and (ii) FeFET based Compute-In-Memory (CiM). For each topic, issues related to circuits, architectures and application-level benchmarking will be elaborated. We will culminate the talk with a specific application-level case study, i.e., memory augmented neural networks for few-shot learning.

NCFETs to Address the Fundamental Limits in Technology Scaling:

The inability of MOSFET transistors to switch faster than 60mV/decade, due to the nonscalable Boltzmann factor, is one of the key fundamental limits in physics for technology scaling. This is, in fact, the bottleneck in voltage scaling, which had led to the discontinuation of Dennard's scaling more than a decade ago. As a result, on-chip power densities have continuously increased and the operating frequency of processors stopped improving in the last decade to prevent unsustainable on-chip temperatures. In this talk, we will demonstrate how improvements in the electrical characteristics of transistors, obtained by a ferroelectric material, can be investigated from physics, where they do originate, all the way up to the system level, where they ultimately affect the efficiency of computing. We will focus on the Negative Capacitance FET (NCFET), which is unlike the abovementioned FeFET devices operate in the hysteresis-free region. We will explain how NCFET pushes the sub-threshold swing to below its fundamental limit and how this can revive the prior trends in processor design with respect to voltage and frequency scaling. We will focus on answering the following three key questions to draw the impact of NCFET technology on computing efficiency: In how far NCFET technology will enable processors (i) to operate at higher frequencies without increasing voltage? (ii) to operate at higher frequencies without increasing power density? and (iii) to operate at lower voltages, while still fulfilling performance requirement? The latter is substantial for IoT devices, where available power budgets are extremely restricted. We will also demonstrate how employing NCFET technology will have a significant impact not only on circuits but also on architecture- and system-level management techniques. For example, as opposed to conventional CMOS technology in which reducing the voltage minimizes the leakage power, NCFET has an inverse dependency. This means that conventional power management techniques will not work any longer since they would lead to suboptimal results depending on system-level workload properties. Such an example and others of the implications at the architectural and system levels will be also discussed during this tutorial talk towards providing the audience with the big picture behind NCFET technology.

**Biography:**

**Prof. X. Sharon Hu** is a professor in the department of Computer Science and Engineering at the University of Notre Dame, USA. Her research interests include low-power system design, circuit and architecture design with emerging technologies, hardware/software co-design and real-time embedded systems. She has published more than 300 papers in these areas. She received 3 best paper awards including one from the Design Automation Conference (DAC) and has participated in several large industry and government sponsored center-level projects and is a theme leader in an NSF/SRC E2CDA project. She is the General Chair of DAC in 2018 and was the TPC chair of DAC in 2015. She also served as Associate Editor for IEEE Transactions on VLSI, ACM Transactions on Design Automation of Electronic Systems, etc. and is an Associate Editor of ACM Transactions on Cyber-Physical Systems. X. Sharon Hu is a Fellow of the IEEE.

**Prof. Xunzhao Yin** is an assistant professor of the College of Information Science and Electronic Engineering at Zhejiang University. He received his Ph.D. degree in Computer Science and Engineering from University of Notre Dame in 2019 and B.S. degree in Electronic Engineering from Tsinghua University in 2013, respectively. His research interests include emerging circuit/architecture designs and novel computing paradigms with both CMOS and emerging technologies. He received the Outstanding Research Assistant Award in the Department of CSE at University of Notre Dame in 2017, and Bronze medal of Student Research Competition at ICCAD2016, etc.

**Dr. Hussam Amrouch** is a Research Group Leader at the Chair for Embedded Systems, Karlsruhe Institute of Technology (KIT), Germany. He is leading of the Dependable Hardware research group. He received his Ph.D. degree from KIT in 2015 with distinct (summa cum laude). His main research interests are emerging technologies, VLSI design and design for reliability at the device, circuit and system levels. He holds seven HiPEAC Paper Awards. He has published around 60 papers in these areas and receieved recently three best paper nominations at DAC'16, DAC'17 and DATE'17. He currently serves as Associate Editor at Integration, the VLSI Journal.

## Tutorial-3 Monday, January 13, 9:00-11:30@Room307A

**Comparison and Summary of Impulse-Sensitivity-Function (ISF) Extraction for Oscillator Phase Noise Optimization**

Organizer:

**Dr. Yong Chen**(Nick) (University of Macau)

Speakers:

**Dr. Yong Chen**(Nick) (University of Macau)

**Biography:**

**Prof. Yong Chen** received the B.Eng. degree in electronic and information engineering, Communication University of China (CUC), Beijing, China, in 2005, and the Ph.D. in Engineering degree in microelectronics and solid- state electronics, Institute of Microelectronics of Chinese Academy of Sciences (IMECAS), Beijing, China, in 2010. From 2010 to 2013, He worked as Post-Doctoral Researcher in Institute of Microelectronics, Tsinghua University, Beijing, China. From 2013 to 2016, he was Research Fellow in VIRTUS/EEE, Nanyang Technological University, Singapore. Since March 2016, he is an Assistant Professor of the State Key Laboratory of Analog and Mixed-Signal VLSI (AMSV) of University of Macau, Macao, China. His research interests include integrated circuits involving analog/mixed-signal/RF/mm-wave/wireline. Dr. Chen serves as an Associate Editor of IEEE Access since 2019 and Vice Chair of IEEE Macau CAS Chapter (’19-‘20). He services a conference local organization committee of ASSCC (’19) and a member of Technical Program Committee of APCCAS (‘19). His team reports 2 chip inventions at the 2019 IEEE International Solid-State Circuits Conference - ISSCC (Chip Olympics): mm-wave PLL (‘19) and VCO (‘19).

## Tutorial-4 Monday, January 13, 9:00-11:30@Room307B

**General Trends of Security Engineering for In-vehicle Network Architecture in Modern Electric Vehicle**

Organizer:

**Dr. Yi (Estelle) Wang** (Continental Automotive Singapore)

Speakers:

**Dr. Yi (Estelle) Wang** (Continental Automotive Singapore), **Prof. Naehyuck Chang** (Korea Advanced Institute of Science and Technology)

**Abstract:**

In this tutorial, we will cover two parts. The first part depicts the in-vehicle network architecture of the modern electric vehicle. The second part analyzes the security-related issue in an automotive domain from an automotive industrial tier-1 perspective (Top 5 in the worldwide and Top2 in Germany).

The motivation of this tutorial is to have a brief view about current hot topic, automotive electric vehicle and automotive security, which has attracted more and more attentions, especially in ASP-DAC in terms of the number of submissions related to this fields.

The first part presents the architecture of a modern electric vehicle and covers three aspects:

(1) Why do we drive electric vehicles? It is not easy to say that electric vehicles are higher performance compared with a similar price range of internal combustion engine vehicles. There are financial benefits including Government subsidies and tax deduction, which cannot be sustainable. A low maintenance cost is a good advantage, but vehicle depreciation is a big question. Therefore, environmental friendliness should be one clear motivation to drive electric vehicles. However, electric vehicles are only "zero exhaust emission" because of tire and brake emissions, which occupy a large portion of the total vehicle emissions. Even putting aside the tire and brake emissions, electric vehicles still contribute to a significant amount of pollution because of the source of electricity. Electric vehicles produce less than half of equivalent exhaust emissions compared with gasoline vehicles and not much different from that of hybrid vehicles. Higher MPGe (mile per gallon gasoline equivalent) of electric vehicles can largely mislead the energy efficiency when it comes to "well to wheel" efficiency taking the entire energy ecosystem into account.

(2) Challenges to make more efficient electric vehicles: It is challenging to make electric vehicles more fuel-efficient because the key powertrain components are already highly efficient, and therefore, there is a very narrow headroom for further enhancement. Consequently, the challenges for extended range of electric vehicles end up with the deployment of more lighter materials, which directly impacts on the manufacturing and repair costs, and it may make the actual cost of ownership very high. An extended driving range of electric vehicles is one of the most demanding requirements of the current and potential electric vehicle owners, but the use of a larger-capacity battery pack makes the vehicle curb weight heavier and thus the fuel efficiency worse.

(3) A system-level solution to enhance electric vehicle fuel efficiency with current powertrain technology: First, we develop an instantaneous power consumption modeling of electric vehicles by the curb weights, speed, acceleration, road slope, passenger and cargo weights, motor capacity, and so on, as a battery discharge model. We ensure the model fidelity as we fabricate a lightweight custom electric vehicle perform an extensive measurement. The model fidelity enables us to achieve a more accurate range estimation. We attempt both design and runtime energy optimization using electric-vehicle-specific energy characteristics. We emphasize that electric vehicles show completely different fuel consumption behaviors from internal combustion engine vehicles due to the significant discrepancy in the drivetrain. We introduce minimum-energy driving methods for electric vehicles, which are largely different from eco-driving methods of internal combustion engine vehicles. We also propose a rapid energy-aware electric vehicle synthesis that allows users to quickly customize their own electric vehicle powertrain specification without understanding the technology.

The second part presents a general introduction to security in automotive engineering. Continental, as a leading automotive technology company, has a holistic security architecture to cope with current and future challenges for electric vehicles, which details protection from a single ECU to the gateway and from in-vehicle communication to car-to-car/car-to-infrastructure communication and backend communication.

From the Continental's perspective, vehicle architecture renovation enlarges the attacking surface of a vehicle and brings more challenges in automotive security. Current challenges are feasible implementation, security process, state-of-the-art technology, heterogeneity architecture, secure development, and legislation, etc. Future automotive security engineering includes the discussions about automotive Ethernet, anomaly detection system, over the air update, post-quantum cryptography, and crypto agility. We detailed key technologies in this domain and provide an overview of each technology used in a modern electric vehicle.

**Biography:**

**Prof. Naehyuck Chang** is a Full Professor at the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST) from 2014. Before he joined KAIST, he was with the Department of Computer Science and Engineering, Seoul National University from 1997 to 2014. Dr. Chang also served as a Vice Dean of College of Engineering, Seoul National University from 2011 to 2013. His current research interests include low-power embedded systems and Design Automation of Things such as systematic design and optimization of Cyber-physical Systems.

Dr. Chang is an ACM Fellow and an IEEE Fellow for contribution to low-power systems. He was the Chair of the ACM SIGDA (Special Interest Group on Design Automation) and the Past Chair of ACM SIGDA. Dr. Chang is the Editor-in-Chief of the ACM (Association for Computing Machinery) Transactions on Design Automation of Electronic Systems, and an Associate Editor of IEEE Transactions on Very Large Scale Integration Systems. He also served for IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, IEEE Embedded Systems Letters, ACM Transactions on Embedded Computing Systems, and so on, as an Associate Editor.

Dr. Chang is (was) the General Co-Chair of VLSI-SoC (Very Large Scale Integration) 2015, ICCD (International Conference on Computer Design) 2014 and 2015, ISLPED (International Symposium on Low-Power Electronics and Design) 2011, etc. Dr. Chang is the Technical Program Chair of DAC (Design Automation Conference) 2016. He was the Technical Program (Co-)Chair of ASP-DAC (Asia and South Pacific Design Automation Conference) 2015, ICCD 2014, CODES+ISSS (Hardware-Software Codesign and System Synthesis) 2012, ISLPED 2009, etc.

Dr. Chang is the winner of the 2014 ISLPED Best Paper Award, 2011 SAE Vincent Bendix Automotive Electronics Engineering Award, 2011 Sinyang Academic Award, 2009 IEEE SSCS International SoC Design Conference Seoul Chapter Award, and several ISLPED Low-Power Design Contest Awards in 2002, 2003, 2004, 2007, 2012, 2014, and 2017.

Dr. Chang is a co-founder and the founding CEO of EMVcon Inc., a company for a battery solution of electric vehicle conversion.

**Dr. Yi Wang** received the Ph.D. degree in School of Computer Engineering from Nanyang Technological University, Singapore in 2008. Dr. Wang is currently a principal specialist in automotive security & privacy, Security & Privacy Competence Center, Corporate Systems and Technology, Continental Teves AG & Co. oHG (Frankfurt, Germany) from July 2016. Currently, she is leading the research topics at APAC on embedded automotive security including automotive Ethernet security, Intrusion Detection System/Anomaly Detection System (IDS/ADS) for in-vehicle network, side channel attacks/countermeasures for ECUs, and post quantum cryptography in embedded system. She works as a security specialist consultant for Continental business units and automotive OEMs (China, Japan and German). She is also responsible for the regulations and standardizations of Cybersecurity in APAC (Singapore, China, Japan, Korea), understanding the upcoming standard: ISO/SAE 21434 Road Vehicles – Cybersecurity Engineering and involving the upcoming regulations UNECE WP29.

Dr. Wang is also active in society activities with more than 40 international top journal (IEEE transactions and ACM transactions)/conference papers and 5 patents. She is a senior IEEE member. She is served as a Committee Member of the Singapore Chapter of the IEEE Circuit and System. She has been served as a Technical Program Committee member for ASP-DAC 2016, ASP-DAC 2018 (security track), CPSS 2018. I have been a program committee member of various reputable conferences, such as FPT-2013, FPT-2014, WESS-2014, UIC-2010, UIC-2011, UIC-2012, UIC-2013, etc., and a reviewer for many conferences/journals, such as TVLSI, TCAS-I, TCAS-II, TRETS, JSA, MICPRO, CSSP, CHES, FPT, WESS, ISCAS, ASP-DAC, VLSI, Latnicrypt, ICCIA, UIC, TSP, etc.

## Tutorial-5 Monday, January 13, 15:30 -18:00@Room306A

**Machine Learning for Reliability of ICs and Systems**

Organizer:

**Mehdi B. Tahoori** (Karlsruhe Institute of Technology)

Speakers:

**Krishnendu Chakrabarty** (Duke University), **Mehdi B. Tahoori** (Karlsruhe Institute of Technology)

**Abstract:**

With increasing the complexity of digital systems and the use of advanced nanoscale technology nodes, various process and runtime variabilities threaten the correct operation of these systems. The interdependence of these reliability detractors and their dependencies to circuit structure as well as running workloads makes it very hard to derive simple deterministic models to analyze and target them. As a result, machine learning techniques can be used to extract useful information which can be used to effectively monitor and improve the reliability of digital systems. These learning schemes are typically performed offline on large data sets in order to obtain various regression models which then are used during runtime operation to predict the health of the system and guide appropriate adaptation and countermeasure schemes. The purpose of this tutorial is to discuss and evaluate various learning schemes in order to analyze the reliability of the ICs and systems due to various runtime failure mechanisms which originate from process and runtime variabilities such as thermal and voltage fluctuations, device and interconnect aging mechanisms, as well as radiation-induced soft errors. The tutorial will also describe how time-series data analytics based on key performance indicators can be used to detect anomalies and predict failure in complex electronic systems. A comprehensive set of experimental results will be presented for data collected during 30 days of field operation from over 20 core routers.

**Biography:**

**Prof. Mehdi Tahoori** is currently a Full Professor and the Chair of Dependable Nano-Computing, Institute of Computer Science and Engineering, Department of Computer Science, Karlsruhe Institute of Technology, Karlsruhe, Germany. He received the B.S. degree in computer engineering from the Sharif University of Technology, Tehran, Iran, in 2000, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 2002 and 2003, respectively. In 2003, he was an Assistant Professor with the Department of Electrical and Computer Engineering, Northeastern University, where he became an Associate Professor in 2009. From August to December 2015, he was a visiting professor at VLSI Design and Education Center (VDEC), University of Tokyo, Japan. From 2002 to 2003, he was a Research Scientist with Fujitsu Laboratories of America, Sunnyvale, CA. He has authored over 250 publications in major journals and conference proceedings on a wide range of topics, from dependable computing and emerging nanotechnologies to system biology, and holds several US and European patents. He is currently the editor-in-chief of Microelectronic Reliability journal, associate editor for IEEE Design and Test Magazine, coordinating editor for Springer Journal of Electronic Testing (JETTA), and associate editor of IET Computers and Digital Techniques. He is the program chair of VLSI Test Symposium 2018 and General Chair of European Test Symposium 2019. Prof. Tahoori was a recipient of the National Science Foundation Early Faculty Development (CAREER) Award. He has received several best paper nominations and awards at various conferences and journals.

**Prof. Krishnendu Chakrabarty** received the B. Tech. degree from the Indian Institute of Technology, Kharagpur, in 1990, and the M.S.E. and Ph.D. degrees from the University of Michigan, Ann Arbor, in 1992 and 1995, respectively. He is now the William H. Younger Distinguished Professor and Department Chair of Electrical and Computer Engineering, and Professor of Computer Science, at Duke University.

Prof. Chakrabarty is a recipient of the National Science Foundation CAREER award, the Office of Naval Research Young Investigator award, the Humboldt Research Award from the Alexander von Humboldt Foundation, Germany, the IEEE Transactions on CAD Donald O. Pederson Best Paper Award (2015), the ACM Transactions on Design Automation of Electronic Systems Best Paper Award (2017), and over a dozen best paper awards at major conferences. He is also a recipient of the IEEE Computer Society Technical Achievement Award (2015), the IEEE Circuits and Systems Society Charles A. Desoer Technical Achievement Award (2017), the Semiconductor Research Corporation Technical Excellence Award (2018), and the Distinguished Alumnus Award from the Indian Institute of Technology, Kharagpur (2014). He is a Research Ambassador of the University of Bremen (Germany) and a Hans Fischer Senior Fellow (named after Nobel Laureate Prof. Hans Fischer) at the Institute for Advanced Study, Technical University of Munich, Germany. He is a 2018 recipient of the Japan Society for the Promotion of Science (JSPS) Fellowship in the "Short Term S: Nobel Prize Level" category (typically awarded to eminent researchers who have won the Nobel Prize or similar honors), and he was a 2009 Invitational Fellow of JSPS. He has held Visiting Professor positions at University of Tokyo and the Nara Institute of Science and Technology (NAIST) in Japan, and Visiting Chair Professor positions at Tsinghua University (Beijing, China) and National Cheng Kung University (Tainan, Taiwan). He is currently an Honorary Chair Professor at National Tsing Hua University in Hsinchu, Taiwan, and an Honorary Professor at Xidian University in Xi'an, China.

Prof. Chakrabarty's current research projects include: testing and design-for-testability of integrated circuits and systems; digital microfluidics, biochips, and cyberphysical systems; data analytics for fault diagnosis, failure prediction, anomaly detection, and hardware security; neuromorphic computing systems. He has authored 20 books on these topics (with one translated into Chinese), published over 660 papers in journals and refereed conference proceedings, and given over 300 invited, keynote, and plenary talks. He has also presented 60 tutorials at major international conferences, including DAC, ICCAD, DATE, ITC, and ISCAS. Prof. Chakrabarty is a Fellow of ACM, a Fellow of IEEE, and a Golden Core Member of the IEEE Computer Society. He holds 11 US patents, with several patents pending. He is a recipient of the 2008 Duke University Graduate School Dean's Award for excellence in mentoring, and the 2010 Capers and Marion McDonald Award for Excellence in Mentoring and Advising, Pratt School of Engineering, Duke University. He has served as a Distinguished Visitor of the IEEE Computer Society (2005-2007, 2010-2012), a Distinguished Lecturer of the IEEE Circuits and Systems Society (2006-2007, 2012-2013), and an ACM Distinguished Speaker (2008-2016).

Prof. Chakrabarty served as the Editor-in-Chief of IEEE Design & Test of Computers during 2010-2012 and ACM Journal on Emerging Technologies in Computing Systems during 2010-2015. Currently he serves as the Editor-in-Chief of IEEE Transactions on VLSI Systems. He is also an Associate Editor of IEEE Transactions on Biomedical Circuits and Systems, IEEE Transactions on Multiscale Computing Systems, and ACM Transactions on Design Automation of Electronic Systems, and a coordinating editor for Springer Journal of Electronic Testing (JETTA).

## Tutorial-6 Monday, January 13, 13:00-15:20@Room306B

**Compression and Neural Architecture Search for Efficient Deep Learning**

Organizer:

**Song Han** (MIT EECS)

Speakers:

**Song Han** (MIT EECS)

**Abstract:**

Efficient deep learning computing requires algorithm and hardware co-design to enable specialization: we usually need to change the algorithm to reduce memory footprint and improve energy efficiency. However, the extra degree of freedom creates a much larger design space. Human engineers can hardly exhaust the design space by heuristics, and there's a shortage of machine learning engineers. We propose techniques to architect efficient neural networks efficiently and automatically.

We first introduce Deep Compression (ICLR'16) techniques to reduce the size of neural networks, followed by EIE accelerator (ISCA'16) that directly accelerate a sparse and compressed model. Then investigate automatically designing small and fast models (ProxylessNAS, ICLR'19), auto channel pruning (AMC, ECCV'18), and auto mixed-precision quantization (HAQ, CVPR'19). We demonstrate such learning-based, automated design achieves superior performance and efficiency than rule-based human design. Finally, we accelerate computation-intensive AI applications including TSM (ICCV'19) for efficient video recognition and PVCNN (NeurIPS'19) for efficient 3D point cloud recognition.

**Biography:**

**Prof. Song Han** is an assistant professor at MIT EECS. Dr. Han received the Ph.D. degree in Electrical Engineering from Stanford University and B.S. degree in Electrical Engineering from Tsinghua University. Dr. Han's research focuses on efficient deep learning computing. He proposed "Deep Compression" and " EIE Accelerator" that impacted the industry. His work received the best paper award in ICLR'16 and FPGA'17. He was the co-founder and chief scientist of DeePhi Tech acquired by Xilinx. Dr. Han is listed by MIT Technology Review's 35 Innovators Under 35.

## Tutorial-7 Monday, January 13, 15:30-18:00@Room306B

**Designing Application-Specific AI Processors**

Organizer:

**Zhiru Zhang** (Cornell University)

Speakers:

**Manish Pandey** (Synopsys, Inc.), **Claudionor Coelho** (Google, Inc. ), **Zhiru Zhang** (Cornell University)

**Abstract:**

As machine learning is used in increasingly diverse applications, ranging from autonomous drones and IoT edge devices to self-driving vehicles, specialized computing architectures and platforms are emerging as alternatives to CPUs and GPUs, to meet energy, cost and performance (throughput/latency) requirements imposed by these applications. The proposed tutorial starts with an overview of the compute and data complexity for deep neural networks (DNNs), the underlying operations and how these can be realized as Application-specific integrated circuits (ASICs) or field-programmable gate arrays (FPGAs). Exploiting the underlying parallelism in DNNs requires large computational arrays and high-bandwidth memory accesses for weights, feature maps and inter-layer communication. These arrays, consisting of adders, multipliers, square root and other arithmetic circuits consume expensive chip real estate. Memory accesses, necessary to store network parameters and activation values, impose high bandwidth requirements, necessitating both on-chip memory as well as high-bandwidth off-chip memory interconnects. The tutorial discusses algorithm-hardware co-design, starting with benchmarking metrics and energy-driven DNN models and covers a number of different hardware optimizations including reduction of parameters and floating-point operations, network pruning and compression, and data size reduction. The power and latency cost of memory accesses have prompted new near-memory and in-memory computing architectures which reduce energy cost by embedding computations in memory structures.

**Biography:**

**Manish Pandey** is a Fellow and Vice President of R&D at Synopsys, and an Adjunct Professor in the ECE Department at Carnegie Mellon University. He leads the Machine Learning and Formal Verification engineering teams at Synopsys. Manish completed his PhD in Computer Science from Carnegie Mellon University and a B.Tech. in Computer Science from the Indian Institute of Technology Kharagpur. He has extensive experience in machine learning, distributed systems and infrastructure, when he led the display ad targeting and security group at Yahoo!, and storage analytics systems at Nutanix. He previously led the development of several formal verification technologies at Verplex and Cadence which are in widespread use in the industry. Dr. Pandey has been the recipient of the IEEE Transaction in CAD Outstanding author award, and holds over two dozen patents and refereed publications.

**Claudionor N. Coelho** is a serial innovator, working on Machine Learning/Deep Learning hardware acceleration for video compression at Google. Previously, he was the VP of Software Engineering, Machine Learning and Deep Learning at NVXL Technology, being responsible for creating new hardware/software acceleration techniques that led to an investment from Alibaba of USD 15 million. He was the VP of Debug and CTO for AI at Synopsys Inc, the GM for Brazil for Cadence Design Systems, and previously the SVP of Engineering for Jasper Design Automation, leading the team that was awarded the Red Herring most innovative company in the US in 2013. He has more than 80 papers and patents, and he was an Associate Professor of Computer Science at UFMG, Brazil. He has a PhD in EE/CS from Stanford University, and an MBA from IBMEC Business School, and an MSCS and BSEE (summa cum laude) from UFMG, Brazil. He is currently an Associate Editor for IEEE TCAD on Machine Learning/AI Automation.

**Zhiru Zhang** is an Associate Professor in the School of ECE at Cornell University. His research investigates new applications, design automation tools, and accelerator architectures for heterogeneous computing. He co-founded AutoESL Design Technologies, Inc. to commercialize his dissertation research on high-level synthesis (HLS). AutoESL was acquired by Xilinx in 2011 and its HLS tool is now known as Vivado HLS. His research group designed an efficient binarized neural network (BNN) accelerator for the Celerity SoC, a complex RISC-V based SoC with 385 million transistors implemented in TSMC 16nm by a team of three universities. His recent research on hardware-efficient model compression and quantization methods for DNNs was presented in the premier ML and computer vision conferences (e.g., ICML'19, CVPR'19). His work has been recognized with a Google Research Award (2018), DAC Under-40 Innovators Award (2018), the UCLA Rising Professional Achievement Award (2018), a DARPA Young Faculty Award (2015), the IEEE CEDA Ernest S. Kuh Early Career Award (2015), an NSF CAREER Award (2015), the Ross Freeman Award for Technical Innovation from Xilinx (2012).

## Tutorial-8 Monday, January 13, 14:00-18:00@Room307A

**Hardware-based Security Solutions for the Internet of Things**

Organizer:

**Dr. Basel Halak** (University of Southampton)

Speakers:

**Prof. Gang Qu, Dr. Yier Jin, Dr. Chongyan Gu, Dr. Basel Halak**

**Abstract:**

The internet of Things technology is expected to generate tremendous economic benefits, this promise is undermined by major security threats. First of all the vast majority of these devices are expected to communicate wirelessly, and will be connected to the Internet, which makes them especially susceptible to confidentiality threats from attackers snooping for messages contents. Second, most IoT devices are expected to be deployed in remote locations with little or no protection. Therefore, they can be vulnerable to both invasive and side channel attacks, malicious adversaries can potentially gain access to a device and apply well know power or timing analyses to extract sensitive data that might be stored on the IoT node, such as encryption keys, digital identifiers, and recorded measurements. Furthermore, with ubiquitous systems, it can no longer be assumed that the attacker is remote. Indeed, the attack could even come from within the system itself, from rogue embedded hardware (e.g. Trojans) or a malicious software (e.g. a malware). A large proportion of IoT devices operate in an energy- constrained environment with very limited computing resources, this makes the use of typical defence mechanisms such as classic cryptography algorithms prohibitively expensive. The challenges for building secure IoT systems can be stated as three questions:

1) How to develop cryptographic primitives which are secure and energy-efficient
2) How to implement complex security protocols with very limited resources
3) How to remotely verify the secure and reliable operation of an IoT node

This tutorial provides detailed explanation of the state of the art techniques used to tackle the above three challenges, these includes lightweight authentication protocols, attestation schemes and physically unclonable functions

**Biography:**

**Dr. Basel Halak** is the founder and director of the embedded system program at the University of Southampton, a visiting professor at the Technical University of Kaiserslautern, a fellow of the royal academy of engineering and a senior fellow of the higher education academy. He has written over 70-refereed conference and journal papers, and authored two books, including the first textbook on Physically Unclonable Functions. His research expertise include evaluation of security of hardware devices, development of appropriate countermeasures, the development of mathematical formalisms of reliability issues in CMOS circuits (e.g. crosstalk, radiation, ageing), and the use of fault tolerance techniques to improve the robustness of electronics systems against such issues. Dr Halak serves in several technical program committees such as HOST, IEEE IVSW, ICCCA, ICCCS, MTV and EWME. He is an associate editor of IEEE access and an editor of the IET circuit devices and system journal. He is also member of hardware security working group of the World Wide Web Consortium (W3C).

Speakers' related Experience:

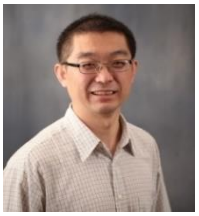
This tutorial was presented in IEEE DATE 2019 for the first time, in addition, participating speakers have delivered related materials in other events. We have included below a list of related talks for each speaker:

**Dr. Basel Halak**

Invited Speaker, University of Kaiserslautern, Germany, On the Personalities of Electronics Systems and their Security Applications, 2018.

Embedded Tutorial: Physically Unclonable Functions: Design Principles, Applications and Outstanding Challenges, IEEE International Verification and Security Workshop (IVSW), Spain, 2018.

Half-Day Tutorial: Hardware-based Security Solutions for the Internet of Things. 59th IEEE International Midwest Symposium on Circuits and Systems, Abu Dhabi, 2016



**Prof. Gang Qu**

Tutorial: Hardware based Lightweight Authentication for IoT Application. ACM SIGDA Design Automation Summer School at DAC, 2017

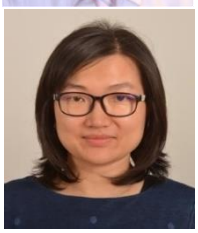
Tutorial: Hardware based Lightweight Authentication for IoT Application VLSI Test Technology Workshop, 2017

Invited Talk on Lightweight Authentication for IoT RISE Spring School at the University of Cambridge.2018

**Dr. Yier Jin**

Invited Talk: Hardware Supported Cybersecurity for Internet of Things, Northwestern University, Chicago, IL February 2018

Keynote Hardware Supported Cybersecurity for Internet of Things 18th International Workshop on Microprocessor/SoC Test, Security & Verification (keynote), Austin, TX December 2017



**Dr. Chongyan Gu**

Invited Talk on IoT security, Global Grand Challenges Summit organized by the Chinese Academy of Engineering, UK Royal Academy of Engineering and US National Academy of Engineering, Beijing, September 2015.

## Tutorial-9 Monday, January 13, 14:00 -18:00@Room307B

**An Emerging Trend in Post Moore Era: Monolithic 3D IC Technology**

Organizer:

**Yuanqing Cheng** (Beihang University)

Speakers:

**Sébastien Thuries** (CEA-Leti), **Mohamed M. Sabry Aly** (Nanyang Technological University), **Aida Todri-Sanial** (LIRMM/University of Montpellier), **Ricardo Reis** (UFRGS), **Yuanqing Cheng** (Beihang University)

**Abstract:**

The semiconductor industry enters the post Moore era where transistor scaling is not the sole driving force in delivering the required performance and functionality. To harvest the gains of higher integration densities without shrinking the feature size, monolithic three-dimensional (3D) integration has been proposed as a highly promising alternative to lead system integration in the post Moore regime. This tutorial aims to introduce this emerging technology from the perspectives of fabrication process, design automation, reliable and low power design, and architecutre innovations.

**Biography:**

**Sébastien Thuries** is leading the High-Density 3D Architecture and Design group at CEA-LETI including fine pitch 3D Stacking as well as Monolithic 3D (M3D). He has worked on and led several Digital ASIC developments for a set of application like 4G Digital Base Band, Complex Imagers, System on Chip, Mixed Signal RF over the last decade…He has been a pioneer in FDSOI digital design and back biasing capability. He leads the research team on new architecture and design paradigm raised by M3D-IC in order to optimize the full system to technology fields. Sébastien Thuries has received his Master Degree in 2003 from Institut des Sciences de l'Ingénieur de Montpellier (Poly'tech Montpellier) and joined CEA/Leti in 2004 as research engineer.

**Prof. Mohamed M. Sabry Aly** is an assistant professor at Nanyang Technological University, Singapore. He received his Ph.D. degree in electrical and computer engineering from École Polytechnique Fédérale de Lausanne (EPFL), in 2013. He was a postdoctoral research fellow at Stanford University. His current research interests include system-level design and optimization of computing systems enabled by emerging technologies. Dr. Aly was a recipient of the Swiss National Science Foundation Early Post-Doctoral Mobility Fellowship in 2013.

**Prof. Aida Todri-Sanial** received the B.S. degree in electrical engineering from Bradley University, IL in 2001, M.S. degree in electrical engineering from Long Beach State University, CA, in 2003 and a Ph.D. degree in electrical and computer engineering from the University of California Santa Barbara, in 2009. She received her French Habilitation (Habilitation a Diriger des Recherches) from the University of Montpellier in 2015. She obtained a post-graduate certificate in Entrepreneurship Programme for Women in Science, Technology and Engineering from the Judge Business School, University of Cambridge, UK in 2017. Her research interests focus on nanometer-scale issues in high-performance VLSI design with emphasis on power, thermal, signal integrity, and reliability issues as well as on circuits and systems for emerging technologies and nanomaterials. She has co-authored more than 100 publications on VLSI design area and emerging technologies.

**Prof. Ricardo Reis** is a Professor at UFRGS since 1979. He is former member of the Microelectronics Committee of National Council for Scientific and Technological Development (CNPq). Former member of the Computer Science Committee of National Council for Scientific and Technological Development (CNPq), for two terms. He pulished more than 500 hundred papers in journals and conferences proceedings (like IEEE Design & Test, ACM TODAES, IEEE JSSC, ISCAS, SBCCI, PATMOS, VLSI-SoC, DAC, DATE, ICCD, CICC, ASP-DAC, LATW). He recevied many awards including Award as research of the year from the Fapergs, Silver Core award from IFIP, Research level 1A of the CNPq (Brazilian National Science Foundation). His primary research interests include Physical Design Automation and Methodologies, CAD tools, Circuits Tolerant to Radiation, VLSI Design Methodologies and Microelectronics Education.

**Prof. Yuanqing Cheng** received B.S. degree from Xidian University, Xi'an, China and M.S. degree from Harbin Institute of Technology, Harbin, China. He got Ph.D. degree from Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China. From 2012 to 2013, Dr. Cheng was a post-doc researcher in LIRMM, Montpellier, France. Then, Dr. Cheng joined in School of Microelectronics, Beihang University as an assistant professor. From 2015 to 2016, Dr. Cheng worked in University of California, Santa Barbara, CA, USA as a visiting scholar. Now, Dr. Cheng is IEEE/ACM member, CCF senior member. He has published more than 40 peer-review conference/journal papers, including ICCAD, ASPDAC, TCAD, TVLSI, etc. He now severs as IEEE/ACM DATE conferene, IEEE PATMOS/ISVLSI TPC member. His research topics include computer architecture/aided design for emerging technologies, such as STT- MRAM and carbon nanotube technology, 3D integrated circuit design, etc.

# At a glance

## Tuesday, January 14

| | Room 310 | Room 308 | Room 307A | Room 307B |
|---|---|---|---|---|
| 9:00 | **1K** (Room 311) **Opening and Keynote Session I** | | | |
| 10:30 | Coffee Break | | | |
| 10:45 | 1A University Design Contest | 1B Machine Learning in Physical Design | 1C Toward Optimal Timing and PDN Design | 1D Side Channel Attacks and Countermeasures |
| 12:00 | **2K** (Room 311)**Keynote session II** | | | |
| 12:40 | Lunch Break | | | |
| 14:00 | 2A (SS-1): Designing Reliable and Robust Circuits and Systems in the Nanometer Era | 2B System Architecture Innovation | 2C Optical Networks-on-Chips and Quantum Circuit Design | 2D Reliability from Design to Manufacturing |
| 15:40 | Coffee Break | | | |
| 16:00 | 3A Reliability and Security for Deep Neural Networks | 3B Memory Architecture for Emerging Technologies | 3C Techniques for Analog Circuits and NoC | 3D Advanced test, verification and fault tolerance techniques |
| 17:15 | Break | | | |
| 18:15 | | ACM SIGDA Student Research Forum at ASP-DAC 2020 | | |
| 20:00 | | | | |

## Wednesday, January 15

| | Room 310 | Room 308 | Room 307A | Room 307B |
|---|---|---|---|---|
| 9:00 | **3K** (Room 311) **Keynote Session III** | | | |
| 10:00 | Coffee Break | | | |
| 10:15 | 4A (DF-1): Trends in EDA | 4B Machine-Learning and Low-Power Design | 4C Cryptographic Hardware Implementation and Secure Approximate Computing | 4D Emerging Embedded Systems Architecture |
| 11:30 | **4K** (Room 311) **Keynote Session IV** | | | |
| 12:10 | Lunch Break | | | |
| 13:50 | 5A Architecture and Algorithm for Deep Neural Networks | 5B Advanced Memory Systems | 5C Advances in Physical Design | 5D System Simulation and Exploration |
| 15:30 | Coffee Break | | | |
| 15:45 | 6A (SS-2): Computation-in-Memory based on emerging non-volatile memories: Technology, design, and test and reliability | 6B (SS-3): Title: Emerging Memory Enabled Computing in The Post-Moore's Era [15:45-17:25] | 6C (SS-4): AI Enhanced Simulation and Optimization in Back-End EDA Flow | 6D (DF-2): Emerging Design |
| 17:00 | Break | | | |
| 17:30 | **5K** (Room 311) **Keynote session V** | | | |
| 18:10 | Break | | | |
| 18:30 | (Room 311) **Banquet** | | | |
| 20:00 | | | | |

## Thursday, January 16

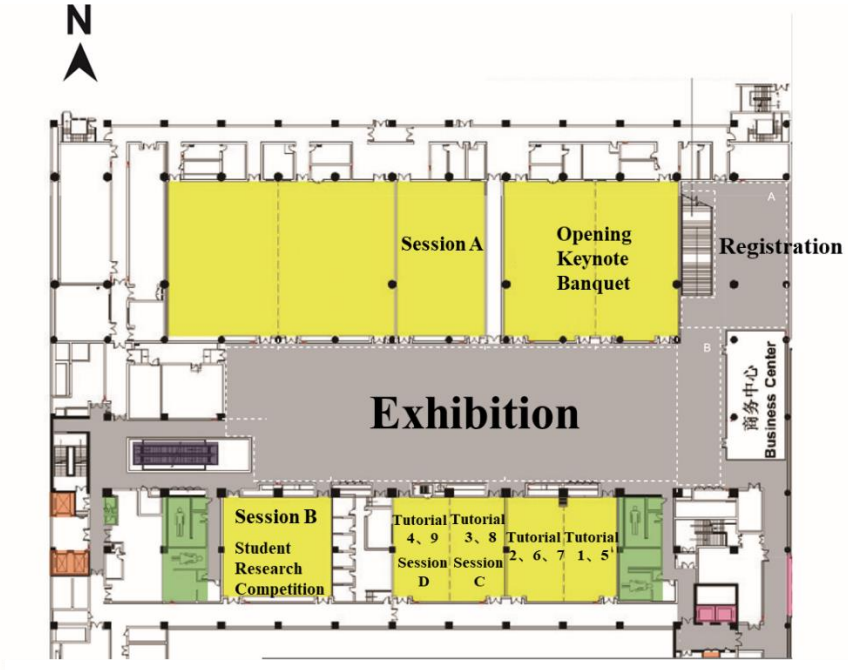
| | Room 310 | Room 308 | Room 307A | Room 307B |
|---|---|---|---|---|
| 9:00 | **6K** (Room 311) **Keynote Session VI** | | | |
| 10:00 | Coffee Break | | | |
| 10:15 | 7A Neuromorphic Computing | 7B Machine Learning for Embedded Systems | 7C Malicious Activities Generation and Detection | 7D Embedded Software for Energy Optimization and Non-Volatile Memory |
| 11:30 | Lunch Break | | | |
| 13:50 | 8A Search and Optimization for Deep Neural Networks | 8B FPGAs for Big Data Systems, Nonvolatile Computing, and Microfluidics | 8C Advances in Logic/High-Level Synthesis | 8D Scalable and Reconfigurable Approximate Arithmetic Units |
| 15:30 | Coffee Break | | | |
| 15:45 | 9A (SS-5): Resilience in Integrated Systems | 9B (SS-6): Emerging Technologies across the Abstraction Layers | 9C (SS-7): CMOS Annealing Hardware: Pursuing Efficiency for Solving Combinatorial Optimization Problems | 9D (DF-3): AI Accelerators |
| 17:00 | | | | |

# Room Assignment

## Room Assignment

| Location | Event |
|---|---|
| North Foyer | Registration, Information Desk, Supporter's Exhibition, and Coffee Break |
| Room306A | Tutorials 2,6,7 |
| Room306B | Tutorials 1,5 |
| Room307A | Session C and Tutorials 3,8 |
| Room307B | Session D and Tutorials 4,9 |
| Room308 | Session B and Student Research Forum |
| Room310 | Session A |
| Room311 | Opening, Keynotes I,II,III, IV, V, VI, and Banquet |

## Floor Map of China National Convention Center 3F:




## Area Map for China National Convention Center:

# Keynote Addresses

## *Keynote Speeches From Academia*

## Keynote I

Tuesday, January 14, 9:00-10:30

### "Skin electronics for continuous health monitoring"

**Takao Someya**

The University of Tokyo

**Abstract**

Flexible and stretchable hybrid electronics are expected to open up a new class of applications ranging from healthcare, medical, sports, wellness, human-machine interfaces, and new IT fashion. In particular, to expand emerging applications of wearable technologies, printed flexible biomedical sensors have attracted much attention recently. In order to minimize the discomfort of wearing sensors, it is highly desirable to use soft electronic materials particularly for devices that come directly into contact with the skin and/or biological tissues. In this regard, electronics manufactured on thin polymeric films, elastomeric and textile substrates by printing are very attractive. In this talk, I will review recent progresses of wearables, smart apparels, and artificial electronic skins (E-skins) from the contexts of high-precision and long-term vital signal monitoring. Furthermore, the issues and the future prospect of wearables and beyond wearables will be addressed.

## Keynote III

Wednesday, January 15, 9:00-10:00

### "Design Automation for Customizable Computing"

**Jason Cong**

University of California, Los Angles

**Abstract**

With large-scale deployment of FPGAs in both private and public clouds in the past a few years, customizable computing is transitioning from advanced research into mainstream computing. Customized accelerators have demonstrated significant performance and energy efficiency benefits for a wide range of applications. However, efficient design and implementation of various accelerators on FPGAs remains a formidable barrier to many software programmers, despite the recent advances in high-level synthesis. This calls for a community-wide effort to "demacratize customizable computing". In this talk, I shall first discuss various research opportunities associated with design automation for customizable computing. Then, I shall highlight our recent progress on source-code level transformation and optimization for customizable computing, including support of high-level domain-specific languages (DSL) for deep learning (e.g. Caffe), imaging processing (e.g. Halide), and big-data processing (e.g. Spark), and suppoort of automated compilation to customized microarchictecture templates, such as systolic arrays, stencils, and CPPs (composable parallel and pipelined).

## *Keynote Speeches From Industry*

# Keynote II

Tuesday, January 14, 12:00-12:40

### “Edge-to-Cloud Innovations for Inclusive AI”

**Xiaoning Qi**

Alibaba Group

**Abstract**

Technology has propelled us into an era of data and AI, and computing power is the force behind it all. At the core of computing power is the tiny yet mighty chip. T-Head has formed a full-stack chip system that facilitates edge-to-cloud integration, including processor IPs, SoC platforms, and AI chips. T-Head's success in hardware-software innovation is built on its self-developed chip structure and bolstered by Alibaba DAMO Academy's leading AI algorithms and AliOS operating system.

# Keynote IV

Wednesday, January 15, 11:30-12:10

### “Huge development of RISC-V arising from IOT spurt”

**Zhang Yingwu**

GigaDevice Semiconductor (Beijing) Inc

**Abstract**

With the huge demand of IoT, wearable device, AI, automotive, intelligent manufacturing and new emerging applications, which offers MCU greater opportunities as well as more challenges. We should find the optimized solutions and technologies for these obstacles in different scenarios, such as larger data processing and faster processing speed in automotive, ultra-low power in wearable and IoT, interconnection and data reliability and post Moore Era.

As a leading company in 32-bit general MCU market, GigaDevice provided the low power, connectivity, security design in both ARM and RISC-V MCUs. In this speech, we will unveil our RISC-V core solutions and advantage design techniques, like modular design, user extension instructions and ecological development and active community, and the security design focus on code protection, data encryption, safe downloading, security boot and reliability design.

# Keynote V

Wednesday, January 15, 17:30-18:10

## “Emulation View of Synopsys Verification Continuum Platform”

**Michael Wang**

Synopsys

**Abstract**

Increasing System-on-Chip (SoC) complexity and software content combined with rising time-to-market pressures are driving the need for a next-generation verification solution that spans pre-silicon verification, post-silicon validation and early software bring-up.

Synopsys' Verification Continuum platform, developed in collaboration with market leaders, unites Synopsys' best-in-class verification solutions, facilitating a seamless transition between them and improving SoC time-to-market by months. Verification Continuum is architected with FPGA-based emulation and prototyping, delivering the speed and scalability required for software bring-up and SoC verification.

By natively integrating the industry’s fastest emulator, ZeBu Server 4, with other Synopsys’ verification engines in the Verification Continuum Platform, like Virtualizer virtual prototyping, VCS simulation, HAPS prototyping, SpyGlass static and Verdi debug, many effective emulation solutions are created and help improve design verification and software bring-up productivity significantly.

In addition, on top of the Verification Continuum Platform, Synopsys develops domain specific solutions, to meet special technical requests from Networking, AI and 5G sectors.

All above emulation technologies and solutions will be discussed in this presentation.

# Keynote VI

Thursday, January 16, 9:00-10:00

## “Explore the next tides of EDA”

**Lifeng Wu**

Empyrean Software

**Abstract**

EDA, one of the most critical pillars of semiconductor industry, has been supporting Moore’s law for four decades. On the other hand, recent EDA growth in last two decades is mostly driven by applications rather than fundamental breakthrough in EDA research. What are the possible directions for future EDA tides? From our point of view, computing platform (heterogeneous computing, Cloud computing, ARM-based massive-threading architecture) and AI based algorithm will provide more dimensions for EDA research.

We will demonstrate some solutions powered by heterogeneous computing platform and machine-learning algorithms.

## 1K Opening and Keynote Session I

Time: 9:00 - 10:30, Tuesday, January 14, 2020

Location: Room 311

1K-1 (Time: 9:30 - 10:30)

(Keynote Address) Skin Electronics for Continuous Health Monitoring

Takao Someya (Univ. of Tokyo, Japan)

## 1A University Design Contest

Time: 10:45 - 12:00, Tuesday, January 14, 2020

Location: Room 310

Chair: Dajiang Liu (Chongqing Univ.)

1A-1 (Time: 10:45 - 10:48)

Design of a Single-Stage Wireless Charger with 92.3%-Peak-Efficiency for Portable Devices Applications

*Lin Cheng (Univ. of Science and Tech. of China, China), Xinyuan Ge, Wai Chiu Ng, Wing-Hung Ki, Jiawei Zheng, Tsz Fai Kwok, Chi-Ying Tsui (Hong Kong Univ. of Science and Tech., China), Ming Liu (Institute of Microelectronics, Chinese Academy of Sciences,, China)

1A-2 (Time: 10:48 - 10:51)

A Capacitance-to-Digital Converter with Differential Bondwire Accelerometer, On-chip Air Pressure and Humidity Sensor in 0.18 um CMOS

Sujin Park (KAIST, Republic of Korea), Geon-Hwi Lee (KAIST/SK Hynix, Republic of Korea), *Seungmin Oh (KAIST, Republic of Korea)

1A-3 (Time: 10:51 - 10:54)

A 28GHz CMOS Differential Bi-Directional Amplifier for 5G NR

*Zheng Li, Jian Pang, Ryo Kubozoe, Xueting Luo, Rui Wu, Yun Wang, Dongwon You, Ashbir Aviat Fadila, Joshua Alvin, Bangan Liu, Zheng Sun, Hongye Huang, Atsushi Shirane, Kenichi Okada (Tokyo Inst. of Tech., Japan)

1A-4 (Time: 10:54 - 10:57)

A Quantity Evaluation and Reconfiguration Mechanism for Signal- and Power-Interconnections in 3D-Stacking System

*Ching-Hwa Cheng (Feng Chia Univ., Taiwan)

1A-5 (Time: 10:57 - 11:00)

An Inductively Coupled Wireless Bus for Chiplet-Based Systems

*Junichiro Kadomoto, Satoshi Mitsuno, Hidetsugu Irie, Shuichi Sakai (Univ. of Tokyo, Japan)

1A-6 (Time: 11:00 - 11:03)

FPGA-based Heterogeneous Solver for Three-Dimensional Routing

Kento Hasegawa, *Ryota Ishikawa, Makoto Nishizawa, Kazushi Kawamura, Masashi Tawada, Nozomu Togawa (Waseda Univ., Japan)

## 1B Machine Learning in Physical Design

Time: 10:45 - 12:00, Tuesday, January 14, 2020

Location: Room 308

Chair: Iris Hui-Ru Jiang (National Taiwan Univ.)

1B-1 (Time: 10:45 - 11:10)

PowerNet: Transferable Dynamic IR Drop Estimation via Maximum Convolutional Neural Network

*Zhiyao Xie (Duke Univ., USA), Haoxing Ren, Brucek Khailany, Ye Sheng, Santosh Santosh (Nvidia, USA), Jiang Hu (TAMU, USA), Yiran Chen (Duke Univ., USA)

1B-2 (Time: 11:10 - 11:35)

FIST: A Feature-Importance Sampling and Tree-Based Method for Automatic Design Flow Parameter Tuning

*Zhiyao Xie (Duke Univ., USA), Guan-Qi Fang, Yu-Hung Huang (National Taiwan Univ. of Science and Tech., Taiwan), Haoxing Ren, Yanqing Zhang, Brucek Khailany (Nvidia, USA), Shao-Yun Fang (National Taiwan Univ. of Science and Tech., Taiwan), Jiang Hu (TAMU, USA), Yiran Chen (Duke Univ., USA), Erick Carvajal Barboza (TAMU, USA)

1B-3 (Time: 11:35 - 12:00)
High-Definition Routing Congestion Prediction for Large-Scale FPGAs
Mohamed Baker Alawieh, Wuxi Li, *Yibo Lin (Univ. of Texas, Austin, USA), Love Singhal, Mahesh Iyer (Intel, USA), David Z. Pan (Univ. of Texas, Austin, USA)

## 1C Toward Optimal Timing and PDN Design

Time: 10:45 - 12:00, Tuesday, January 14, 2020
Location: Room 307A
Chairs: Yu-Guang Chen (National Central Univ., Taiwan), Jianglei Yang (Beihang Univ.)

1C-1 (Time: 10:45 - 11:10)
Integrated Airgap Insertion and Layer Reassignment for Circuit Timing Optimization
*Younggwang Jung, Daijoon Hyun, Youngsoo Shin (KAIST, Republic of Korea)

1C-2 (Time: 11:10 - 11:35)
An Adaptive Electromigration Assessment Algorithm for Full-chip Power/Ground Networks
*Shaobin Ma, Xiaoyi Wang (Beijing Univ. of Tech., China), Sheldon X.-D. Tan, Liang Chen (Univ. of California, Riverside, USA), Jian He (Beijing Univ. of Tech., China)

1C-3 (Time: 11:35 - 12:00)
Template-based PDN Synthesis in Floorplan and Placement Using Classifier and CNN Techniques
*Vidya A. Chhabria (Univ. of Minnesota, USA), Andrew B. Kahng, Minsoo Kim, Uday Mallappa (Univ. of California, San Diego, USA), Sachin S. Sapatnekar (Univ. of Minnesota, USA), Bangqi Xu (Univ. of California, San Diego, USA)

## 1D Side Channel Attacks and Countermeasures

Time: 10:45 - 12:00, Tuesday, January 14, 2020
Location: Room 307B
Chairs: Hiromitsu Awano (Osaka Univ., Japan), Song Bian (Kyoto Univ., Japan)

1D-1 (Time: 10:45 - 11:10)
Analyzing The Security of The Cache Side Channel Defences With Attack Graphs
*Limin Wang, Ziyuan Zhu, Zhanpeng Wang, Dan Meng (Chinese Academy of Sciences, China)

1D-2 (Time: 11:10 - 11:35)
iGPU Leak: An Information Leakage Vulnerability on Intel Integrated GPU
*Wenjian He, Wei Zhang (Hong Kong Univ. of Science and Tech., Hong Kong), Sharad Sinha (Indian Inst. of Tech. Goa, India), Sanjeev Das (Univ. of North Carolina, Chapel Hill, USA)

1D-3 (Time: 11:35 - 12:00)
Design for EM Side-Channel Security through Quantitative Assessment of RTL Implementations
*Jiaji He (Tsinghua Univ., China), Haocheng Ma (Tianjin Univ., China), Xiaolong Guo (Kansas State Univ., USA), Yiqiang Zhao (Tianjin Univ., China), Yier Jin (Univ. of Florida, USA)

## 2K Keynote Session II

Time: 12:00 - 12:40, Tuesday, January 14, 2020
Location: Room 311

2K-1 (Time: 12:00 - 12:40)
(Keynote Address) Edge-to-Cloud Innovations for Inclusive AI
Xiaoning Qi (Alibaba)

## 2A (SS-1): Designing Reliable and Robust Circuits and Systems in the Nanometer Era

Time: 14:00 - 15:40, Tuesday, January 14, 2020

Location: Room 310

Chair: Sheldon Tan (Univ. of California Riverside, USA)

2A-1 (Time: 14:00 - 14:25)

(Invited Paper) Impact of Self-Heating On Performance, Power and Reliability in FinFET Technology

Victor M. van Santen, Paul R. Genssler, Om Prakash, Simon Thomann, Jörg Henkel, *Hussam Amrouch (Karlsruhe Inst. of Tech., Germany)

2A-2 (Time: 14:25 - 14:50)

(Invited Paper) Reliable Power Grid Network Design Framework Considering EM Immortalities for Multi-Segment Wires

Han Zhou, Shuyuan Yu, Zeyu Sun, *Sheldon Tan (Univ. of California, Riverside, USA)

2A-3 (Time: 14:50 - 15:15)

(Invited Paper) Investigating the Inherent Soft Error Resilience of Embedded Applications by Full-System Simulation

Uzair Sharif, Daniel Müller-Gritschneder, *Ulf Schlichtmann (Tech. Univ. of Munich, Germany)

## 2B System Architecture Innovation

Time: 14:00 - 15:40, Tuesday, January 14, 2020

Location: Room 308

Chair: Eric Liang (Peking Universtiy)

2B-1 (Time: 14:00 - 14:25)

Co-Exploring Neural Architecture and Network-on-Chip Design for Real-Time Artificial Intelligence

*Lei Yang (Univ. of Pittsburgh, USA), Weiwen Jiang (Univ. of Notre Dame, USA), Weichen Liu (Nanyang Technological Univ., Singapore), Edwin Sha (East China Normal Univ., China), Yiyu Shi (Univ. of Notre Dame, USA), Jingtong Hu (Univ. of Pittsburgh, USA)

2B-2 (Time: 14:25 - 14:50)

Thanos: High-Performance CPU-GPU Based Graph Partitioning Using Cross-Decomposition

DaeHee Kim, Rakesh Nagi, *Deming Chen (Univ. of Illinois, Urbana-Champaign, USA)

2B-3 (Time: 14:50 - 15:15)

Reutilization of Trace Buffers for Performance Enhancement of NoC based MPSoCs

*Sidhartha Sankar Rout, Badri M, Sujay Deb (Indraprastha Institute of Information Technology, Delhi, India)

2B-4 (Time: 15:15 - 15:40)

Formal Semantics of Predictable Pipelines: a Comparative Study

Mathieu Jan, *Mihail Asavoae (CEA LIST, France), Martin Schoeberl (Tech. Univ. of Denmark, Denmark), Edward Lee (Univ. of California, Berkeley, USA)

## 2C Optical Networks-on-Chips and Quantum Circuit Design

Time: 14:00 - 15:40, Tuesday, January 14, 2020

Location: Room 307A

Chairs: Rudy Raymond H.P. (IBM Research, Japan), Shigeru Yamashita (Ritsumeikan Univ.)

2C-1 (Time: 14:00 - 14:25)

Maximizing the Communication Parallelism for Wavelength-Routed Optical Networks-on-Chips

*Mengchu Li, Tsun-Ming Tseng (Tech. Univ. of Munich, Germany), Mahdi Tala (Univ. of Ferrara, Italy), Ulf Schlichtmann (Tech. Univ. of Munich, Germany)

2C-2 (Time: 14:25 - 14:50)

Concurrency in DD-based Quantum Circuit Simulation

*Stefan Hillmich, Alwin Zulehner, Robert Wille (Johannes Kepler Univ. Linz Institute for Integrated Circuits, Austria)

2C-3 (Time: 14:50 - 15:15)
Approximation of Quantum States Using Decision Diagrams
Alwin Zulehner, Stefan Hillmich (Johannes Kepler Univ. Linz Institute for Integrated Circuits, Austria), Igor Markov (Univ. of Michigan, USA), *Robert Wille (Johannes Kepler Univ. Linz Institute for Integrated Circuits, Austria)

2C-4 (Time: 15:15 - 15:40)
Advanced Equivalence Checking of Quantum Circuits
*Lukas Burgholzer, Robert Wille (Johannes Kepler Univ. Linz, Austria)

## 2D Reliability from Design to Manufacturing

Time: 14:00 - 15:40, Tuesday, January 14, 2020
Location: Room 307B
Chair: Changhao Yan (Fudan Univ., China)

2D-1 (Time: 14:00 - 14:25)
Equivalent Capacitance Guided Dummy Fill Insertion for Timing and Manufacturability
*Sheng-Jung Yu, Chen-Chien Kao, Chia-Han Huang, Iris Hui-Ru Jiang (National Taiwan Univ., Taiwan)

2D-2 (Time: 14:25 - 14:50)
Synthesis of Hardware Performance Monitoring and Prediction Flow Adapting to Near-Threshold Computing and Advanced Process Nodes
*Jeongwoo Heo (Seoul National Univ., Republic of Korea), Kwangok Jeong (Samsung Electronics, Republic of Korea), Taewhan Kim, Kyumyung Choi (Seoul National Univ., Republic of Korea)

2D-3 (Time: 14:50 - 15:15)
Enhancing Generalization of Wafer Defect Detection by Data Discrepancy-aware Preprocessing and Contrast-varied Augmentation
Chaofei Yang (Duke Univ., USA), Jiang Hu (Texas A&M Univ., USA), Hai Li, *Yiran Chen (Duke Univ., USA)

2D-4 (Time: 15:15 - 15:40)
Exploring Graphical Models with Bayesian Learning and MCMC for Failure Diagnosis
*Hongfei Wang, Wenjie Cai, Jianwen Li, Kun He (Huazhong Univ. of Science and Tech., China)

## 3A Reliability and Security for Deep Neural Networks

Time: 16:00 - 17:15, Tuesday, January 14, 2020
Location: Room 310
Chair: Andrew Putnam (Microsoft, USA)

3A-1 (Time: 16:00 - 16:25)
Mitigating Adversarial Attacks for Deep Neural Networks by Input Deformation and Augmentation
*Pengfei Qiu (Tsinghua Univ., China), Qian Wang (Univ. of Maryland, College Park, USA), Yongqiang Lyu (Tsinghua Univ., China), Zhaojun Lu (Univ. of Maryland, College Park, USA), Dongsheng Wang (Tsinghua Univ., USA), Gang Qu (Univ. of Maryland, College Park, USA)

3A-2 (Time: 16:25 - 16:50)
When Single Event Upset Meets Deep Neural Networks: Observations, Explorations, and Remedies
Zheyu Yan (Zhejiang Univ., China), Yiyu Shi (Univ. of Notre Dame, USA), Wang Liao, Masanori Hashimoto (Osaka Univ., Japan), Xichuan Zhou (Chongqing Univ., China), *Cheng Zhuo (Zhejiang Univ., China)

3A-3 (Time: 16:50 - 17:15)
Concurrent Monitoring of Operational Health in Neural Networks Through Balanced Output Partitions
Elbruz Ozen, *Alex Orailoglu (Univ. of California, San Diego, USA)

## 3B Memory Architecture for Emerging Technologies

Time: 16:00 - 17:15, Tuesday, January 14, 2020

Location: Room 308

Chairs: Dongsuk Jeon (Seoul National Univ.), Xianzhang Chen (Chongqing Univ.)

3B-1 (Time: 16:00 - 16:25)

PARC: A Processing-in-CAM Architecture for Genomic Long Read Pairwise Alignment using ReRAM

*Fan Chen, Linghao Song, Hai Li, Yiran Chen (Duke Univ., USA)

3B-2 (Time: 16:25 - 16:50)

RRAM-VAC: A Variability-Aware Controller for RRAM-based Memory Architectures

*Shikhar Tuli, Marco Antonio Rios, Alexandre Levisse, David Atienza (Swiss Federal Inst. of Tech. (EPFL), Switzerland)

3B-3 (Time: 16:50 - 17:15)

Defects Mitigation in Resistive Crossbars for Analog Vector/Matrix Multiplication

*Fan Zhang, Miao Hu (Binghamton Univ., USA)

## 3C Techniques for Analog Circuits and NoC

Time: 16:00 - 17:15, Tuesday, January 14, 2020

Location: Room 307A

Chairs: Markus Olbrich (Leibniz Univ. Hannover, Germany), Fan Yang (Fudan Univ., China)

3C-1 (Time: 16:00 - 16:25)

$S^3$DET: Detecting System Symmetry Constraints for Analog Circuits with Graph Similarity

Mingjie Liu, Wuxi Li, Keren Zhu, Biying Xu, *Yibo Lin, Linxiao Shen, Xiyuan Tang, Nan Sun, David Z. Pan (Univ. of Texas, Austin, USA)

3C-2 (Time: 16:25 - 16:50)

Establishing Reachset Conformance for the Formal Analysis of Analog Circuits

*Niklas Kochdumper (Tech. Univ. of Munich, Germany), Ahmad Tarraf (Goethe Univ. Frankfurt, Germany), Malgorzata Rechmal (Leibniz Univ. Hannover, Germany), Matthias Althoff (Tech. Univ. of Munich, Germany), Lars Hedrich (Goethe Univ. Frankfurt, Germany), Markus Olbrich (Leibniz Univ. Hannover, Germany)

3C-3 (Time: 16:50 - 17:15)

Contention Minimized Bypassing in SMART NoC

*Peng Chen (Nanyang Technological Univ./Chongqing Univ., Singapore), Weichen Liu (Nanyang Technological Univ., Singapore), Mengquan Li (Nanyang Technological Univ./Chongqing Univ., Singapore), Lei Yang (Univ. of Pittsburgh, USA), Nan Guan (Hong Kong Polytechnic Univ., Hong Kong)

## 3D Advanced test, verification and fault tolerance techniques

Time: 16:00 - 17:15, Tuesday, January 14, 2020

Location: Room 307B

Chairs: Ying Zhang (Tongji Univ., China), Michihiro Shintani (NAIST, Japan)

3D-1 (Time: 16:00 - 16:25)

FTT-NAS: Discovering Fault-Tolerant Neural Architecture

*Wenshuo Li, Xuefei Ning, Guangjun Ge (Tsinghua Univ., China), Xiaoming Chen (Chinese Academy of Sciences, China), Yu Wang, Huazhong Yang (Tsinghua Univ., China)

3D-2 (Time: 16:25 - 16:50)

The Notion of Cross Coverage in AMS Design Verification

Sayandeep Sanyal, Aritra Hazra, *Pallab Dasgupta (Indian Inst. of Tech. Kharagpur, India), Scott Morrison (Texas Instruments, USA), Sudhakar Surendran (Texas Instruments, India), Lakshmanan Balasubramanian (Texas Instruments (India) Pvt., India)

3D-3 (Time: 16:50 - 17:15)

Automated Test Generation for Activation of Assertions in RTL Models

*Yangdi Lyu, Prabhat Mishra (Univ. of Florida, USA)

## SRF ACM SIGDA Student Research Forum at ASP-DAC 2020

Time: 18:15 - 20:00, Tuesday, January 14, 2020

Location: Room 308

Chairs: Hyung Gyu Lee (Daegu University, Korea)
Weichen Liu (Nanyang Technological University, Singapore)
Lei Jiang (Indiana University Bloomington, US)

SRF-1: LanCe: A Comprehensive and Lightweight CNN Defense Methodology against Physical Adversarial Attacks on Embedded Multimedia Applications
Zirui Xu (George Mason University)

SRF-2: Enhancing and Accelerating Design Automation with Machine Learning and Unified Optimization
Yuzhe Ma (The Chinese University of Hong Kong)

SRF-3: Response Time Analysis and Communication Optimization on NoC-based Multi-Core Platforms
Peng Chen (Chongqing University)

SRF-4: A Wear Leveling Aware Memory Allocator for Both Stack and Heap Management in PCM-based Main Memory Systems
Wei Li (Wuhan University)

SRF-5: Reducing Write Amplification for Inodes of Journaling File System using Persistent Memory
Chaoshu Yang（Chongqing University)

SRF-6: HyPar: Towards Hybrid Parallelism for Deep Learning Accelerator Array
Linghao Song (Duke University)

SRF-7: Archivist: A Machine Learning Assisted Data Placement Mechanism for Hybrid Storage Systems
Jinting Ren (Chongqing University)

SRF-8: EMC: Energy-aware Morphable Cache Design for Non-volatile Processors
Weining Song (Shandong University)

SRF-9: Statistical Property Enhancement in Memristor-based Physically Unclonable Functions with Timing Variability
Ha-Phuong Nguyen (Yeungnam University)

SRF-10: Astraea: Self-balancing Federated Learning for Improving Classification Accuracy of Mobile Deep Learning Applications
Moming Duan (Chongqing University)

SRF-11: Temperature Sensor Assisted Lifetime Enhancement of Satellite Embedded Systems via Multi-Core Task Mapping and DVFS
Beomsik Kim (Ajou university)

SRF-12: Test Generation for Hardware Security Validation
Yangdi Lyu (University of Florida)

SRF-13: Co-Design of Hardware Implementation and Training Framework for Neural Network-Inspired Analog-to-Digital Conversion
Weidong Cao (Washington University St. Louis)

SRF-14: Scaling SoC Verification through Instruction-Level Hardware Models
Yue Xing (Princeton University)

SRF-15: Modular SSD Firmware with ISP Framework and Security-Aware SPM Management
Thomas Haywood Dadzie (Hanyang University)

SRF-16: An Improved Parallel Floating Random Walk Based Capacitance Solver for VLSI and Flat Panel Display
Mingye Song (Tsinghua University)

SRF-17: Re-Tangle: A ReRAM-based Processing-in-Memory Architecture for Transaction-based Blockchain
Qian Wang (Shandong University)

SRF-18: Audio Adversarial Examples Generation with Recurrent Neural Networks
Po-Hao Huang (National Tsing Hua University)

## 3K Keynote Session III

Time: 9:00 - 10:00, Wednesday, January 15, 2020

Location: Room 311

3K-1 (Time: 9:00 - 10:00)

(Keynote Address) Design Automation for Customizable Computing

Jason Cong (Univ. of California, Los Angles, USA)

## 4A (DF-1): Trends in EDA

Time: 10:15 - 11:30, Wednesday, January 15, 2020

Location: Room 310

Chair: Bei Yu (Chinese Univ. of Hong Kong)

4A-1 (Time: 10:15 - 10:40)

(Designers' Forum) The Golden Age of EDA – Clock Design, Machine Learning and A-I Collaboration

Zhuo Li (Cadence design systems, USA)

4A-2 (Time: 10:40 - 11:05)

(Designers' Forum) New Trend on High-Level Synthesis and Customized Compiler for Edge Intelligence

Deming Chen (UIUC, USA)

4A-3 (Time: 11:05 - 11:30)

(Designers' Forum) Data-driven Instant Model Synthesis Enhanced by Learning Algorithms For DTCO Enablement In the FinFET Era

Yanfeng Li (Platform Design Automation, China)

## 4B Machine-Learning and Low-Power Design

Time: 10:15 - 11:30, Wednesday, January 15, 2020

Location: Room 308

Chairs: Cheng Zhuo (Zhejiang Univ., China), Hai Wang (UESTC, China)

4B-1 (Time: 10:15 - 10:40)

Machine Learning Based Online Full-Chip Heatmap Estimation

Sheriff Sadiqbatcha, Yue Zhao, Jinwei Zhang (Univ. of California, Riverside, USA), Hussam Amrouch, Joerg Henkel (Karlsruhe Inst. of Tech., Germany), *Sheldon Tan (Univ. of California, Riverside, USA)

4B-2 (Time: 10:40 - 11:05)

A Reconfigurable Approximate Multiplier for Quantized CNN Applications

*Chuliang Guo, Li Zhang, Xian Zhou (Zhejiang Univ., China), Weikang Qian (Shanghai Jiao Tong Univ., China), Cheng Zhuo (Zhejiang Univ., China)

4B-3 (Time: 11:05 - 11:30)

EFFORT: Enhancing Energy Efficiency and Error Resilience of a Near-Threshold Tensor Processing Unit

*Noel Daniel Gundi, Tahmoures Shabanian, Prabal Basu, Pramesh Pandey, Sanghamitra Roy, Koushik Chakraborty, Zhen Zhang (Utah State Univ., USA)

## 4C Cryptographic Hardware Implementation and Secure Approximate Computing

Time: 10:15 - 11:30, Wednesday, January 15, 2020

Location: Room 307A

Chair: Weiqiang Liu (Nanjing Univ. of Aeronautics and Astronautics, China)

4C-1 (Time: 10:15 - 10:40)

Towards Efficient Kyber on FPGAs: A Processor for Vector of Polynomials

*Zhaohui Chen (Univ. of Chinese Academy of Sciences, China), Yuan Ma, Tianyu Chen, Jingqiang Lin (Chinese Academy of Sciences, China), Jiwu Jing (Univ. of Chinese Academy of Sciences, China)

4C-2 (Time: 10:40 - 11:05)
Efficient Subquadratic Space Complexity Digit-Serial Multipliers over GF($2^m$) based on Bivariate Polynomial Basis Representation
Chiou-Yng Lee (Lunghwa Univ. of Science and Tech., Taiwan), *Jiafeng Xie (Villanova Univ., USA)

4C-3 (Time: 11:05 - 11:30)
Security Threats and Countermeasures for Approximate Arithmetic Computing
*Pruthvy Yellu, Mezanur Rahman Monjur, Timothy Kammerer, Dongpeng Xu, Qiaoyan Yu (Univ. of New Hampshire, USA)

## 4D Emerging Embedded Systems Architecture

Time: 10:15 - 11:30, Wednesday, January 15, 2020
Location: Room 307B

4D-1 (Time: 10:15 - 10:40)
Broadcast Mechanism Based on Hybrid Wireless/Wired NoC for Efficient Barrier Synchronization in Parallel Computing
Hemanta Kumar Mondal (National Inst. of Tech. Durgapur, India), *Navonil Chatterjee (Univ. de Bretagne Sud, France), Rodrigo Cataldo (PUCRS Univ., Brazil), Jean-Philippe Diguet (CNRS / Lab-STICC, France)

4D-2 (Time: 10:40 - 11:05)
A Generic FPGA Accelerator for Minimum Storage Regenerating Codes
Mian Qin (Texas A&M Univ., USA), Joo Hwan Lee, Rekha Pitchumani, Yang Seok Ki (Samsung Semiconductor, USA), Narasimha Reddy, *Paul V. Gratz (Texas A&M Univ., USA)

4D-3 (Time: 11:05 - 11:30)
Parallel-Log-Single-Compaction-Tree: Flash-Friendly Two-Level Key-Value Management in KVSSDs
*Yen-Ting Chen (National Tsing Hua Univ., Taiwan), Ming-Chang Yang (Chinese Univ. of Hong Kong, Hong Kong), Yuan-Hao Chang (Academia Sinica, Taiwan), Wei-Kuan Shih (National Tsing Hua Univ., Taiwan)

## 4K Keynote Session IV

Time: 11:30 - 12:10, Wednesday, January 15, 2020
Location: Room 311

4K-1 (Time: 11:30 - 12:10)
(Keynote Address) Huge Development of RISC-V Arising from IOT Spurt
Yingwu Zhang (GigaDevice, China)

## 5A Architecture and Algorithm for Deep Neural Networks

Time: 13:50 - 15:30, Wednesday, January 15, 2020
Location: Room 310
Chair: Deming Chen (UIUC)

5A-1 (Time: 13:50 - 14:15)
Towards Design Methodology of Efficient Fast Algorithms for Accelerating Generative Adversarial Networks on FPGAs
Jung-Woo Chang, *Saehyun Ahn, Keon-Woo Kang, Suk-Ju Kang (Sogang Univ., Republic of Korea)

5A-2 (Time: 14:15 - 14:40)
Designing Efficient Shortcut Architecture for Improving the Accuracy of Fully Quantized Neural Networks Accelerator
*Baoting Li, Longjun Liu, Yanming Jin, Peng Gao, Hongbin Sun, Nanning Zheng (Xi'an Jiaotong Univ., China)

5A-3 (Time: 14:40 - 15:05)
CRANIA: Unlocking Data and Value Reuse in Iterative Neural Network Architectures
Maedeh Hemmat, *Tejas Shah, Yuhua Chen, Joshua San Miguel (Univ. of Wisconsin Madison, USA)

5A-4 (Time: 15:05 - 15:30)

Tiny but Accurate: A Pruned, Quantized and Optimized Memristor Crossbar Framework for Ultra Efficient DNN Implementation

Xiaolong Ma, Geng Yuan, *Sheng Lin (Northeastern Univ., USA), Caiwen Ding (Univ. of Connecticut, USA), Fuxun Yu (George Mason Univ., USA), Tao Liu (Florida International Univ., USA), Wujie Wen (Lehigh Univ., USA), Xiang Chen (George Mason Univ., USA), Yanzhi Wang (Northeastern Univ., USA)

## 5B Advanced Memory Systems

Time: 13:50 - 15:30, Wednesday, January 15, 2020

Location: Room 308

Chairs: Ing-Chao Lin (National Cheng Kung Univ.), Guangyu Sun (Peking Univ.)

5B-1 (Time: 13:50 - 14:15)

Towards Read-Intensive Key-Value Stores with Tidal Structure Based on LSM-Tree

*Yi Wang, Shangyu Wu, Rui Mao (Shenzhen Univ., China)

5B-2 (Time: 14:15 - 14:40)

A Flexible Processing-in-Memory Accelerator for Dynamic Channel-Adaptive Deep Neural Networks

Li Yang (Arizona State Univ., USA), Shaahin Angizi (Univ. of Central Florida, USA), *Deliang Fan (Arizona State Univ., USA)

5B-3 (Time: 14:40 - 15:05)

Workload-aware Data-eviction Self-adjusting System of Multi-SCM Storage to Resolve Trade-off between SCM Data-retention Error and Storage System Performance

*Reika Kinoshita, Chihiro Matsui, Atsuya Suzuki, Shouhei Fukuyama, Ken Takeuchi (Chuo Univ., Japan)

5B-4 (Time: 15:05 - 15:30)

An Energy-Efficient Quantized and Regularized Training Framework For Processing-In-Memory Accelerators

*Hanbo Sun, Zhenhua Zhu, Yi Cai (Tsinghua Univ., China), Xiaoming Chen (Chinese Academy of Sciences, China), Yu Wang, Huazhong Yang (Tsinghua Univ., China)

## 5C Advances in Physical Design

Time: 13:50 - 15:30, Wednesday, January 15, 2020

Location: Room 307A

Chairs: Jiang Hu (TAMU), Jianli Chen (Fuzhou Univ.)

5C-1 (Time: 13:50 - 14:15)

Unified Redistribution Layer Routing for 2.5D IC Packages

Chun-Han Chiang, *Fu-Yu Chuang, Yao-Wen Chang (National Taiwan Univ., Taiwan)

5C-2 (Time: 14:15 - 14:40)

AIR: A Fast but Lazy Timing-Driven FPGA Router

*Kevin E. Murray, Shen Zhong, Vaughn Betz (Univ. of Toronto, Canada)

5C-3 (Time: 14:40 - 15:05)

SP&R: Simultaneous Placement and Routing Framework for Standard Cell Synthesis in Sub-7nm

Dongwon Park, *Daeyeal Lee (Univ. of California, San Diego, USA), Ilgweon Kang (Cadence, USA), Sicun Gao, Bill Lin, Chung-Kuan Cheng (Univ. of California, San Diego, USA)

5C-4 (Time: 15:05 - 15:30)

Chiplet-Package Co-Design For 2.5D Systems Using Standard ASIC CAD Tools

MD Arafat Kabir, *Yarui Peng (Univ. of Arkansas, USA)

## 5D System Simulation and Exploration

Time: 13:50 - 15:30, Wednesday, January 15, 2020

Location: Room 307B

Chairs: Weichen Liu (Nanyang Technological Univ., Singapore), Eric Liang (Peking Univ., China)

5D-1 (Time: 13:50 - 14:15)
Event Delivery using Prediction for Faster Parallel SystemC Simulation
*Zhongqi Cheng, Emad Arasteh, Rainer Doemer (Univ. of California, Irvine, USA)

5D-2 (Time: 14:15 - 14:40)
Standard-compliant Parallel SystemC simulation of Loosely-Timed Transaction Level Models
*Gabriel Busnot, Tanguy Sassolas, Nicolas Ventroux (CEA, LIST, Computing and Design Environment Laboratory, France), Matthieu Moy (Univ Lyon, EnsL, UCBL, CNRS, Inria, LIP, France)

5D-3 (Time: 14:40 - 15:05)
JIT-Based Context-Sensitive Timing Simulation for Efficient Platform Exploration
*Alessandro Cornaglia, Md Shakib Hasan, Alexander Viehl (FZI Research Center for Information Technology, Germany), Oliver Bringmann, Wolfgang Rosenstiel (Univ. of Tübingen, Germany)

5D-4 (Time: 15:05 - 15:30)
Towards Automatic Hardware Synthesis from Formal Specification to Implementation
*Fritjof Bornebusch, Christoph Lüth (German Research Center for Artificial Intelligence (DFKI), Germany), Robert Wille (Johannes Kepler Univ. Linz, Austria), Rolf Drechsler (Univ. of Bremen, Germany)

## 6A (SS-2): Computation-in-Memory based on emerging non-volatile memories: Technology, design, and test and reliability

Time: 15:45 - 17:00, Wednesday, January 15, 2020

Location: Room 310

Chair: Mehdi Tahoori (Faculty of Informatik, Karlsruhe Inst. of Tech. (KIT), Germany)

6A-1 (Time: 15:45 - 16:10)
(Invited Paper) Emerging Non-Volatile Memories for Computation-in-Memory
*Bin Gao (Tsinghua Univ., China)

6A-2 (Time: 16:10 - 16:35)
(Invited Paper) The Power of Computation-in-Memory Based on Memristive Devices
*Jintao Yu, Muath Abu Lebdeh, Hoang Anh Du Nguyen, Mottaqiallah Taouil, Said Hamdioui (Delft Univ. of Tech., Netherlands)

6A-3 (Time: 16:35 - 17:00)
(Invited Paper) Tolerating Retention Failures in Neuromorphic Fabric based on Emerging Resistive Memories
Christopher Münch (Karlsruhe Inst. of Tech., Germany), Rajendra Bishnoi (Delft Univ. of Tech., Netherlands), *Mehdi B. Tahoori (Karlsruhe Inst. of Tech., Germany)

## 6B (SS-3): Emerging Memory Enabled Computing in The Post-Moore's Era

Time: 15:45 - 17:25, Wednesday, January 15, 2020

Location: Room 308

Chair: Xueqing Li (Tsinghua Univ., China)

6B-1 (Time: 15:45 - 16:10)
(Invited Paper) Ferroelectrics: From Memory to Computing
*Kai Ni (Rochester Inst. of Tech., USA), Sourav Dutta, Suman Datta (Univ. of Notre Dame, USA)

6B-2 (Time: 16:10 - 16:35)
(Invited Paper) Adaptive Circuit Approaches to Low-Power Multi-Level/Cell FeFET Memory
Juejian Wu, Yixin Xu, Bowen Xue, Yu Wang, Yongpan Liu, Huazhong Yang, *Xueqing Li (Tsinghua Univ., China)

6B-3 (Time: 16:35 - 17:00)
(Invited Paper) Emerging Memories as Enablers for In-Memory Layout Transformation Acceleration and Virtualization 414
Minli Liao, *John (Jack) Sampson (Pennsylvania State Univ., USA)

6B-4 (Time: 17:00 - 17:25)
(Invited Paper) Benchmark Non-volatile and Volatile Memory Based Hybrid Precision Synapses for In-situ Deep Neural Network Training
Yandong Luo, *Shimeng Yu (Georgia Tech, USA)

## 6C (SS-4): AI Enhanced Simulation and Optimization in Back-End EDA Flow

Time: 15:45 - 17:00, Wednesday, January 15, 2020
Location: Room 307A
Chair: Wenjian Yu (Tsinghua Univ., China)

6C-1 (Time: 15:45 - 16:10)
(Invited Paper) Capacitance Extraction and Power Grid Analysis Using Statistical and AI Methods
*Wenjian Yu, Ming Yang, Yao Feng, Ganqu Cui (Tsinghua Univ., China), Ben Gu (Tsinghua Univ., USA)

6C-2 (Time: 16:10 - 16:35)
(Invited Paper) VLSI Mask Optimization: From Shallow To Deep Learning
*Haoyu Yang (Chinese Univ. of Hong Kong, Hong Kong), Wei Zhong (Dalian Univ. of Tech., China), Yuzhe Ma, Hao Geng, Ran Chen, Wanli Chen, Bei Yu (Chinese Univ. of Hong Kong, Hong Kong)

6C-3 (Time: 16:35 - 17:00)
(Invited Paper) Bayesian Methods for the Yield Optimization of Analog and SRAM Circuits
Shuhan Zhang, *Fan Yang (Fudan Univ., China), Dian Zhou (Univ. of Texas, Dallas, USA), Xuan Zeng (Fudan Univ., China)

## 6D (DF-2): Emerging Design

Time: 15:45 - 17:00, Wednesday, January 15, 2020
Location: Room 307B
Chair: Pingqiang Zhou (ShanghaiTech Univ.)

6D-1 (Time: 15:45 - 16:10)
(Designers' Forum) Recent Advances in Hardware Security and Testing Tools
Junfeng Fan (Open Security Research, Inc, China)

6D-2 (Time: 16:10 - 16:35)
(Designers' Forum) Design of Energy-Efficient Dynamic Reconfigurable Cryptographic Chip
Jinjiang Yang (Tsinghua Univ., China)

6D-3 (Time: 16:35 - 17:00)
(Designers' Forum) Cognitive SSD Controller: A Case for Agile Domain-Specific SoC Design
Ying Wang (Chinese Academy of Sciences, China)

## 5K Keynote Session V

Time: 17:30 - 18:10, Wednesday, January 15, 2020
Location: Room 311

5K-1 (Time: 17:30 - 18:10)
(Keynote Address) Emulation View of Synopsys Verification Continuum Platform
Michael Wang (Synopsys)

## 6K Keynote Session VI

Time: 9:00 - 10:00, Thursday, January 16, 2020

Location: Room 311

6K-1 (Time: 9:00 - 10:00)

(Keynote Address) Explore the Next Tides of EDA

Lifeng Wu (Empyrean Software)

## 7A Neuromorphic Computing

Time: 10:15 - 11:30, Thursday, January 16, 2020

Location: Room 310

Chair: Shinya Takamaeda-Yamazaki (Univ. of Tokyo)

7A-1 (Time: 10:15 - 10:40)

Programmable Neuromorphic Circuit based on Printed Electrolyte-Gated Transistors

*Dennis D. Weller, Michael Hefenbrock, Mehdi B. Tahoori (Karlsruhe Inst. of Tech., Germany), Jasmin Aghassi-Hagmann (Offenburg Univ. of Applied Sciences, Germany), Michael Beigl (Karlsruhe Inst. of Tech., Germany)

7A-2 (Time: 10:40 - 11:05)

HashHeat: An O(C) Complexity Hashing-based Filter for Dynamic Vision Sensor

Shasha Guo, *Ziyang Kang, Lei Wang, Shiming Li, Weixia Xu (National Univ. of Defense Tech., China)

7A-3 (Time: 11:05 - 11:30)

A Tuning-Free Hardware Reservoir Based on MOSFET Crossbar Array for Practical Echo State Network Implementation

*Yuki Kume, Song Bian, Takashi Sato (Kyoto Univ., Japan)

## 7B Machine Learning for Embedded Systems

Time: 10:15 - 11:30, Thursday, January 16, 2020

Location: Room 308

Chairs: Yongfu Li (Shanghai Jiao Tong Univ.), Huiyuan Song (Beijing Univ. of Tech.)

7B-1 (Time: 10:15 - 10:40)

MindReading: An Ultra Low-Power Nanophotonic Accelerator for EEG-based Intention Recognition

*Qian Lou (Indiana Univ. Bloomington, USA), Wenyang Liu, Weichen Liu (Nanyang Technological Univ., Singapore), Feng Guo, Lei Jiang (Indiana Univ. Bloomington, USA)

7B-2 (Time: 10:40 - 11:05)

LanCe: A Comprehensive and Lightweight CNN Defense Methodology against Physical Adversarial Attacks on Embedded Multimedia Applications

*Zirui Xu, Fuxun Yu, Xiang Chen (George Mason Univ., USA)

7B-3 (Time: 11:05 - 11:30)

Towards Area-Efficient Optical Neural Networks: An FFT-based Architecture

*Jiaqi Gu, Zheng Zhao, Chenghao Feng, Mingjie Liu, Ray T. Chen, David Z. Pan (Univ. of Texas, Austin, USA)

## 7C Malicious Activities Generation and Detection

Time: 10:15 - 11:30, Thursday, January 16, 2020

Location: Room 307A

Chairs: Xueyan Wang (Beihang Univ., China), Qiaoyan Yu (Univ. of New Hampshire, USA)

7C-1 (Time: 10:15 - 10:40)

Automated Trigger Activation by Repeated Maximal Clique Sampling

*Yangdi Lyu, Prabhat Mishra (Univ. of Florida, USA)

7C-2 (Time: 10:40 - 11:05)
Audio Adversarial Examples Generation with Recurrent Neural Networks
Kuei-Huan Chang, *Po-Hao Huang (National Tsing Hua Univ., Taiwan), Honggang Yu, Yier Jin (Univ. of Florida, USA), Ting-Chi Wang (National Tsing Hua Univ., Taiwan)

7C-3 (Time: 11:05 - 11:30)
Database and Benchmark for Early-stage Malicious Activity Detection in 3D Printing
*Xiaolong Ma (Northeastern Univ., USA), Zhe Li (Syracuse Univ., USA), Hongjia Li (Northeastern Univ., USA), Qiyuan An (Virginia Polytechnic Inst. and State Univ., USA), Qinru Qiu (Syracuse Univ., USA), Wenyao Xu (State Univ. of New York, Buffalo, USA), Yanzhi Wang (Northeastern Univ., USA)

## 7D Embedded Software for Energy Optimization and Non-Volatile Memory

Time: 10:15 - 11:30, Thursday, January 16, 2020
Location: Room 307B
Chairs: Hussam Amrouch (Karlsruhe Inst. of Tech.), Sarah Bing Li (Capital Normal Univ.)

7D-1 (Time: 10:15 - 10:40)
EA-HRT: An Energy-Aware scheduler for Heterogeneous Real-Time systems
*Sanjay Moulik, Rishabh Chaudhary, Zinea Das (IIIT Guwahati, India), Arnab Sarkar (IIT Guwahati, India)

7D-2 (Time: 10:40 - 11:05)
Insights and Optimizations on IR-drop Induced Sneak-Path for RRAM Crossbar-based Convolutions
*Yujie Zhu, Xue Zhao, Keni Qiu (Capital Normal Univ., China)

7D-3 (Time: 11:05 - 11:30)
Boosting the Profitability of NVRAM-based Storage Devices via the Concept of Dual-Chunking Data Deduplication
*Shuo-Han Chen (Academia Sinica, Taiwan), Yu-Pei Liang (National Tsing Hua Univ., Taiwan), Yuan-Hao Chang (Academia Sinica, Taiwan), Hsin-Wen Wei (Tamkang Univ., Taiwan), Wei-Kuan Shih (National Tsing Hua Univ., Taiwan)

## 8A Search and Optimization for Deep Neural Networks

Time: 13:50 - 15:30, Thursday, January 16, 2020
Location: Room 310
Chair: Li Jiang (Shanghai Jiao Tong Univ.)

8A-1 (Time: 13:50 - 14:15)
Black Box Search Space Profiling for Accelerator-Aware Neural Architecture Search
*Shulin Zeng, Hanbo Sun (Tsinghua Univ., China), Yu Xing (Tsinghua Univ., Xilinx, China), Xuefei Ning (Tsinghua Univ., China), Yi Shan (Xilinx, China), Xiaoming Chen (Chinese Academy of Sciences, China), Yu Wang, Huazhong Yang (Tsinghua Univ., China)

8A-2 (Time: 14:15 - 14:40)
Search-free Accelerator for Sparse Convolutional Neural Networks
*Bosheng Liu, Xiaoming Chen, Yinhe Han, Ying Wang, Jiajun Li, Haobo Xu, Xiaowei Li (Chinese Academy of Sciences, China)

8A-3 (Time: 14:40 - 15:05)
NESTA: Hamming Weigh Compression-Based Neural Proc. Engine
Ali Mirzaeian, Houman Homayoun (George Mason Univ., USA), *Avesta Sasan (Institute for Research in Fundamental Sciences, USA)

8A-4 (Time: 15:05 - 15:30)
Representable Matrices: Enabling High Accuracy Analog Computation for Inference of DNNs using Memristors
Baogang Zhang, Necati Uysal (Univ. of Central Florida, USA), Deliang Fan (Arizona State Univ., USA), *Rickard Ewetz (Univ. of Central Florida, USA)

## 8B FPGAs for Big Data Systems, Nonvolatile Computing, and Microfluidics

Time: 13:50 - 15:30, Thursday, January 16, 2020

Location: Room 308

Chairs: Tsun-Ming Tseng (Tech. Univ. of Munich, Germany), Xueqing Li (Tsinghua Univ., China)

8B-1 (Time: 13:50 - 14:15)

Reliability-Oriented IEEE Std. 1687 Network Design and Block-Aware High-Level Synthesis for MEDA Biochips

Zhanwei Zhong, Tung-Che Liang, *Krishnendu Chakrabarty (Duke Univ., USA)

8B-2 (Time: 14:15 - 14:40)

Optimal Fluid Loading on Programmable Microfluidic Devices for Bio-protocol Execution

Satoru Maruyama (Ritsumeikan Univ., Japan), Debraj Kundu (Indian Inst. of Tech. Roorkee, India), *Shigeru Yamashita (Ritsumeikan Univ., Japan), Sudip Roy (Indian Inst. of Tech. Roorkee, India)

8B-3 (Time: 14:40 - 15:05)

An FPGA based Network Interface Card with Query Filter for Storage Nodes of Big Data Systems

Ying Li, *Jinyu Zhan, Wei Jiang, Junting Wu (Univ. of Electronic Science and Tech. of China, China), Jianping Zhu (Tencent Technology Shenzhen, China)

8B-4 (Time: 15:05 - 15:30)

Nonvolatile and Energy-efficient FeFET-Based Multiplier for Energy-Harvesting Devices

*Mengyuan Li (Univ. of Notre Dame, USA), Xunzhao Yin (Zhejiang Univ., China), Xiaobo Sharon Hu (Univ. of Notre Dame, USA), Cheng Zhuo (Zhejiang Univ., China)

## 8C Advances in Logic/High-Level Synthesis

Time: 13:50 - 15:30, Thursday, January 16, 2020

Location: Room 307A

Chair: Bing Li (Tech. Univ. München)

8C-1 (Time: 13:50 - 14:15)

Modulo Scheduling with Rational Initiation Intervals in Custom Hardware Design

*Patrick Sittel (Univ. of Kassel, Germany), John Wickerson (Imperial College London, UK), Martin Kumm (Univ. of Applied Sciences Fulda, Germany), Peter Zipf (Univ. of Kassel, Germany)

8C-2 (Time: 14:15 - 14:40)

HL-Pow: A Learning-Based Power Modeling Framework for High-Level Synthesis

*Zhe Lin, Jieru Zhao (Hong Kong Univ. of Science and Tech., Hong Kong), Sharad Sinha (Indian Inst. of Tech. Goa, India), Wei Zhang (Hong Kong Univ. of Science and Tech., Hong Kong)

8C-3 (Time: 14:40 - 15:05)

DRiLLS: Deep Reinforcement Learning for Logic Synthesis

*Abdelrahman Hosny, Soheil Hashemi (Brown Univ., USA), Mohamed Shalan (American Univ. in Cairo, Egypt), Sherief Reda (Brown Univ., USA)

8C-4 (Time: 15:05 - 15:30)

Lightening Asynchronous Pipeline Controller Through Resynthesis and Optimization

*Jeongwoo Heo, Taewhan Kim (Seoul National Univ., Republic of Korea)

## 8D Scalable and Reconfigurable Approximate Arithmetic Units

Time: 13:50 - 15:30, Thursday, January 16, 2020

Location: Room 307B

Chairs: Jie Han (Univ. of Alberta, Canada), Weikang Qian (Shanghai Jiao Tong Univ.)

8D-1 (Time: 13:50 - 14:15)

WEID: Worst-Case Error Improvement in Approximate Dividers

*Hassaan Saadat (Univ. of New South Wales, Sydney, Australia), Haris Javaid (Xilinx, Singapore), Aleksandar Ignjatovic, Sri Parameswaran (Univ. of New South Wales, Sydney, Australia)

8D-2 (Time: 14:15 - 14:40)
Small-Area and Low-Power FPGA-Based Multipliers using Approximate Elementary Modules
*Yi Guo, Heming Sun, Shinji Kimura (Waseda Univ., Japan)

8D-3 (Time: 14:40 - 15:05)
LeAp: Leading-one Detection-based Softcore Approximate Multipliers with Tunable Accuracy
*Zahra Ebrahimi Mamaghani, Salim Ullah, Akash Kumar (Tech. Univ. Dresden, Germany)

8D-4 (Time: 15:05 - 15:30)
Scaled Population Arithmetic for Efficient Stochastic Computing
*He Zhou, Sunil Khatri, Jiang Hu (Texas A&M Univ., USA), Frank Liu (IBM Research, USA)

## 9A (SS-5): Resilience in Integrated Systems

Time: 15:45 - 17:00, Thursday, January 16, 2020

Location: Room 310

Chair: Masanori Hashimoto (Osaka Univ., Japan)

9A-1 (Time: 15:45 - 16:10)
(Invited Paper) Soft Error and Its Countermeasures in Terrestrial Environment
*Masanori Hashimoto (Osaka Univ., Japan), Wang Liao (Kochi Univ. of Tech., Japan)

9A-2 (Time: 16:10 - 16:35)
(Invited Paper) Timing Resilience for Efficient and Secure Circuits
Grace Li Zhang, Michaela Brunner, *Bing Li, Georg Sigl, Ulf Schlichtmann (Tech. Univ. of Munich, Germany)

9A-3 (Time: 16:35 - 17:00)
(Invited Paper) Run-Time Enforcement of Non-Functional Application Requirements in Heterogeneous Many-Core Systems
Jürgen Teich, Behnaz Pourmohseni, *Oliver Keszocze, Jan Spieck, Stefan Wildermann (Friedrich-Alexander-Univ. Erlangen-Nürnberg (FAU), Germany)

## 9B (SS-6): Emerging Technologies across the Abstraction Layers

Time: 15:45 - 17:00, Thursday, January 16, 2020

Location: Room 308

Chair: Hussam Amrouch (Karlsruhe Inst. of Tech. (KIT), Germany)

9B-1 (Time: 15:45 - 16:10)
(Invited Paper) NCFET to Rescue Technology Scaling: Opportunities and Challenges
*Hussam Amrouch, Victor M. van Santen (Karlsruhe Inst. of Tech., Germany), Girish Pahwa (Indian Inst. of Tech. Kanpur, India), Yogesh Chauhan (Indian Inst. of Tech. Kanpur, Germany), Jörg Henkel (Karlsruhe Inst. of Tech. (KIT), Germany)

9B-2 (Time: 16:10 - 16:35)
(Invited Paper) Parallelism in Deep Learning Accelerators
*Linghao Song, Fan Chen, Yiran Chen, Hai (Helen) Li (Duke Univ., USA)

9B-3 (Time: 16:35 - 17:00)
(Invited Paper) Software-Based Memory Analysis Environments for In-Memory Wear-Leveling
*Christian Hakert, Kuan-Hsun Chen, Mikail Yayla, Georg von der Brueggen, Sebastian Bloemeke, Jian-Jia Chen (TU Dortmund, Germany)

## 9C (SS-7): CMOS Annealing Hardware: Pursuing Efficiency for Solving Combinatorial Optimization Problems

Time: 15:45 - 17:00, Thursday, January 16, 2020

Location: Room 307A

Chair: Shu Tanaka (Waseda Univ., Japan)

9C-1 (Time: 15:45 - 16:10)

(Invited Paper) Digital Annealer for High-Speed Solving of Combinatorial Optimization Problems and Its Applications 659

*Satoshi Matsubara, Motomu Takatsu, Toshiyuki Miyazawa, Takayuki Shibasaki, Yasuhiro Watanabe, Kazuya Takemoto, Hirotaka Tamura (Fujitsu Labs., Japan)

9C-2 (Time: 16:10 - 16:35)

(Invited Paper) CMOS Annealing Machine: A Domain-Specific Architecture for Combinatorial Optimization Problem 665

*Chihiro Yoshimura, Masato Hayashi, Takashi Takemoto, Masanao Yamaoka (Hitachi, Japan)

9C-3 (Time: 16:35 - 17:00)

(Invited Paper) Theory of Ising Machines and a Common Software Platform for Ising Machines

*Shu Tanaka (Waseda Univ., Japan), Yoshiki Matsuda (Fixstars, Japan), Nozomu Togawa (Waseda Univ., Japan)

## 9D (DF-3): AI Accelerators

Time: 15:45 - 17:00, Thursday, January 16, 2020

Location: Room 307B

Chair: Xiaoming Chen (Chinese Academy of Sciences)

9D-1 (Time: 15:45 - 16:10)

(Designers' Forum) AI Chips, What's Next: Architecture, Tools, and Methodology

Shan Tang (AI chip expert, China)

9D-2 (Time: 16:10 - 16:35)

(Designers' Forum) Computing-in-Memory SoC Chip for Neural Network Inference

Shaodi Wang (Witin Tech, China)

9D-3 (Time: 16:35 - 17:00)

(Designers' Forum) Enabling Data Center-Wide Accelerator Resource Pools for AI Applications

Kun Wang (VirtAI Tech)

## Exhibition

Supporter's exhibition is held by thirteen companies which support ASP-DAC 2020 and have exhibition booths. The supporter's exhibition is presented at China National Convention Center 3F North Foyer from January 13 through January 16.

**Exhibit Hours: 9:00-17:00, January 13 / 9:00-17:00, January 14 /**
**9:00-17:00, January 15 / 9:00-17:00, January 16**
**Location: China National Convention Center 3F North Foyer**

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|  www.synopsys.com | Synopsys technology is at the heart of innovations that are changing the way we work and play. Autonomous vehicles. Artificial intelligence. The cloud. 5G. These breakthroughs are ushering in the era of Smart, Secure Everything—where devices are getting smarter, everything's connected, and everything must be secure.<br><br>Powering this new era of digital innovation are advanced silicon chips and exponentially growing amounts of software content—all working together, smartly and securely. Synopsys is at the forefront of Smart, Secure Everything with the world's most advanced technologies for chip design and verification, IP integration, and software security and quality testing. We help our customers innovate from silicon to software so they can deliver Smart, Secure Everything. |
|  www.gigadevice.com | Founded in 2005, GigaDevice Semiconductor Inc. is headquartered in Beijing, China with more than 800 employees. It has successfully completed the IPO at Shanghai Stock Exchange in August, 2016. GigaDevice is a leading fabless semiconductor company engaged in advanced memory technology and IC solutions. It has established the global sales network with branches and offices in various regions and countries including Beijing, Shanghai, Shenzhen, Hefei, Xi'an, Chengdu, Suzhou, Taiwan, U.S., South Korea, Japan, U.K. and Singapore, enabling quality and convenient local support services to customers.<br><br>The key product lines of GigaDevice include FLASH memory, 32-bit general-purpose MCU. Known for its "high performance, low power", GigaDevice provides turnkey services for customers from industry, automotive, computing, consumer, IoT, mobile application to network/telecommunications. GigaDevice currently has the largest share in China's SPI NOR FLASH® market, while ranking Top 3 suppliers globally with the accumulated shipments over 10 billion and annual shipments over 2 billion in units. GigaDevice's GD32 MCUs, with a top-ranking coverage of 330 parts in 23 series and 300 million units shipped in total, have been deemed as the mainstream 32-bit general purpose MCU products in China. |
|  https://www.xilinx.com/ | Xilinx is the inventor of the FPGA, programmable SoCs, and now, the ACAP. Our highly-flexible programmable silicon, enabled by a suite of advanced software and tools, drives rapid innovation across a wide span of industries and technologies - from consumer to cars to the cloud. Xilinx delivers the most dynamic processing technology in the industry, enabling rapid innovation with its adaptable, intelligent computing. |

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| https://www.alibaba.com/ | ALIBABA GROUP'S MISSION IS TO MAKE IT EASY TO DO BUSINESS ANYWHERE.<br>We enable businesses to transform the way they market, sell and operate and improve their efficiencies. We provide the technology infrastructure and marketing reach to help merchants, brands and other businesses to leverage the power of new technology to engage with their users and customers and operate in a more efficient way. |
| http://witin.net/ | WITIN Tech was founded in October 2017, dedicated in computing-in-memory technology development， leveraging the analog property of non-volatile memories to do massive matrix related computation. It eliminates the data accessing bottleneck, so-called "memory wall", boosting performance and efficiency by 15-100X. WITIN Tech has released MemCore001/MemCore001+ chips for low-power real-time smart voice applications, such as voice commands recognition, voice-print recognition, noise cancelation, and etc. |
| http://www.platform-da.com/en/ | Platform Design Automation, Inc. （PDA） provides EDA tools and a comprehensive set of services to facilitate designs using highly scaled technologies. Our years of experiences in device modeling, PDK and cell library as well as our unique EDA platform technology enable us to ensure accurate and robust design inputs including device models, PDK and cell libraries. Our EDA tools in device modeling, PDK and device characterization solutions are based on the latest technology and grow rapidly in recent years. PDA HQ is in Beijing, and has branch offices in Shanghai and Taiwan Hsinchu. |
| https://www.jeejio.com/en | Born in 2018, Jeejio is a young startup, founded by leading experts from both industry and academia, including Intel, Chinese Academy of Sciences, Tsinghua University, Peking University, and National University of Singapore.<br>We are building a new type of small yet powerful, AI-enabling computers meant for constructing novel and innovative IoT hardware devices and applications.<br>We have a vertically integrated team: at the bottom level, we design our own IoT AI chips; with those, we build lean-and-mean tiny machines; on top of that, we work on system softwares and cloud-based platforms that seek to make programmers' work joyful experiences; and with these powerful little machines, we build new hardware devices that showcase the machines' capabilities and deliver, we hope, novel, productive, diverse, and enjoyable user experiences. |
| https://virtai.tech/ | VirtAI Tech is a software startup company based at Beijing, China. Its product helps customers build and manage data-center-wide high-efficient and high-performance AI accelerator resource pools, so that customers can deploy and run their AI applications on any server in the data center, and access any AI accelerators (GPUs, FPGAs and ASICs) in the data center, no matter local accelerators or remote accelerators. VirtAI Tech software not only makes application deployment much more easier and flexible, but also improve the utilization of both CPUs and accelerators in the data center. |
| https://www.empyrean-tech.com/ | Empyrean Software, founded in 2009, is an EDA and service provider to the global semiconductor industry. Empyrean Software is a trusted technology leader serving fabless semiconductor design houses and IDMs throughout Asia, North America and Europe with unique and best in class design solutions.<br>In the EDA domain, Empyrean Software provides analog and mixed-signal IC design solutions, SoC design optimization solutions, foundry EDA and flat panel display (FPD) design solutions, delivering innovative and high quality products addressing advanced node challenges.<br>Empyrean Software also provides EDA related services such as IP design and foundry design enablement services. IP design includes IP licensing, customization, and design from spec. Foundry design enablement service includes SPICE modeling and PDK, SRAM test chip, cell library & memory compiler development.<br>Empyrean is headquartered in Beijing, with major R&D centers in Nanjing, Chengdu, Shanghai and Shenzhen in China. Additional branches offering sales and support are located at Taiwan, Japan, Singapore, South Korea and North America. |

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| http://www.icfc.tsinghua.edu.cn/ | Beijing Innovation Center for Future Chips (ICFC) is one of the first “Beijing University Innovation of Excellence Centers” certified by Beijing Municipal Education Commission in 2015. Relying on Tsinghua University’s advantages in disciplines, research and personnel, the Center – which is jointly set up by Beijing government and Tsinghua University – focuses on disruptive, innovative key devices, chips and micro-system technology. The Center is committed to building a top-tier talent team and a global open chip technology support platform, so as to promote the leapfrog development of Beijing’s IC industry and dedicated in serving China’s innovation-driven development strategy and Beijing’s innovation and technology center initiative. |
| http://www.pi2star.com/ | Pi2Star Technology Ltd. was founded in April 2018. The founder team is all from Tsinghua University. Based on the world's leading energy-efficient AI chips and high-precision AI algorithms, PI2STAR has built a four-in-one product matrix of the STARCORE, the STARDUST, the NEBULA, and the ASTROLOGY. As the industry's leading equipment intelligent management service provider, PI2STAR provides customers with cross-category, full-stack equipment management AIoT solutions to achieve quality improvement, cost reduction, efficiency increase, and risk control of production operations. As an enabler of the "Industry 4.0" era, Pi2Star has refined the two core capabilities of industrial interconnection and intelligent upgrade, and has continued to create "Smart +" made in China. |
| https://jiagu.360.cn/ | Founded in 2005, 360 is a leader in global cyber security. In terms of talent and technology, 360 forms the largest "White Hat Corps" in the Eastern Hemisphere, with world-class technology of vulnerability discovery and network attack and defense. 360 is a company that finds the largest quantity of vulnerability and APT in the world. At the same time, 360 accumulates the most comprehensive and up-to-date security big data. By the end of 2019, 360 owns more than 25 billion samples of program files and more than 22 trillion of program behavior logs.<br>The Polaris team is a research team of Qihoo 360 that dedicated to the security research of internet of things (IoT). The Polaris team`s research covers IoT device security、 IoT system security、 IoT application security、 IoT communication security and IoT cloud computing security. The Polaris team also provides professional security solutions to smart cars, smart homes, smart wearable devices, smart controlling and other IoT related fields. |

# Information

**Proceedings:**

ASP-DAC 2020 will be producing an authority to access the download site for the conference proceedings. The site will be open on Jan. 11, 2020. A USB memory include the conference proceedings will be provided.

**Banquet:**

Conference registrants are invited to attend a banquet to be held on January 15, 2020. The banquet will start at 18:30 in China National Convention Center Room 311. Conference registrants will receive a ticket to the banquet when they register at the conference.

**Currency Exchange:**

Only Renminbi (RMB)is acceptable at regular stores and restaurants. Certain foreign currencies may be accepted limited number of hotels, restaurants and souvenir shops.

**Payment and credit cards:**

VISA, MasterCard are widely accepted at hotels, department stores, shops, restaurants and nightclubs. WeChat payment and Alipay can be widely used.

**Tipping:**

In China, tips are not necessary anywhere, even at hotels and restaurants.

**Subway information:**

Participants can get Beijing-subway information from “https://www.bjsubway.com/en/”.

**Electricity:**

Electric voltage is uniformly 220 volts, AC, throughout China. Leading hotels in major cities only have outlets of 220 volts and their sockets usually accept both two- leg plug and three-leg plug.

**Shopping:**

Shops and other sales outlets in China are generally open on Saturdays, Sundays and national holidays as well as weekdays. Some convenience stores offer 24-hour service.

**Wi-Fi Information:**

Free Wi-Fi named “CNCC-FREE” is provided in China National Convention Center.

**Other Information:**

Participants can get other information at the check-in desk in the Conference site during the Conference period.

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# MEMO

# MEMO

# Call for Papers
# ASP-DAC 2021

**http://www.aspdac.com/**
**January 18-21, 2021**
**Tokyo, Japan**

**Aims of the Conference:**
ASP-DAC 2021 is the 26th annual international conference on VLSI design automation in Asia and South Pacific regions, one of the most active regions of design and fabrication of silicon chips in the world. The conference aims at providing the Asian and South Pacific CAD/DA and Design community with opportunities of presenting recent advances and with forums for future directions in technologies related to Electronic Design Automation (EDA). The format of the meeting intends to cultivate and promote an instructive and productive interchange of ideas among EDA researchers/developers and system/circuit/device designers. All scientists, engineers, and students who are interested in theoretical and practical aspects of VLSI design and design automation are welcomed to ASP-DAC.

**Areas of Interest:**
Original papers in, but not limited to, the following areas are invited.

**[1] System-Level Modeling and Design Methodology:**
1.1. HW/SW co-design, co-simulation and co-verification
1.2. System-level design exploration, synthesis, and optimization
1.3. System-level formal verification
1.4. System-level modeling, simulation and validation tools/methodology

**[2] Embedded Systems and Cyberphysical Systems:**
2.1. Many- and multi-core SoC architecture
2.2. IP/platform-based SoC design
2.3. Domain-specific architecture
2.4. Dependable architecture
2.5. Cyber physical system
2.6. Internet of things

**[3] Embedded Systems Software:**
3.1. Kernel, middleware, and virtual machine
3.2. Compiler and toolchain
3.3. Real-time system
3.4. Resource allocation for heterogeneous computing platform
3.5. Storage software and application
3.6. Human-computer interface

**[4] Memory Architecture and Near/In Memory Computing:**
4.1. Storage system and memory architecture
4.2. On-chip memory architectures and management: Scratchpads, compiler, controlled memories, etc.
4.3. Memory and storage hierarchies with emerging memory technologies
4.4. Near-memory and in-memory computing
4.5. Memory architecture and management for emerging memory technologies

**[5] AI/Machine Learning System Designs:**
5.1. Hardware and devices for neuromorphic and neural network computing
5.2. Design method for learning on a chip
5.3. Systems for neural computing (including deep neural networks)
5.4. Neural network acceleration co-design techniques
5.5. Design techniques for AI of Things

**[6] Analog/Mixed-Signal Design, Simulation and Validation:**
6.1. Analog/mixed-signal/RF synthesis
6.2. Analog layout, verification, and simulation techniques
6.3. High-frequency electromagnetic simulation of circuit
6.4. Mixed-signal design consideration
6.5. Communication architectures using nanophotonics, RF, 3D, etc.
6.6. Networks-on-chip and NoC-based system design

**[7] Approximate, Stochastic and Neuromorphic Computing:**
7.1. Circuit and system techniques for approximate computing
7.2. Stochastic computing for AI/ML
7.3. CAD for approximate and stochastic systems
7.4. Neuromorphic computing for AI/ML
7.5. CAD for bio-inspired and neuromorphic systems

**[8] Logic/High-Level Synthesis and Optimization:**
8.1. High-level synthesis tool and methodology
8.2. Combinational, sequential and asynchronous logic synthesis
8.3. Logic synthesis and physical design technique for FPGA
8.4. Technology mapping

**[9] Physical Design:**
9.1. Floorplanning, partitioning and placement
9.2. Interconnect planning and synthesis
9.3. Placement and routing optimization
9.4. Clock network synthesis
9.5. Post layout and post-silicon optimization
9.6. Package/PCB/3D-IC routing

**[10] Design for Manufacturability and Reliability:**
10.1. Reticle enhancement, lithography-related design and optimization
10.2. Resilience under manufacturing variation
10.3. Design for manufacturability, yield, and defect tolerance
10.4. Reliability, aging and soft error analysis
10.5. Design for reliability, aging, and robustness
10.6. Machine learning for smart manufacturing and process control

**[11] Design and Analysis for Timing and Low Power:**
11.1. Power modeling, analysis and simulation
11.2. Low-power design and optimization at circuit and system levels
11.3. Thermal aware design and dynamic thermal management
11.4. Energy harvesting and battery management
11.5. Deterministic/statistical timing analysis and optimization
11.6. 2D/3D on-chip power/ground and package modeling, analysis and optimization
11.7. Signal/power integrity, EM modeling and analysis
11.8. Extraction, TSV and package modeling

**[12] Testing, Validation, Simulation, and Verification:**
12.1. ATPG, BIST and DFT
12.2. System test and 3D IC test
12.3. Online test and fault tolerance
12.4. Memory test and repair
12.5. RTL and gate-leveling modeling, simulation, and verification
12.6. Circuit-level formal verification
12.7. Device/circuit-level simulation tool and methodology

**[13] Hardware and Embedded Security:**
13.1. Hardware-based security
13.2. Detection and prevention of hardware Trojans
13.3. Side-channel attacks, fault attacks and countermeasures
13.4. Design and CAD for security
13.5. Cyberphysical system security
13.6. Nanoelectronic security
13.7. Supply chain security and anti-counterfeiting

**[14] Emerging Technologies and Applications:**
14.1. Biomedical, biochip, and biodata processing.
14.2. Big/thick data, datacenter
14.3. Advanced multimedia application
14.4. Energy-storage/smart-grid/smart-building design and optimization
14.5. Automotive system design and optimization
14.6. New transistor/device and process technology: spintronic, phase-change, single-electron etc.
14.7. Nanotechnology, MEMS, quantum computing etc.

*Please note that each paper shall be accompanied by at least one different conference registration at the speaker's registration rate (e.g., two speaker registrations are needed for presenting two accepted papers). But any registered co-author can present the work at the conference. ACM and IEEE reserve the right to exclude a paper from distribution after the conference (e.g., removal from ACM Digital Library and IEEE Xplore) if the paper is not presented at the conference by the author of the paper. ASP-DAC does not allow double and/or parallel submissions of similar work to any other conferences, symposia, and journals.*

**Submission of Papers:**

| | | |
|---|---|---|
| Deadline for submission: | **5 PM AOE (Anywhere on earth)** | **Jul. 26 (Sun), 2020** |
| Notification of acceptance: | | **Sep. 13 (Sun), 2020** |
| Deadline for final version: | **5 PM AOE (Anywhere on earth)** | **Nov. 6 (Fri), 2020** |

For detailed instructions for submission, please refer to the "Authors' Guide" at: **http://www.aspdac.com/**

**ASP-DAC 2021 Chairs**

| | |
|---|---|
| **General Co-Chairs:** | **Toshihiro Hattori (Renesas Electronic Corporation)** |
| **Technical Program Chair:** | **Sheldon Tan (University of California, Riverside)** |
| **Technical Program Vice Chairs:** | **Masanori Hashimoto (Osaka University)** |

**Panels, Special Sessions, and Tutorials:** Suggestions and proposals are welcome and have to be addressed to the Conference Secretariat (aspdac2021@aspdac.com) no later than August 2 (Sunday), 2020.
**Contact:** Conference Secretariat: aspdac2021@aspdac.com TPC Secretariat: tpc@aspdac21.com

# Call for Designs

## University LSI Design Contest
## ASP-DAC 2021

http://www.aspdac.com/
January 18-21, 2021
Tokyo, Japan

**Aims of the Contest:**

As a unique feature of ASP-DAC 2021, the University LSI Design Contest will be held. The aim of the Contest is to encourage education and research on VLSI design at universities and other educational organizations. We solicit designs that fit in one or more of the following categories:

(1) Designed, and actually implemented on chips in universities or other educational organizations during the last two years;
(2) Designs that report actual measurements from implementations;
(3) Innovative design prototypes.

Interesting or excellent designs selected will be honored by providing the opportunities for presentation in a special session at the conference. Award(s) will be given to a few numbers of outstanding designs, selected from those presented at the conference.

**Areas of Design:**

Application areas or types of circuits of the original LSI circuit designs include (but are not limited to):
(1) Analog, RF and Mixed-Signal Circuits, (2) Digital Signal Processing, (3) Microprocessors, (4) Custom ASIC.
Methods or technology used for implementation include:
(a) Custom ASIC and Cell-Based LSIs, (b) Gate Arrays, (c) FPGA/PLDs.

**Submission of Design Descriptions:**

A camera-ready summary is requested to be prepared within 2 pages including figures, tables, and references. It is strongly recommended that measured experimental results and a chip micrograph are included in the summary. Please do not submit the same paper as a regular paper.

Specification of the submission format will be available at **http://www.aspdac.com/**

| | | |
|---|---|---|
| **Deadline for summary:** | 5 PM AOE (Anywhere on earth) | July 26 (Sun), 2020 |
| **Notification of acceptance:** | | Sep. 13 (Sun), 2020 |
| **Deadline for camera-ready:** | 5 PM AOE (Anywhere on earth) | Nov. 6 (Fri), 2020 |

**Review:**

Submitted designs will be reviewed by the Design Contest Committee in a process similar to the review process for the technical papers. The following criteria will be applied in the selection of designs:
(1) Reliability of design and implementation, (2) Quality of implementation, (3) Performance of the design,
(4) Novelty of application, algorithm, architecture, (5) Others.
Interesting or excellent designs selected will be presented at a special session of the conference.

**Presentation:**

An author of each selected design will be required to make a short presentation at a special session of ASP-DAC 2021. A digest of each design to be presented will be included in the conference proceedings.

**Contact Email: aspdac2021-udc@aspdac.com**

**ASP-DAC 2021 Chairs**

| | |
|---|---|
| **General Chair:** | **Toshihiro Hattori (Renesas Electronics Corp., Japan)** |
| **Technical Program Chair:** | **Sheldon Tan (University of California, Riverside, USA)** |
| **Technical Program Vice Chair:** | **Masanori Hashimoto (Osaka University, Japan)** |
| **Design Contest Co-Chairs:** | **Kousuke Miyaji (Shinshu University, Japan)** |
| | **Akira Tsuchiya (The University of Shiga Prefecture, Japan)** |

**Prospective Sponsors: ACM SIGDA, IEEE CASS, IEEE CEDA, IEICE ESS, IPSJ SIGSLDM**