Advancements and Challenges on Parasitic Extraction for Advanced Process Technologies

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Speaker’s bio

Dr. Wenjian Yu is a tenured Associate Professor with the Department of Computer Science and Technology, Tsinghua University, Beijing, China. His current research interests include physical-level modeling and simulation techniques for IC design, high-performance numerical algorithms, and Big-Data analytics and machine learning. Dr. Yu has coauthored two books and over 150 papers in refereed journals and conferences. He was the recipient of the distinguished Ph.D. Award from Tsinghua University in 2004, the Excellent Young Scientist Award from the National Science Foundation of China in 2014. He received the Best Paper Awards of DATE'2016, ACES'2017 and ICTAI'2019, and 5 Best Paper Award Nominations in DATE, ASPDAC, ISQED and GLSVLSI.
Outline

- Background
- Recent Advancements on Parasitic Extraction
  - Enhancements to the FRW based capacitance solver
  - Machine-learning based parasitic extraction/electrostatic analysis
  - Other related work
- Challenges for Advanced Process Technologies
- Conclusions
Accurate parasitic extraction is crucial to the success of today’s high-performance IC design.

- Parasitics refer to resistance (R) and capacitance (C) among interconnects, which are the key factors affecting signal delay and other performance.
- Parasitic extraction means calculating these R and C values.
- Capacitance extraction is of major concern, due to the massive couplings among millions of on-chip interconnect segments.
Background

◆ Two kinds of methods
  ➢ Electrostatic field solver
    • The best accuracy, with excessive computing time and memory cost
    • Can’t be applied to the whole design
    • A building block of pattern matching based method
    • For accurate analysis and calibration
  ➢ Pattern matching based method
    • Suitable for large or full-chip layout
    • Adopted in the industrial PEX tools
    • Not sufficiently good accuracy, for structures under advanced process technology
Directly applying 3-D capacitance field solver to the design is more demanded

- Finite difference/finite element method
  - Stable, versatile; slow
- Boundary element method
  - Fast, handle complex geometry
  - Not scalable; discretization quality affects accuracy
- Floating random walk method
  - No discretization of problem domain (stable accuracy)
  - Suitable for large problem (low memory cost)
  - Embarrassingly parallel
  - Restriction on geometry

\[ \nabla^2 \phi = 0 \]
\[ C_{ij} = Q_j = \int_{\Gamma_j} \varepsilon \frac{\partial \phi}{\partial n} ds \]

Raphael, COMSOL

xACT3D, Q3D, FastCap, QBEM

QuickCap, RWCap
Background

◆ The basics of FRW method

➢ Integral formula for the electrostatic potential

\[ \phi(r) = \oint_{S_1} P_1(r, r^{(1)}) \phi(r^{(1)}) ds^{(1)} \]

\( P_1 \) is called surface Green's function, and can be regarded as a probability density function

➢ Monte Carlo method: \( \phi(r) = \frac{1}{M} \sum_{m=1}^{M} \phi_m \)

\( \phi_m \) is the potential of a point on \( S_1 \), randomly sampled with \( P_1 \)

➢ What if \( \phi_m \) is unknown? expand the integral recursively

\[ \phi(r) = \oint_{S_1} P_1(r, r^{(1)}) \oint_{S_2} P_1(r^{(1)}, r^{(2)}) \cdots \]

\[ \oint_{S_k} P_1(r^{(k-1)}, r^{(k)}) \phi(r^{(k)}) ds^{(k)} \cdots ds^{(2)} ds^{(1)} \]

This spatial sampling procedure is called floating random walk
The Markov random process + MC method prove the correctness

A 2-D example with 3 walks

- Use maximal cubic transition domain

How to calculate capacitances?

$$
\begin{bmatrix}
C_{11} & C_{12} & C_{13} \\
C_{12} & C_{22} & C_{23} \\
C_{13} & C_{23} & C_{33}
\end{bmatrix}
\begin{bmatrix}
V_1 \\
V_2 \\
V_3
\end{bmatrix} =
\begin{bmatrix}
Q_1 \\
Q_2 \\
Q_3
\end{bmatrix}
$$

$$Q_1 = C_{11}V_1 + C_{12}V_2 + C_{13}V_3$$

Integral for calculating charge (Gauss theorem)

$$Q_1 = \oint_{G_1} F(r) \cdot \hat{n} \cdot \nabla \phi(r) \, dr = \oint_{G_1} F(r) \cdot \hat{n} \cdot \nabla \int_{S_1} P_1(r, r^{(1)}) \phi(r^{(1)}) \, ds^{(1)} \, ds$$

$$= \oint_{G_1} F(r) g \oint_{S_1} P_1(r, r^{(1)}) \phi(r^{(1)}) \omega(r, r^{(1)}) \, ds^{(1)} \, ds$$

weight value, estimate of $C_{11}, C_{12}, C_{13}$ coefficients
**Background**

- Key techniques for the FRW capacitance solver
  - Pre-calculation of transition probability and weight value
    - Transition probabilities \( \{p_i\} \)
      \[
      \phi(C) = \sum_{i=1}^{6n^2} p_i \phi(S_i)
      \]
    - GFTs and WVTs for transition cubes with various dielectric configurations are pre-calculated and stored as data files
  - Space management for structures with a large number of conductors
  - Important sampling to accelerate convergence
  - Handling cylindrical ITV in 3-D ICs, non-Manhattan and floating metals
  - Parallel implementations on GPU, FPGA and computer cluster

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[Zhang, TCAD 13] [Yu, TCAD 13] [Zhang, IJNM 16] [Zhang, TCAD 15] [Xu, TCAD 17] [Yu, TCAD 18] [Zhai, DATE’13] [Wei, DATE’19] [Song, GLSVLSI’18]
Outline

◆ Background
◆ **Recent Advancements on Parasitic Extraction**
  - Enhancements to the FRW based capacitance solver
  - Machine-learning based parasitic extraction/electrostatic analysis
  - Other related work
◆ Challenges for Advanced Process Technologies
◆ Conclusions
Recent Advancements on Parasitic Extraction

- Enhancements to the FRW capacitance solver
  - Improved technique handling non-stratified dielectrics, based on an approach using eight-octant transition cubes + equivalent permittivity
  - A difficulty occurs for solving structure with a large quantity of non-stratified dielectrics
  - Need to calculate volume weighted average permittivities for the transition cube involving non-stratified dielectric
  - We extend the space management structure for conductors through adding a “dielectric” candidate list to each spatial cell
  - With this we avoid traversing all non-stratified dielectrics to check if/how they intersect the transition cube, and therefore save a lot of time
Enhancements to the FRW capacitance solver

- Improved technique handling non-stratified dielectrics
- Test cases: 1) 11x157x2 array of air bubbles,
  2) 11x209x3 array of air bubbles,
  3) 774911 conformal dielectrics

<table>
<thead>
<tr>
<th>Case</th>
<th>Algorithm</th>
<th>Memory (MB)</th>
<th>Cap. (aF)</th>
<th>$T_{sp}$ (s)</th>
<th>$T_{fr,w}$ (s)</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>brute force</td>
<td>52.7</td>
<td>88.44</td>
<td>0.02</td>
<td>89.96</td>
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<td></td>
<td>proposed</td>
<td>52.7</td>
<td>88.44</td>
<td>0.02</td>
<td>4.94</td>
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<td>2</td>
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<td>89.05</td>
<td>0.03</td>
<td>176.3</td>
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<tr>
<td></td>
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<td>54.5</td>
<td>89.05</td>
<td>0.03</td>
<td>8.26</td>
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<tr>
<td>3</td>
<td>brute force</td>
<td>1140</td>
<td>761.6</td>
<td>29.9</td>
<td>5478</td>
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<tr>
<td></td>
<td>proposed</td>
<td>1200</td>
<td>761.6</td>
<td>114</td>
<td>3.78</td>
</tr>
</tbody>
</table>

Large acceleration!
Recent Advancements on Parasitic Extraction

- Enhancements to the FRW capacitance solver

  - Improved technique handling large net (Gaussian surface generation)
  - Large net includes thousands of wire segments, like power grid
  - Difficulty occurs for generating Gaussian surface
  - VGSS technique avoids this, but determining the placement of BGS needs the nearest environment conductor and its distance
  - To speed up this distance calculation, we propose to use a grid-based spatial structure
  - The runtime overhead for construction is negligible
  - A case with 1.5M conductor blocks (6450 in master net), $341s \rightarrow 0.93s$
Recent Advancements on Parasitic Extraction

- Enhancements to the FRW capacitance solver
  - Reduction of pre-characterization data
  - Transition probability is the probability that a random walk starting at cube’s center reaches corresponding surface panel
  - The symmetry of transition cube with multilayer dielectrics infers GFT value’s symmetry $P(C, A_l) = P(C, A_r) = P(C, A_b)$
  - The quantities in WVT: $w^{(z)}(A_l) = w^{(z)}(A_r) = w^{(z)}(A_b)$, $\begin{cases} w^{(x)}(A_l) = -w^{(x)}(A_r) \\ w^{(y)}(A_l) = w^{(y)}(A_r) \\ w^{(x)}(A_r) = w^{(y)}(A_b) \\ w^{(y)}(A_r) = -w^{(x)}(A_b) \end{cases}$
  - Only need store GFT/WVT values for the surface panels in blue-shade region
  - Reduce memory cost by 8X, and also initialization time
Recent Advancements on Parasitic Extraction

- Machine-learning based parasitic extraction/electrostatic analysis
  - For building the capacitance models in pattern matching method, the neural network (NN) is certainly a potential solution
  - A NN based approach is used to estimate the total capacitance for three 3-D interconnect structures in homogeneous dielectric[8] (RMSE is 1.7% to 4.5%)
  - An automatic approach for pattern classification & capacitance formulas building proposed for pattern matching method [10]
  - Considers 2-D cross-section, clusters patterns sharing same formula. NN is used to do pattern matching and ensure accuracy
  - Experiment on synthesized 3-layer structures validate good accuracy

Recent Advancements on Parasitic Extraction

- Machine-learning based parasitic extraction/electrostatic analysis
  - **MLParest [16]:** predict net’s $R_{\text{eff}}$ and $C_{\text{eff}}$ for pre-layout design of analog IP
    - Synthesize a post-layout net with simple star topology
    - Random forest model for regression, with input features of net properties
    - Experiments on 400K nets on 14nm/10nm processes show the reduction of 37% to 8% averagely on the error of pre-layout simulation

Recent Advancements on Parasitic Extraction

- Machine-learning based parasitic extraction/electrostatic analysis
  - **ParaGraph [14]:** predict net’s total capacitance and device parameters
    - Schematic of analog / mixed-signal circuit is viewed as a heterogeneous graph
    - Incorporates key ideas from GraphSage, Relational GCN and Graph Attention Network
    - Ensemble learning technique is presented to improve the accuracy of capacitance over a large range
    - Errors of pre-layout prediction on 67 circuit metrics

<table>
<thead>
<tr>
<th>Error Range</th>
<th>Layout w/o Parasitics</th>
<th>Designer’s Estimation</th>
<th>Prediction w/ XGB</th>
<th>Prediction w/ ParaGraph</th>
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</thead>
<tbody>
<tr>
<td>&lt; 10%</td>
<td>4</td>
<td>6</td>
<td>17</td>
<td>44</td>
</tr>
<tr>
<td>10%-20%</td>
<td>0</td>
<td>17</td>
<td>14</td>
<td>10</td>
</tr>
<tr>
<td>20%-30%</td>
<td>5</td>
<td>18</td>
<td>4</td>
<td>8</td>
</tr>
<tr>
<td>30%-40%</td>
<td>35</td>
<td>2</td>
<td>7</td>
<td>4</td>
</tr>
<tr>
<td>40%-50%</td>
<td>14</td>
<td>6</td>
<td>9</td>
<td>1</td>
</tr>
<tr>
<td>&gt; 50%</td>
<td>9</td>
<td>18</td>
<td>16</td>
<td>0</td>
</tr>
<tr>
<td>Mean</td>
<td>37.75%</td>
<td>&gt;100%</td>
<td>32.14%</td>
<td>9.60%</td>
</tr>
<tr>
<td>Geometric Mean</td>
<td>29.01%</td>
<td>43.57%</td>
<td>15.46%</td>
<td>4.00%</td>
</tr>
</tbody>
</table>

Recent Advancements on Parasitic Extraction

- **Machine-learning based parasitic extraction/electrostatic analysis**
  - **Attempts applying machine learning to electrostatic field solver**
    - In [28], a single-layer NN was proposed to interpret MoM for capacitance extraction
    - The solving process is regarded as machine learning training process
    - Its application is **limited** due to the intrinsic drawback of MoM
    - In [23], CNN was presented to simulate the field in 2-D square with a point excitation
    - Model the input as image-like data, but the problem is **too simplified and is unpractical**
    - In [13], CNN was proposed for solving the electrostatics within VLSI layout for TDDB aging analysis
    - Image transformation to convert 2-D layout to the map of electric potential
  - **DL has limited application to capacitance solver or scientific computation**

Recent Advancements on Parasitic Extraction

- Other related work
  - In [11], the combination of FRW based capacitance extraction and the generalized polynomial chaos (gPC) expansion is considered.
  - An LS based approach was proposed to accurately deduce the detailed variational capacitance distribution due to wire width and spacing variability.
  - In [20], a technique was proposed to tighten the parasitic corner range of customized design pattern through Monte Carlo simulation.
  - In [27], a FDM based macromodel generation technique was proposed to ensure macromodel matrix’s properties, improving the reliability of macromodel-aware RW algorithm.

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Challenges for Advanced Process Technologies

- Manufacture-aware geometry variation
  - Layout/geometry variations caused by manufacture process (with commands in technology file)
  - Bring challenges to both pattern matching based method and capacitance field solver
  - For multiple-patterning lithography, misalignment of different colored layouts also affects capacitance extraction

Tradeoff between accurate geometric computation (accuracy) and the efficiency of capacitance extraction
Challenges for Advanced Process Technologies

- Random process variation
  - Has larger impact at advanced technology nodes
  -Better random variation modeling and accelerated variation-aware extraction technique for actual scenarios are important topics

- Accurate MEOL capacitance modeling
  - MEOL capacitances around FinFET
  - More complex device structures emerging
  - Even with 3-D patterns, the error often exceeds 10% with pattern matching based method
  - More efficient field solver techniques are needed
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Conclusions

- Parasitic extraction becomes even more important for ensuring design quality of ICs under advanced process technology.
- Floating random work method is a promising technique for accurate capacitance extraction. More effort should be paid to improve its efficiency for handling complex structures.
- Machine learning techniques should be leveraged to enhance the pattern matching method or for early-stage parasitic estimation.
- Geometric variations under advanced process technology bring a lot of engineering labor and the challenge of computational cost to parasitic extraction.
Thank You!

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