

Aims of the Conference:

ASP-DAC 2021 is the 26th annual international conference on VLSI design automation in Asia and South Pacific regions, one of the most active regions of design and fabrication of silicon chips in the world. The conference aims at providing the Asian and South Pacific CAD/DA and Design community with opportunities of presenting recent advances and with forums for future directions in technologies related to Electronic Design Automation (EDA). The format of the meeting intends to cultivate and promote an instructive and productive interchange of ideas among EDA researchers/developers and system/circuit/device designers. All scientists, engineers, and students who are interested in theoretical and practical aspects of VLSI design and design automation are welcomed to ASP-DAC.

Areas of Interest:

Original papers in, but not limited to, the following areas are invited.

[1] System-Level Modeling and Design Methodology:

- 1.1. HW/SW co-design, co-simulation and co-verification
- 1.2. System-level design exploration, synthesis, and optimization
- 1.3. System-level formal verification
- 1.4. System-level modeling, simulation and validation tools/methodology

[2] Embedded Systems and Cyberphysical Systems:

- 2.1. Many- and multi-core SoC architecture
- 2.2. IP/platform-based SoC design
- 2.3. Domain-specific architecture
- 2.4. Dependable architecture
- 2.5. Cyber physical system
- 2.6. Internet of things

[3] Embedded Systems Software:

- 3.1. Kernel, middleware, and virtual machine
- 3.2. Compiler and toolchain
- 3.3. Real-time system
- 3.4. Resource allocation for heterogeneous computing platform
- 3.5. Storage software and application
- 3.6. Human-computer interface

[4] Memory Architecture and Near/In Memory Computing:

- 4.1. Storage system and memory architecture
- 4.2. On-chip memory architectures and management: Scratchpads, compiler, controlled memories, etc.
- 4.3. Memory and storage hierarchies with emerging memory technologies
- 4.4. Near-memory and in-memory computing
- 4.5. Memory architecture and management for emerging memory technologies

[5] AI/Machine Learning System Designs:

- 5.1. Hardware and devices for neuromorphic and neural network computing
- 5.2. Design method for learning on a chip
- 5.3. Systems for neural computing (including deep neural networks)
- 5.4. Neural network acceleration co-design techniques
- 5.5. Design techniques for AI of Things

[6] Analog/Mixed-Signal Design, Simulation and Validation:

- 6.1. Analog/mixed-signal/RF synthesis
- 6.2. Analog layout, verification, and simulation techniques
- 6.3. High-frequency electromagnetic simulation of circuit
- 6.4. Mixed-signal design consideration
- 6.5. Communication architectures using nanophotonics, RF, 3D, etc.
- 6.6. Networks-on-chip and NoC-based system design

[7] Approximate, Stochastic and Neuromorphic Computing:

- 7.1. Circuit and system techniques for approximate computing
- 7.2. Stochastic computing for AI/ML
- 7.3. CAD for approximate and stochastic systems
- 7.4. Neuromorphic computing for AI/ML
- 7.5. CAD for bio-inspired and neuromorphic systems

[8] Logic/High-Level Synthesis and Optimization:

- 8.1. High-level synthesis tool and methodology

- 8.2. Combinational, sequential and asynchronous logic synthesis
- 8.3. Logic synthesis and physical design technique for FPGA
- 8.4. Technology mapping

[9] Physical Design:

- 9.1. Floorplanning, partitioning and placement
- 9.2. Interconnect planning and synthesis
- 9.3. Placement and routing optimization
- 9.4. Clock network synthesis
- 9.5. Post layout and post-silicon optimization
- 9.6. Package/PCB/3D-IC routing

[10] Design for Manufacturability and Reliability:

- 10.1. Reticule enhancement, lithography-related design and optimization
- 10.2. Resilience under manufacturing variation
- 10.3. Design for manufacturability, yield, and defect tolerance
- 10.4. Reliability, aging and soft error analysis
- 10.5. Design for reliability, aging, and robustness
- 10.6. Machine learning for smart manufacturing and process control

[11] Design and Analysis for Timing and Low Power:

- 11.1. Power modeling, analysis and simulation
- 11.2. Low-power design and optimization at circuit and system levels
- 11.3. Thermal aware design and dynamic thermal management
- 11.4. Energy harvesting and battery management
- 11.5. Deterministic/statistical timing analysis and optimization
- 11.6. 2D/3D on-chip power/ground and package modeling, analysis and optimization
- 11.7. Signal/power integrity, EM modeling and analysis
- 11.8. Extraction, TSV and package modeling

[12] Testing, Validation, Simulation, and Verification:

- 12.1. ATPG, BIST and DFT
- 12.2. System test and 3D IC test
- 12.3. Online test and fault tolerance
- 12.4. Memory test and repair
- 12.5. RTL and gate-leveling modeling, simulation, and verification
- 12.6. Circuit-level formal verification
- 12.7. Device/circuit-level simulation tool and methodology

[13] Hardware and Embedded Security:

- 13.1. Hardware-based security
- 13.2. Detection and prevention of hardware Trojans
- 13.3. Side-channel attacks, fault attacks and countermeasures
- 13.4. Design and CAD for security
- 13.5. Cyberphysical system security
- 13.6. Nanoelectronic security
- 13.7. Supply chain security and anti-counterfeiting

[14] Emerging Technologies and Applications:

- 14.1. Biomedical, biochip, and biodata processing.
- 14.2. Big/thick data, datacenter
- 14.3. Advanced multimedia application
- 14.4. Energy-storage/smart-grid/smart-building design and optimization
- 14.5. Automotive system design and optimization
- 14.6. New transistor/device and process technology: spintronic, phase-change, single-electron etc.
- 14.7. Nanotechnology, MEMS, quantum computing etc.

Please note that each paper shall be accompanied by at least one different conference registration at the speaker's registration rate (e.g., two speaker registrations are needed for presenting two accepted papers). But any registered co-author can present the work at the conference. ACM and IEEE reserve the right to exclude a paper from distribution after the conference (e.g., removal from ACM Digital Library and IEEE Xplore) if the paper is not presented at the conference by the author of the paper. ASP-DAC does not allow double and/or parallel submissions of similar work to any other conferences, symposia, and journals.

Submission of Papers:

Deadline for submission: **5 PM AOE (Anywhere on earth) Jul. 26 (Sun), 2020**
 Notification of acceptance: **Sep. 13 (Sun), 2020**
 Deadline for final version: **5 PM AOE (Anywhere on earth) Nov. 6 (Fri), 2020**

For detailed instructions for submission, please refer to the "Authors' Guide" at: <http://www.aspdac.com/>

ASP-DAC 2021 Chairs

General Co-Chairs:

Technical Program Chair:

Technical Program Vice Chairs:

Toshihiro Hattori (Renesas Electronic Corporation)

Sheldon Tan (University of California, Riverside)

Masanori Hashimoto (Osaka University)

Panels, Special Sessions, and Tutorials: Suggestions and proposals are welcome and have to be addressed to the Conference Secretariat (aspdac2021@aspdac.com) no later than August 2 (Sunday), 2020.

Contact: Conference Secretariat: aspdac2021@aspdac.com TPC Secretariat: tpc@aspdac21.com

Call for Designs

University LSI Design Contest

ASP-DAC 2021

<http://www.aspdac.com/>

January 18-21, 2021

Tokyo, Japan



Aims of the Contest:

As a unique feature of ASP-DAC 2021, the University LSI Design Contest will be held. The aim of the Contest is to encourage education and research on VLSI design at universities and other educational organizations. We solicit designs that fit in one or more of the following categories:

- (1) Designed, and actually implemented on chips in universities or other educational organizations during the last two years;
- (2) Designs that report actual measurements from implementations;
- (3) Innovative design prototypes.

Interesting or excellent designs selected will be honored by providing the opportunities for presentation in a special session at the conference. Award(s) will be given to a few numbers of outstanding designs, selected from those presented at the conference.

Areas of Design:

Application areas or types of circuits of the original LSI circuit designs include (but are not limited to):

- (1) Analog, RF and Mixed-Signal Circuits, (2) Digital Signal Processing, (3) Microprocessors, (4) Custom ASIC.

Methods or technology used for implementation include:

- (a) Custom ASIC and Cell-Based LSIs, (b) Gate Arrays, (c) FPGA/PLDs.

Submission of Design Descriptions:

A camera-ready summary is requested to be prepared within 2 pages including figures, tables, and references. It is strongly recommended that measured experimental results and a chip micrograph are included in the summary. Please do not submit the same paper as a regular paper.

Specification of the submission format will be available at <http://www.aspdac.com/>

Deadline for summary:	5 PM AOE (Anywhere on earth)	July 26 (Sun), 2020
Notification of acceptance:		Sep. 13 (Sun), 2020
Deadline for camera-ready:	5 PM AOE (Anywhere on earth)	Nov. 6 (Fri), 2020

Review:

Submitted designs will be reviewed by the Design Contest Committee in a process similar to the review process for the technical papers. The following criteria will be applied in the selection of designs:

- (1) Reliability of design and implementation, (2) Quality of implementation, (3) Performance of the design, (4) Novelty of application, algorithm, architecture, (5) Others.

Interesting or excellent designs selected will be presented at a special session of the conference.

Presentation:

An author of each selected design will be required to make a short presentation at a special session of ASP-DAC 2021. A digest of each design to be presented will be included in the conference proceedings.

Contact Email: aspdac2021-udc@aspdac.com

ASP-DAC 2021 Chairs

General Chair:	Toshihiro Hattori (Renesas Electronics Corp., Japan)
Technical Program Chair:	Sheldon Tan (University of California, Riverside, USA)
Technical Program Vice Chair:	Masanori Hashimoto (Osaka University, Japan)
Design Contest Co-Chairs:	Kousuke Miyaji (Shinshu University, Japan) Akira Tsuchiya (The University of Shiga Prefecture, Japan)

Prospective Sponsors: ACM SIGDA, IEEE CASS, IEEE CEDA, IEICE ESS, IPSJ SIGSLDM