Generation of Shorter Sequences for High Resolution Error Diagnosis Using Sequential SAT

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Outline

- Motivation
- Problem formulation
- Methodology
- Experimental results
- Conclusion

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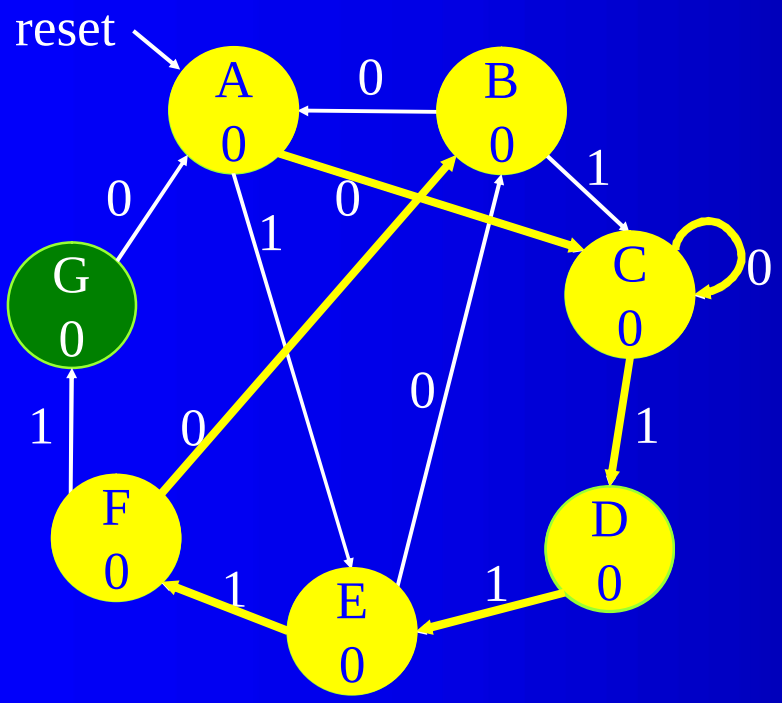
Motivation

- Simulation dominates the source of error traces
  - Length of an error trace tends to be long
  - Long error traces increase diagnosis complexity
- Diagnosis depends on error traces
  - Error traces may contain unnecessary information

Unnecessary State Information

- Unnecessary states in an error trace
  - Visiting a state multiple times
  - Visiting unnecessary states to activate/propagate errors



- Error Sequence: 001110
  - Visited States: A-C-C-D-E-F-B
- Faulty Transition: F-B

Unnecessary State Information

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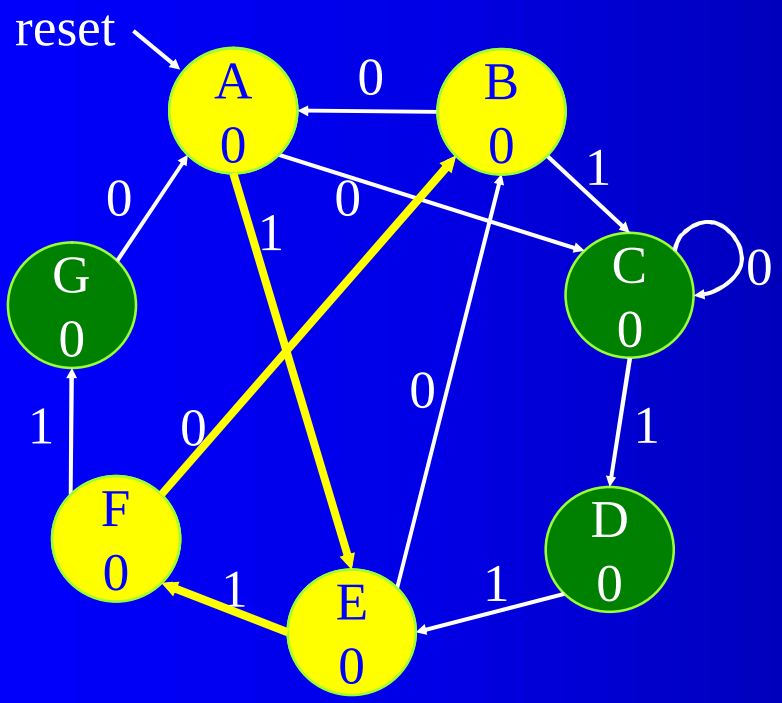

- Error Sequence: 001110
  - Visited States: A-C-C-D-E-F-B
- Faulty Transition: F-B
- Shorter Error Sequence: 110
  - Visited States: A-E-F-B

Objective

- Generate a shorter error sequence from an existing error trace

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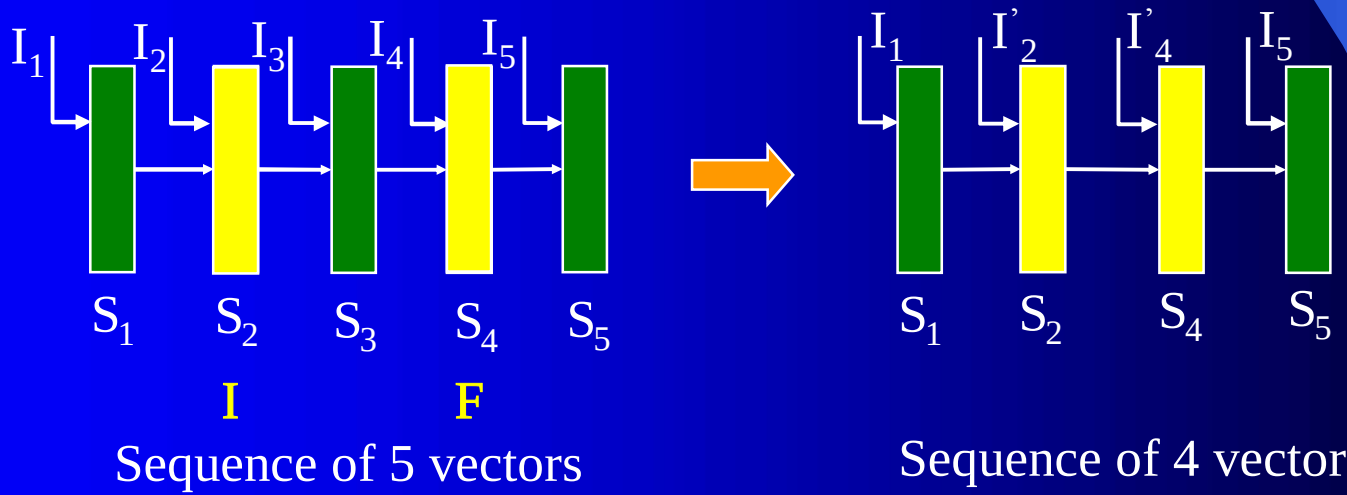
Problem Formulation

- States visited by error sequence are known from simulation
  - Select any pair of states as initial state I and final state F.
  - Apply SAT solver to find the shorter transfer function.

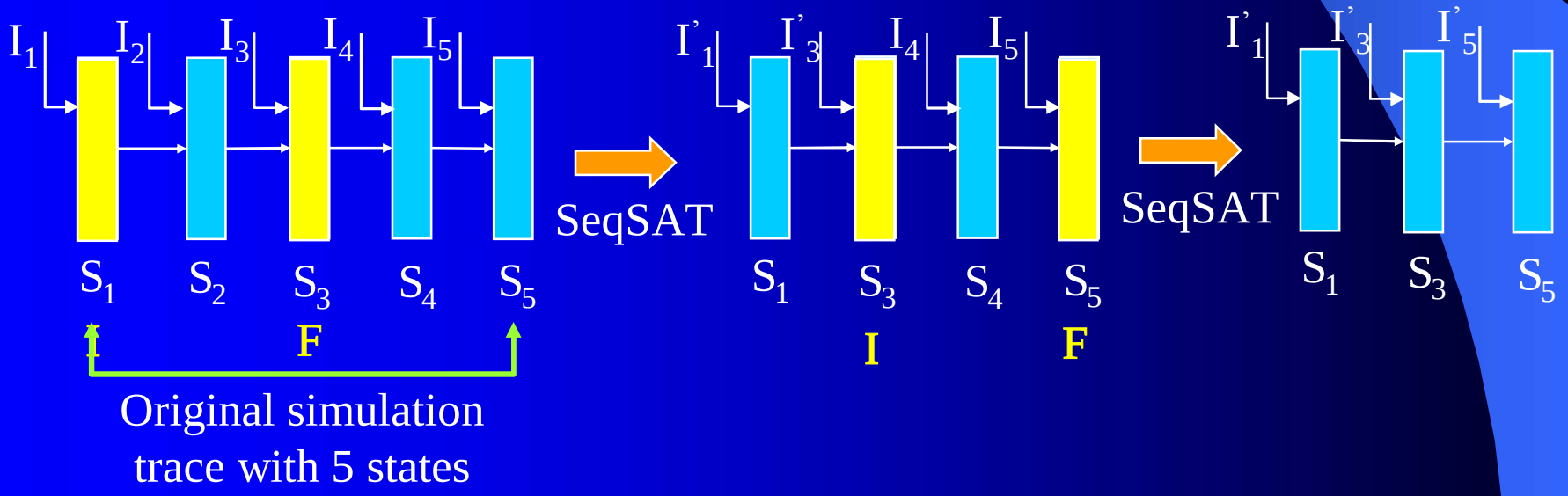


Sequential SAT Solver

- Input Data of a sequential SAT solver:
  - Initial State & Target State
  - One time-frame combinational copy of the sequential circuit
- Improvements on sequential SAT solver offers better sequential search than BMC
  - State reduction
  - Flexible sequential search framework
- F. Lu, et. al., “An Efficient Sequential SAT Solver With Improved Search Strategies”, DATE’05

Problem Formulation (Cont'd)

- Intuitive solution: generate a new sequence with the first state (S_1) as I and the last state (S_5) as F.
- Cannot find a solution within reasonable runtime
- Transform into multiple smaller problems.

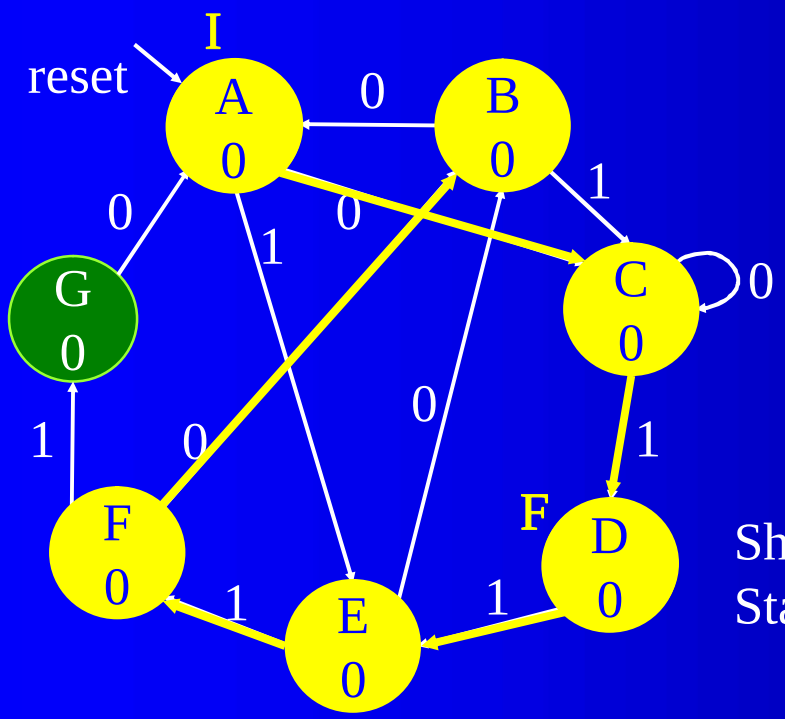


Previous Work

- Find the shortest path from transition graphs of pairs of states
- Correct state information is available
- References:
  - K. Chang, V. Bertacco, & I. Markov, ICCAD'05
  - Y.-A. Chen & F.-S. Chen, ASPDAC'03
  - A. L. D'Souza & M. Hsiao, VLSI Design'01

Target State Selection

- Different target selection affects the reduction ratio.



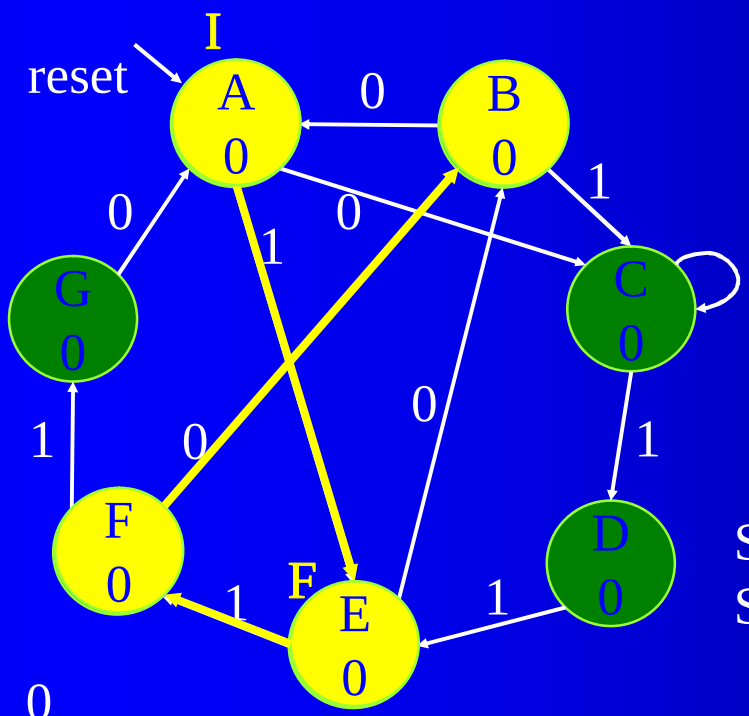
State Transition Graph

Error sequence: 001110
States: A-C-C-D-E-F-B

Shorter sequence: 01110
States: A-C-D-E-F-B

Target State Selection

- Different target selection affects the reduction ratio.



State Transition Graph

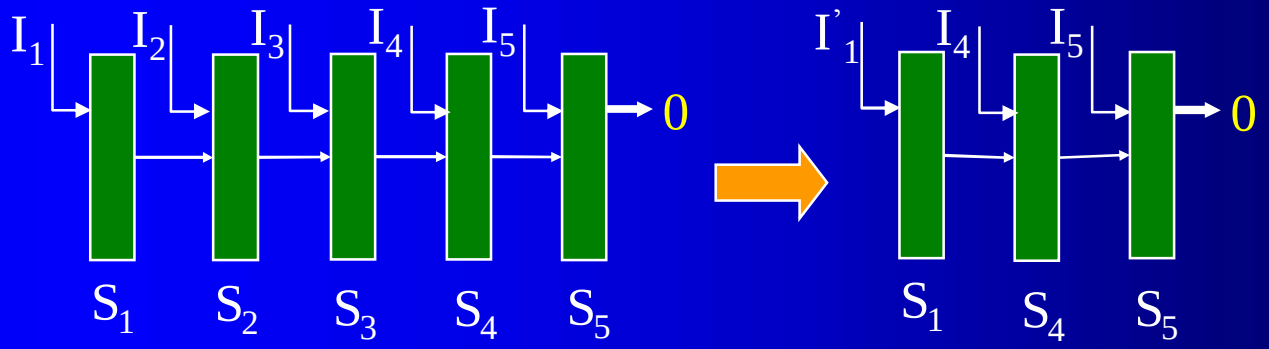
Error sequence: 001110
States: A-C-C-D-E-F-B

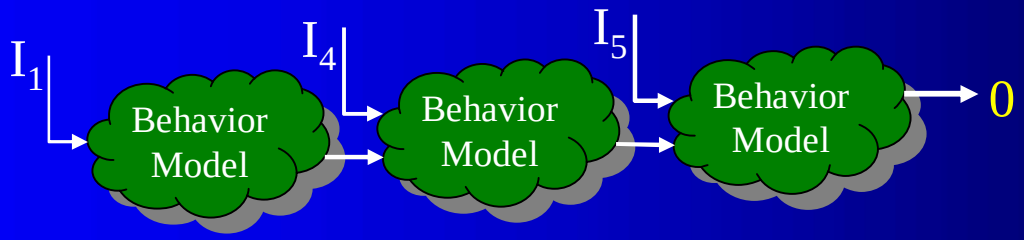
Shorter sequence: 01110
States: A-C-D-E-F-B

Shorter sequence: 110
States: A-E-F-B

Validation of Test Sequence

- SAT generate a new sequence from an erroneous circuit
- Expected output responses may be changed
- Verify the new sequence





Same expected responses to $\{I'_1, I_4, I_5\}$

Discard the sequence

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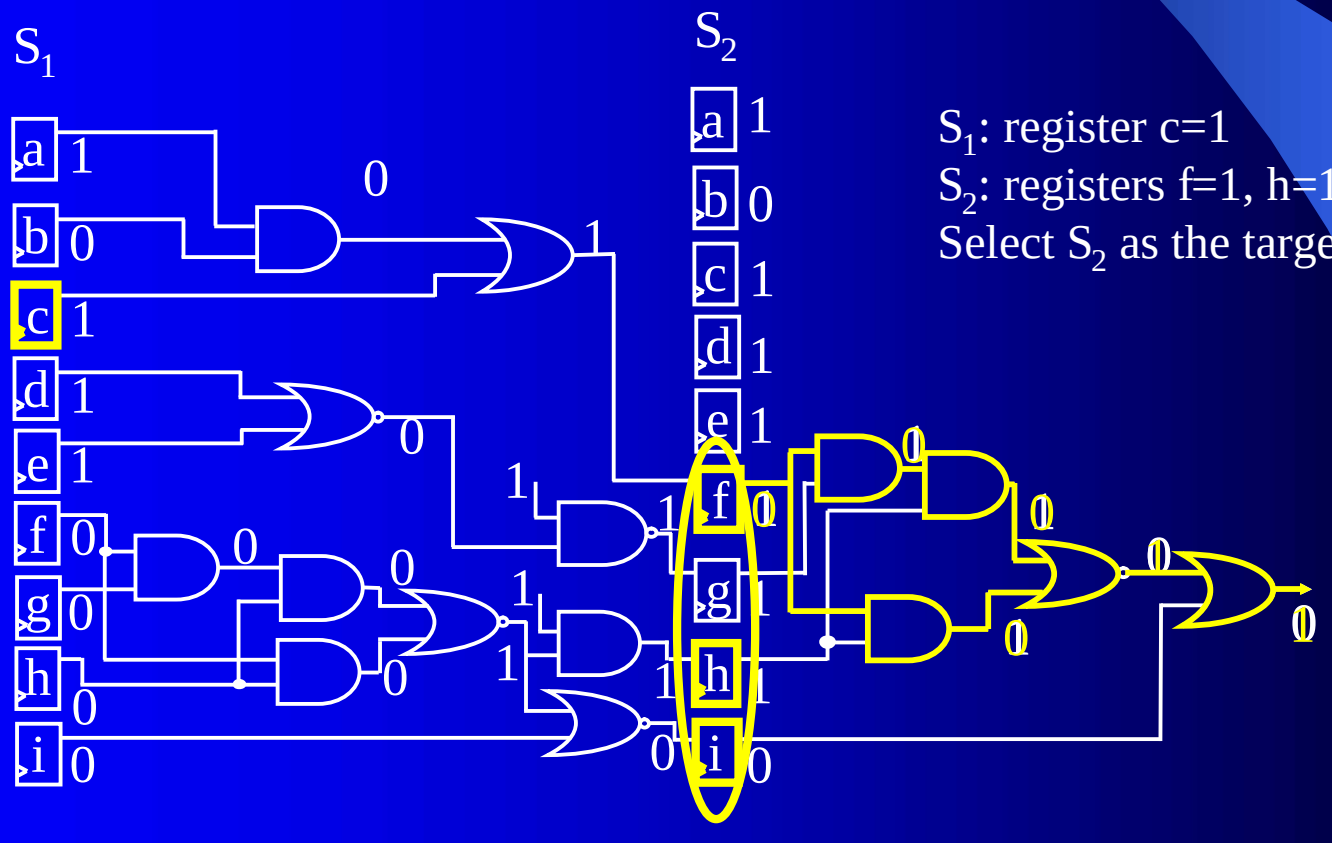
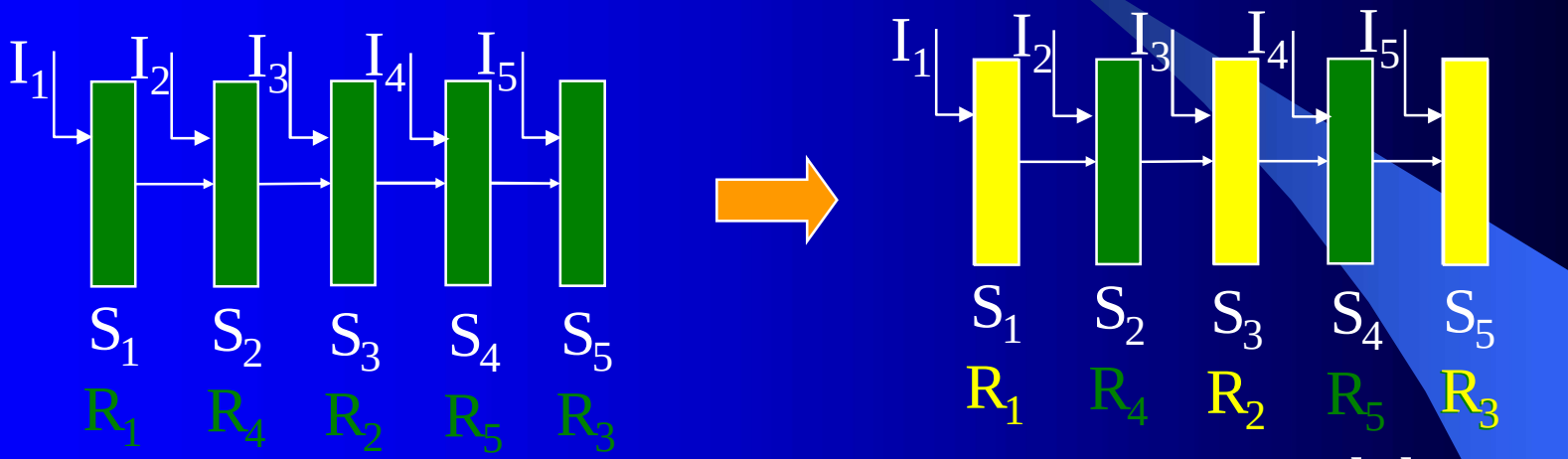
Target Selection

- Infeasible to exhaust transfer functions.
- Rank state based on the number of registers on error propagation path
  - Check whether a register affects outputs by inverting the value.



Target Selection (Cont'd)

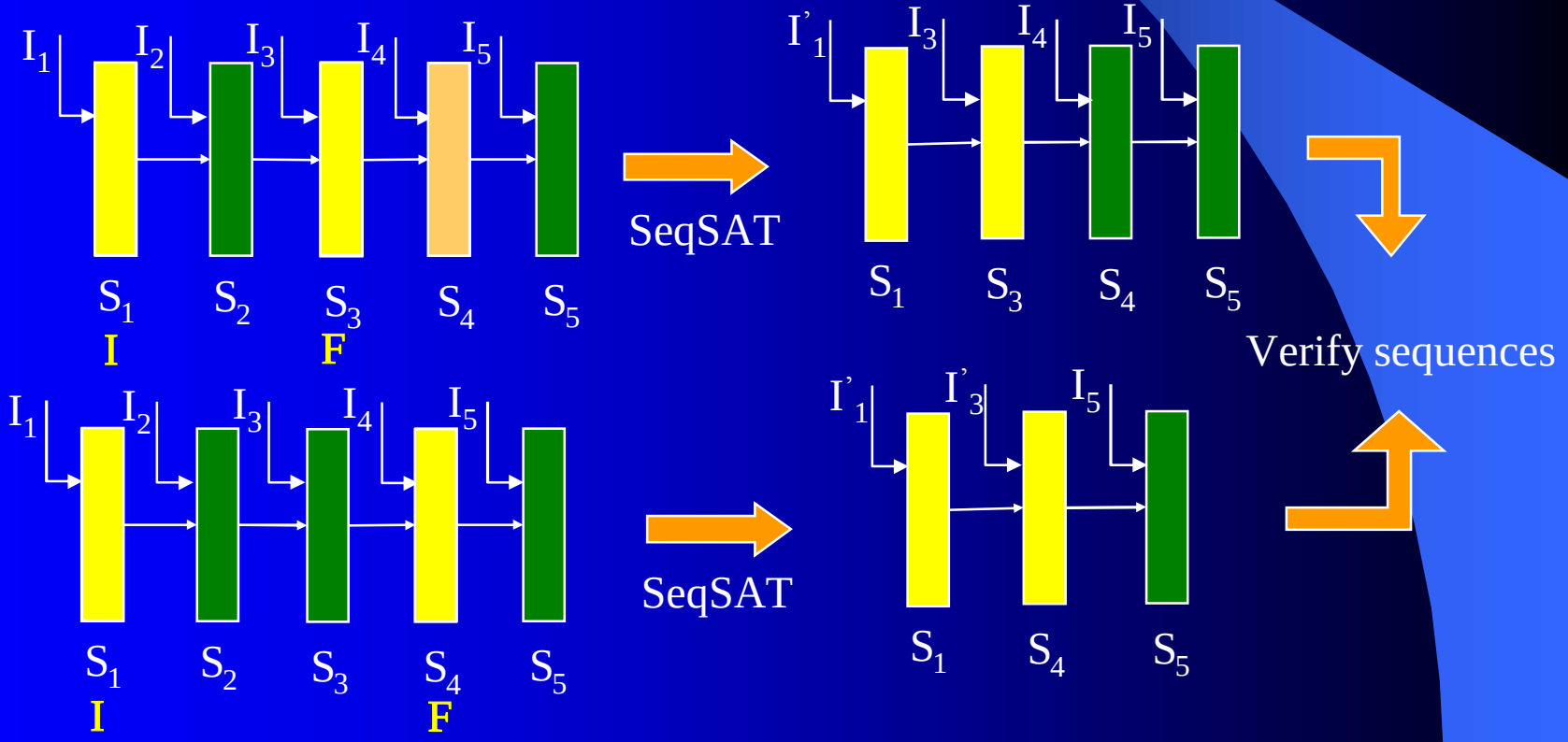
- Select states as target state candidates based on the ranking order



Target state candidates: S_1, S_3, & S_5.

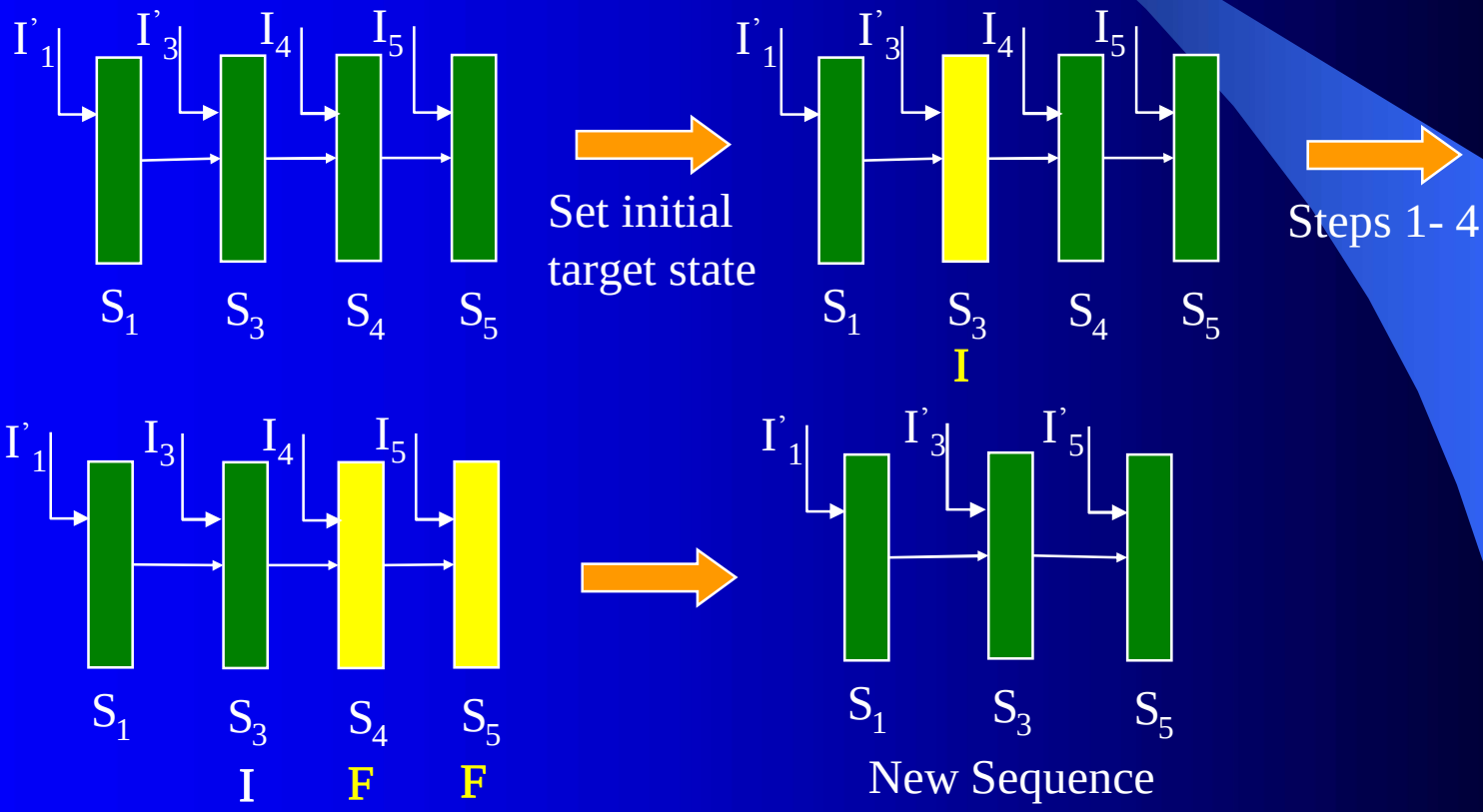
Methodology

1. Determine target state candidates
2. Apply SAT solver to find new transfer functions
3. Combine new sequences with the original sequence.
4. Verify new sequences.



Methodology

5. Select the shortest and valid sequence.
6. Reset the initial target state
7. Repeat steps 1 - 4



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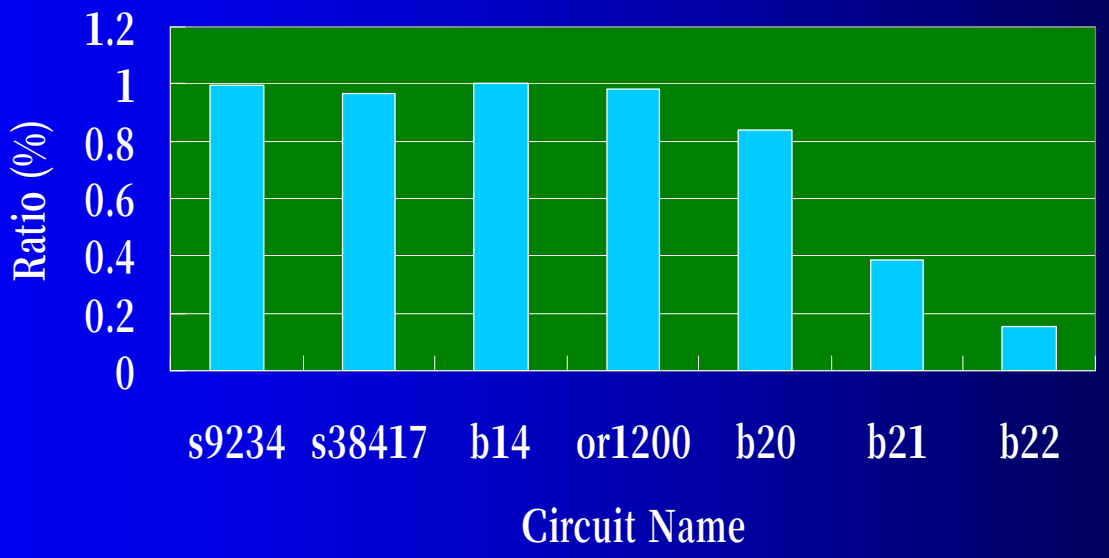
Experimental Results

- Replace gates with different types of gates.
  - ITC99, ISCAS89, & or1200
- Generate sequences randomly for simulation
- Identify error sequences by comparing output responses



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Conclusion

- Error sequence contains unnecessary information.
- Methodology of generating a shorter sequence
  - Applying SAT solver to multiple smaller problems.
  - Heuristic of target state selection.
- Achieve high reduction ratio in experiments.

Q & A