Robust Analytical Gate Delay Modeling for Low Voltage Circuits

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Outline

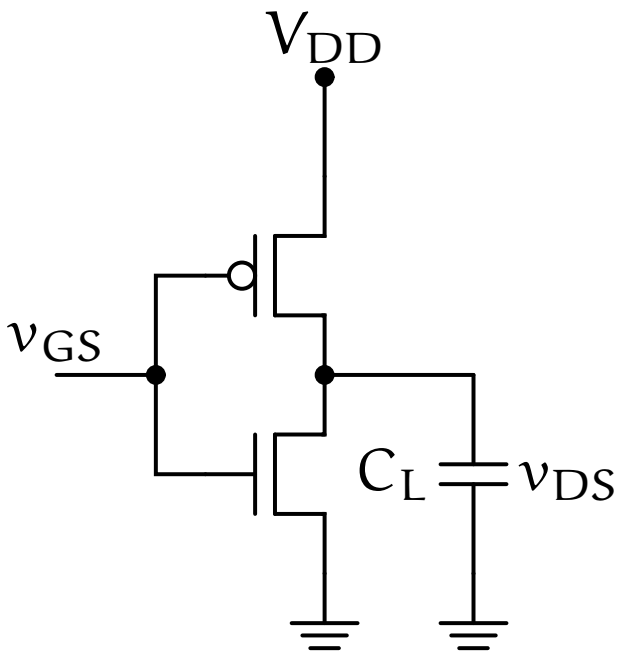
Delay Modeling

- One of the most fundamental EDA problems
- Two components of delay modeling
  - Gate delay
  - Interconnect delay
- Different levels of accuracy and abstraction
  - Analytical formula: simple and intuitive to guide optimization
  - Table look-up based
  - Simulation-based, e.g., SPICE
- This work is on gate delay modeling

Gate Delay Modeling

- Table-look up
- Closed-form formula: Sakurai-Newton (SN) model [1990]
  - Widely used due to its simplicity and reasonable accuracy
  - However, it does not work well at low voltages [Taur and Ning, 1998]
- Contribution of this work
  - We provide a new Elmore-perspective of the SN model, which is the centroid of the current
  - We propose a new closed-form gate delay model based on the centroid of the power dissipated by the gate
  - This new model is robust (across wide ranges) with very high fidelity

Background of Gate Delay



- Gate delay can be approximated as

$$\Delta t = \frac{\Delta Q}{I_D}$$

where

- ΔQ: change in charge at load capacitor C_L
- I_D: drain current

- The 50% gate delay is

$$t_{delay} = \frac{C_L \left(\frac{V_{DD}}{2}\right)}{I_D}$$

Sakurai-Newton (SN) Gate Delay Formula

- SN current equation (saturation-mode) $I_D = \frac{k}{2}(v_{GS} - V_T)^{\alpha}$
  - α is velocity saturation index, $\alpha \approx 1$ for nm regimes
- Assume a step input, $v_{GS} = V_{DD}\, u(t)$
- SN assumes that the transistor is in saturation region till $\frac{V_{DD}}{2}$

$$t_{delay} = \frac{C_L \frac{V_{DD}}{2}}{I_D} \approx \frac{C_L \frac{V_{DD}}{2}}{\frac{k}{2}(V_{DD} - V_T)^{\alpha}}$$

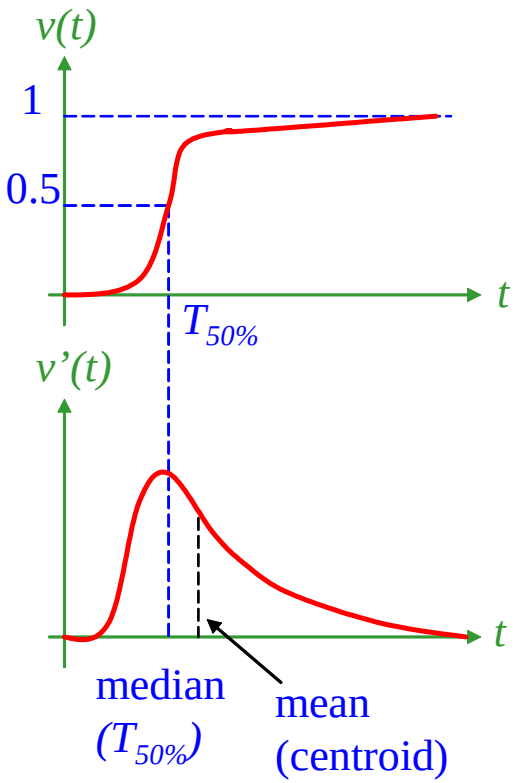
- But discharge under step input has two regions
  - Saturation: $V_{DD} \geqslant v_{DS} > V_{DD} - V_T$
  - Linear: $V_{DD} - V_T \geqslant v_{DS} \geqslant 0$
- Thus SN delay formula is obtained through approximation
- We show that it is in fact Elmore delay of gate

Elmore delay

Definition

Elmore delay is defined as the centroid of the impulse response $h(t)$

- The centroid of a function $f(x)$ is defined as $C[f(x)] = \frac{\int_x x f(x)\, dx}{\int_x f(x)\, dx}$

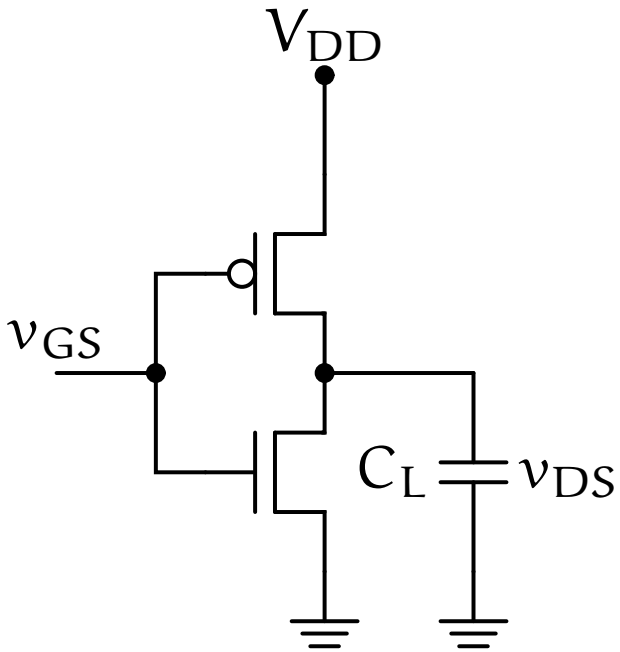


- Since $\int_0^\infty h(t)dt = 1$ for monotonic RC circuit

$$t_{elmore} = \int_0^\infty t\, h(t)dt$$

- Note that Elmore delay is Mean of impulse reponse
  - Real dealy is given by Median
  - Mean is an upperbound of Median for RC circuits

Impulse response $\propto$ switching current in RC circuit

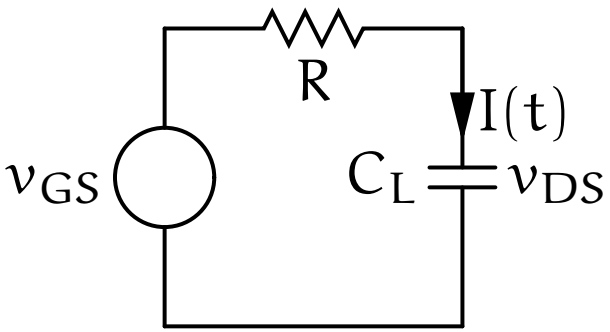


- Model inverter as an RC circuit
  - R: nonlinear resistor
- Laplace transform of $h(t)$ ($H(s)$)

$$H(s) = \frac{V_{DS}(s)}{V_{GS}(s)} = \frac{V_{DS}(s)}{\frac{1}{s}} = sV_{DS}(s)$$

- Translate to time domain

$$h(t) = \frac{dv_{DS}}{dt} = \frac{1}{C_L} I(t) \propto I(t)$$



- Centroid of $I(t)$ instead of $h(t)$

Elmore delay is centroid of switching current

Lemma

The Elmore delay of a CMOS gate under step input is the centroid of the current dissipated by it during switching.

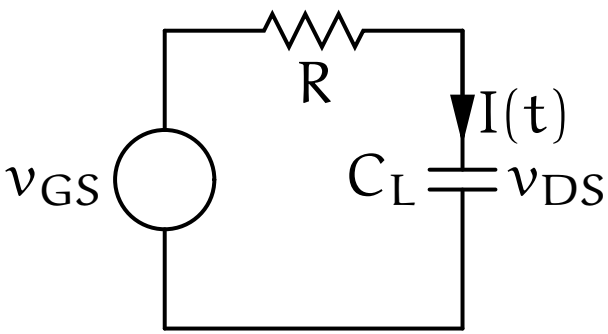
- Thus Elmore delay is

$$t_{elmore} = \frac{\int_0^\infty t\, h(t)dt}{\int_0^\infty h(t)dt} = \frac{\int_0^\infty t\, I(t)dt}{\int_0^\infty I(t)dt}$$
$$= \frac{\int_0^{t_{sat}} t\, i_{D_{SAT}}\, dt + \int_{t_{sat}}^\infty t\, i_{D_{LIN}}\, dt}{\int_0^{t_{sat}} i_{D_{SAT}}\, dt + \int_{t_{sat}}^\infty i_{D_{LIN}}\, dt}$$

- The unknowns in the above equation are
  - t_{sat}: Transition point from saturation to linear
  - $i_{D_{SAT}}/i_{D_{LIN}}$: Current in the saturation/linear region of operation

t_{sat}: Transition point from saturation to linear

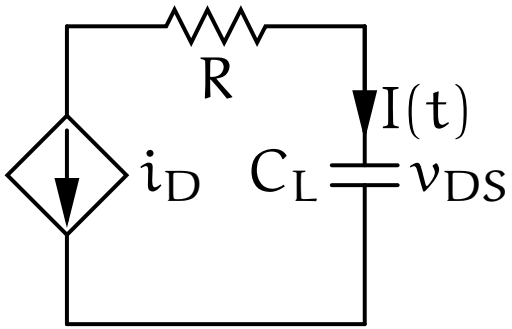
- The transistor under step input switches from saturation to linear when $v_{DS} = V_{DD} - V_T$



- t_{sat}: time taken to change from saturation to linear
- t_{sat} is obtained by applying KCL at C_L

$$t_{sat} = \frac{2C_L V_T}{k(V_{DD} - V_T)^{\alpha}}$$

$i_{D_{SAT}}/i_{D_{LIN}}$: Current in saturation/linear regions

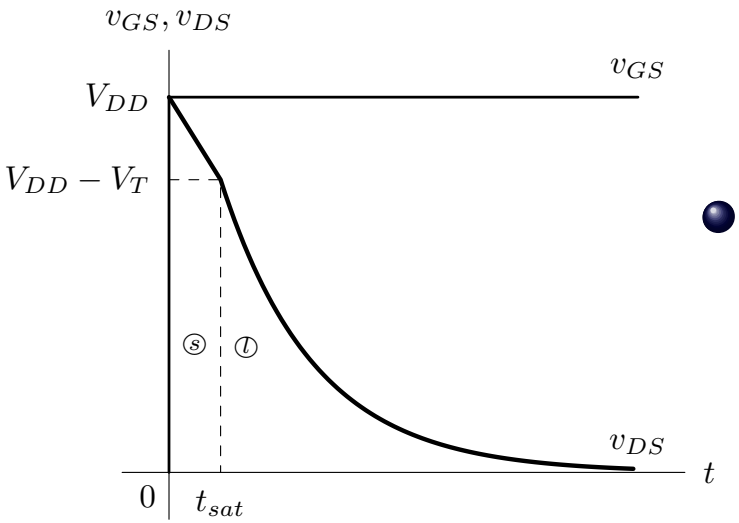


- Constant current in saturation

$$i_{D_{SAT}} = \frac{k}{2}(V_{DD} - V_T)^{\alpha}$$

- Current in linear region is

$$i_{D_{LIN}} = k(V_{DD}-V_T)^{\alpha}\frac{v_{DS}}{V_{DD} - V_T} = \frac{v_{DS}}{R}$$



- v_{DS} is given by

$$v_{DS} = (V_{DD}-V_T)e^{\frac{-(t-t_{sat})}{RC_L}}u(t-t_{sat})$$

SN delay formula is Elmore delay

- Putting t_{sat} and $i_{D_{SAT}}/i_{D_{LIN}}$ back to the Elmore delay (the centroid of $I(t)$), we have

$$\boxed{t_{elmore} = \frac{C_L V_{DD}}{k(V_{DD} - V_T)^{\alpha}}}$$

- It is exactly the same as the Sakurai-Newton formula

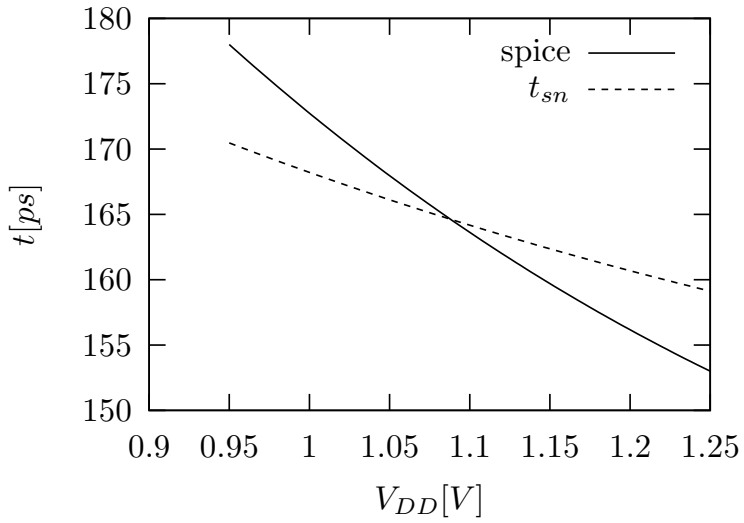
Theorem

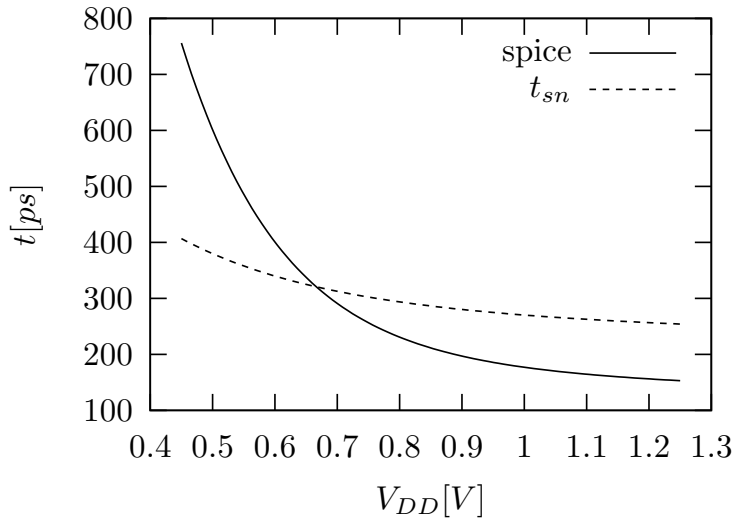
The Sakurai-Newton formula is the Elmore delay of the CMOS gate under the following conditions:

(i) *A step input is applied;*

(ii) *The CMOS gate is modeled as an RC circuit.*

How Well SN Model Works?





- Data of $65nm$ inverter with $C_L = 20fF$ and $V_{T0} = 0.22V$
- Under nominal voltages ($V_{DD} \geqslant 0.9V$), delay varies over small range $[150, 180]ps$
  - Empirically delay $\propto \frac{1}{V_{DD}}$, captured well by SN
- Under low voltages ($V_{DD} < 0.9V$), delay varies over wide range $[200, 800]ps$
  - Need higher order terms to capture this spread which SN lacks

Centroid-of-Power Delay Model

- SN metric fails to track delay under low voltages where delay $\propto \frac{1}{V_{DD}^2}$
- A natural idea is to use centroid of power instead of current to track this quadratic term since power $\propto$ (current)^2
  - This results in Elmore-like closed form expression
- Centroid-of-power delay (t_{cp}) is defined as

$$t_{cp} = \frac{\int_0^\infty t\, v_{DS}\, i_D\, dt}{\int_0^\infty v_{DS}\, i_D\, dt}$$

$$\boxed{t_{cp} = \frac{C_L(3V_{DD}^3 + 3V_{DD}^2 V_T - 3V_{DD}V_T^2 + V_T^3)}{6kV_{DD}^2(V_{DD} - V_T)^\alpha}}$$

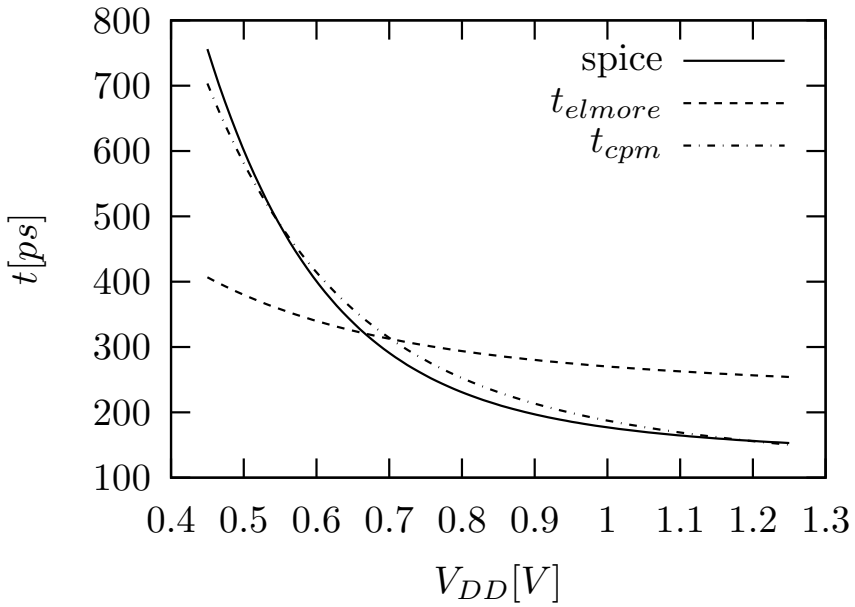
Modified Centroid-of-Power Delay Model

- We empirically found that $\frac{1}{(V_{DD}-V_T)^2}$ tracks delay better than $\frac{1}{V_{DD}^2}$ in the denominator
  - Have not found the rigid theory behind yet
- *Modified* centroid of power based delay metric

$$t_{cpm} \propto \frac{C_L(3V_{DD}^3 + 3V_{DD}^2V_T - 3V_{DD}V_T^2 + V_T^3)}{(V_{DD}-V_T)^2(V_{DD}-V_T)^\alpha}$$

- This modification on t_{cp} leads to near perfect correlation across all voltage ranges
- Possible reasons why it works
  - Gate overdrive is proportional to $(V_{DD}-V_T)$
  - When V_{DD} varies, $\frac{1}{(V_{DD}-V_T)^2}$ has a faster rate of change compared with $\frac{1}{V_{DD}^2}$

Delay models against HSPICE



- Data of $65\mathrm{nm}$ inverter with $C_L = 20\mathrm{fF}$ and $V_{T0} = 0.22V$
- Observe that CPM can track delay across all voltages
  - Higher order terms of CPM help track delay in low voltages

Comparison across Different Technologies and Gates

Gate	45nm			65nm			100nm		
	SN	CP	CPM	SN	CP	CPM	SN	CP	CPM
INV	0.76	0.81	0.99	0.76	0.82	0.99	0.90	0.94	0.98
NAND2	0.72	0.76	0.99	0.73	0.77	0.99	0.83	0.87	1.00
NOR2	0.73	0.78	0.99	0.75	0.80	0.99	0.90	0.93	0.99
XOR2	0.71	0.76	0.99	0.71	0.76	0.98	0.90	0.93	1.00

- Correlation indices for each delay model/gate/technology
- Data obtained by varying V_{DD}, V_{T0}, C_L
- HSPICE delay of a gate is measured for its worst case input combination
- Modified Centroid of Power (CPM) has correlation $\geqslant 0.98$ consistently

Conclusion

- Provide theoretic proof that the classic Sakurai-Newton delay model is indeed Elmore delay
- We propose a new closed form delay model based on the modified centroid of power (modify the Elmore)
- Our proposed metric has very high correlation $(\geqslant 0.98)$ compared to HSPICE simulations
- We expect this simple, accurate and robust gate delay model be used
  - in low power, low voltage circuit designs
  - in inner optimization loop of physical design tools where it is necessary to obtain quick and accurate delay estimates