Process-Induced Skew Reduction in Nominal Zero-Skew Clock Trees

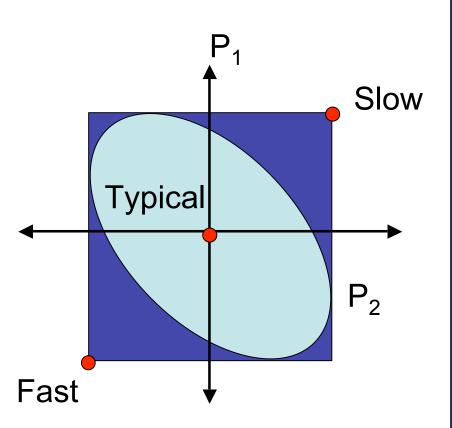
Matthew R. Guthaus, Univ. of Michigan Dennis Sylvester, Univ. of Michigan Richard B. Brown, Univ. of Utah

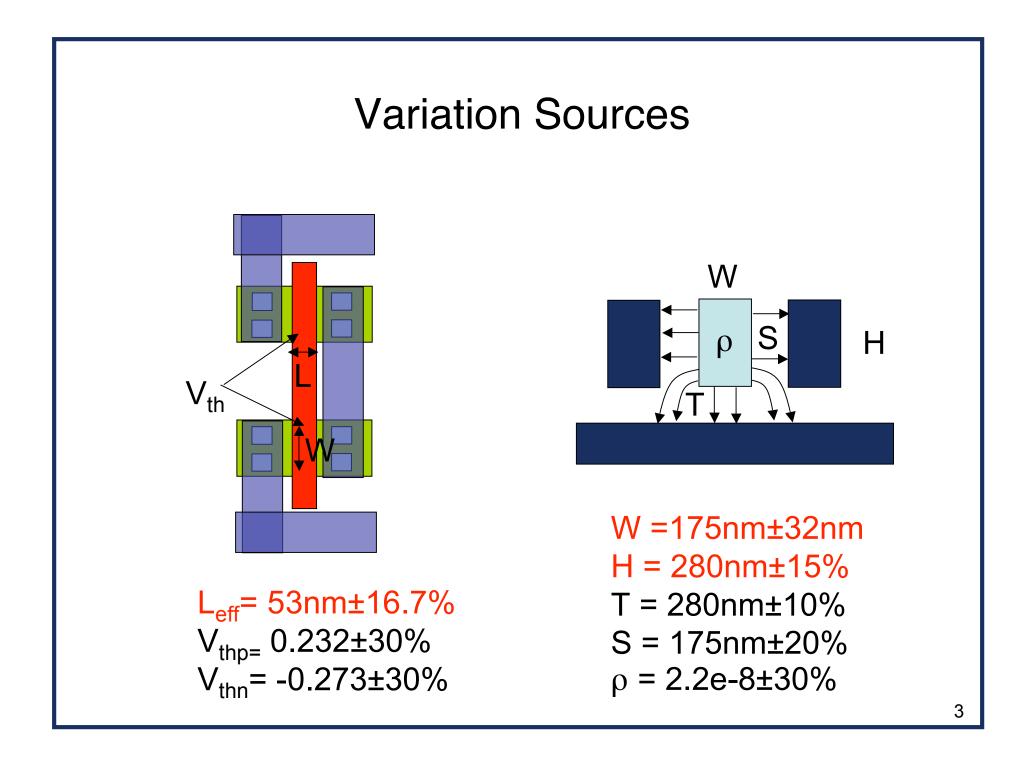


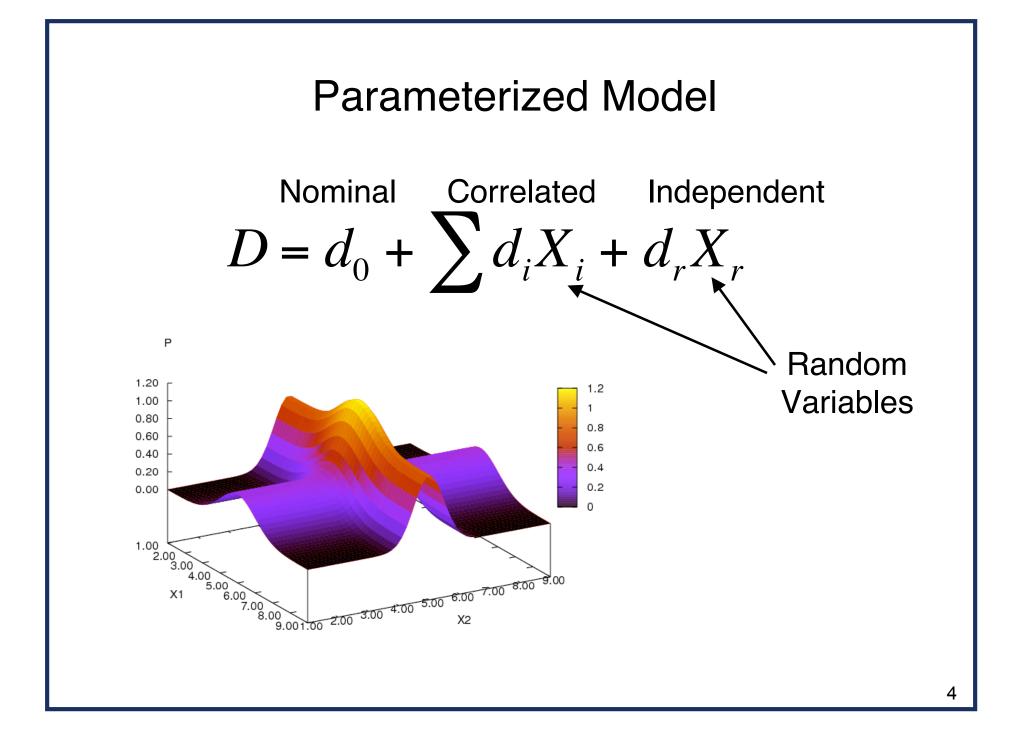


Motivation

- Variation is increasing
- Number of sources is increasing
 - Environmental (temperature, voltage, etc.)
 - Physical (lithography, materials, etc.)
 - Fatigue (NBTI, metal migration, etc.)
- Need statistical optimization
 - Process-Voltage-Temp (PVT) Optimization

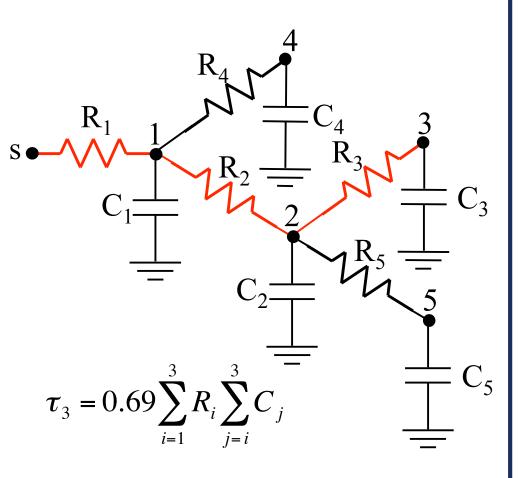


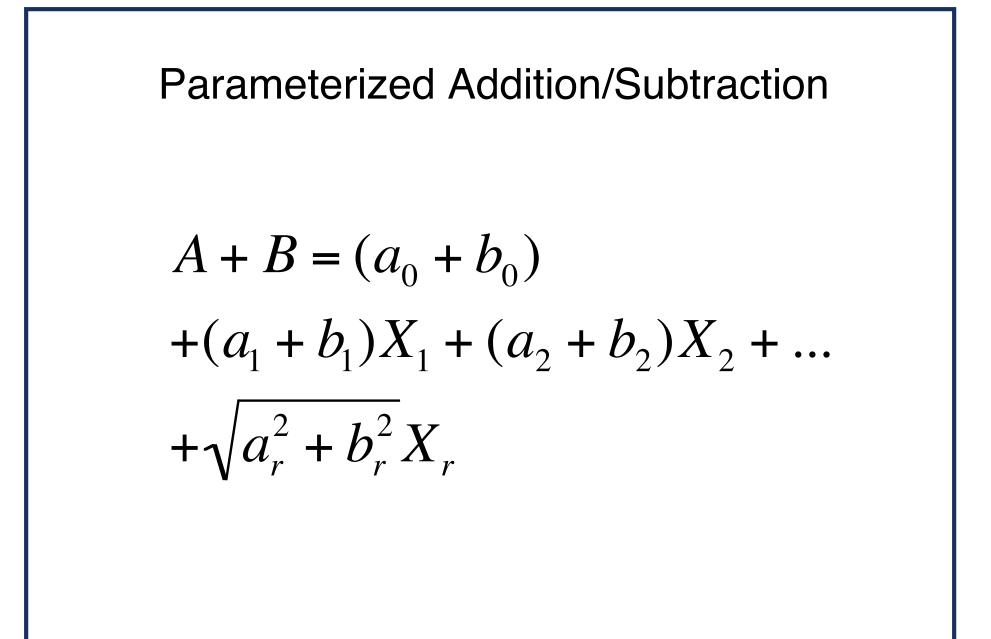




Elmore Delay

- Not accurate, but high fidelity.
- Results can be tuned later with better models.
- Fast for optimization.

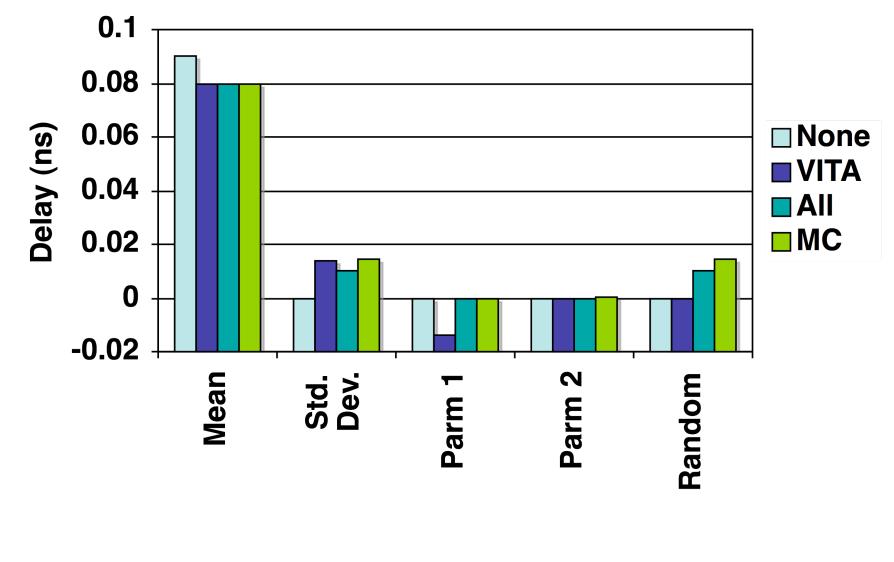




Parameterized Multiplication

AxB	a ₀ +	a ₁ X ₁ +	a ₂ X ₂ +	a _r X _r
b ₀ +	a ₀ b ₀	$a_1b_0X_1$	$a_2b_0X_2$	a _r b ₀ X _r
b ₁ X ₁ +	a ₀ b ₁ X ₁	a ₁ b ₁ (X ₁) ²	a ₂ b ₁ X ₁ X ₂	a _r b ₁ X ₁ X _r
b ₂ X ₂ +	a ₀ b ₂ X ₂	a ₁ b ₂ X ₁ X ₂	a ₂ b ₂ (X ₂) ²	a _r b ₂ X ₂ X _r
b _r X _r	a ₀ b _r X _r	a ₁ b _r X ₁ X _r	a ₂ b _r X ₂ X _r	a _r b _r (X _r) ²

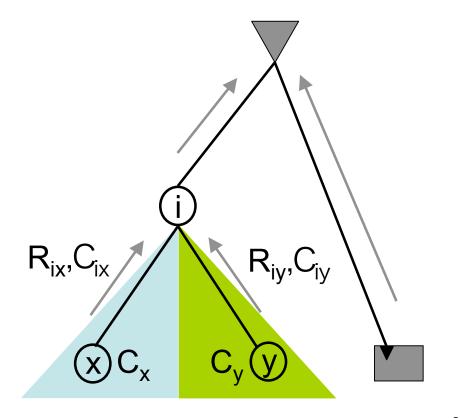
Multiplication Results - Anticorrelated



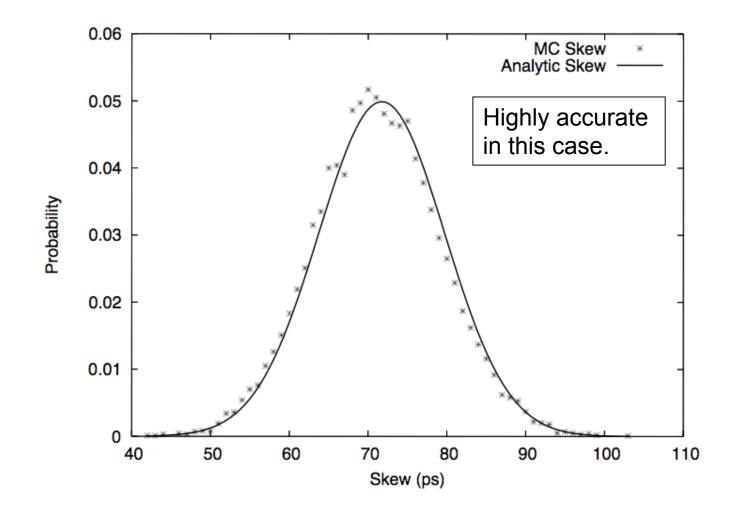
Statistical Analysis

$$D_{\max,i} = MAX(R_{ix}(\frac{C_{ix}}{2} + C_x) + D_{\max,x}, R_{iy}(\frac{C_{iy}}{2} + C_y) + D_{\max,y})$$

- Similar for D_{min,i.}
- These are parameterized R, C, and D values.

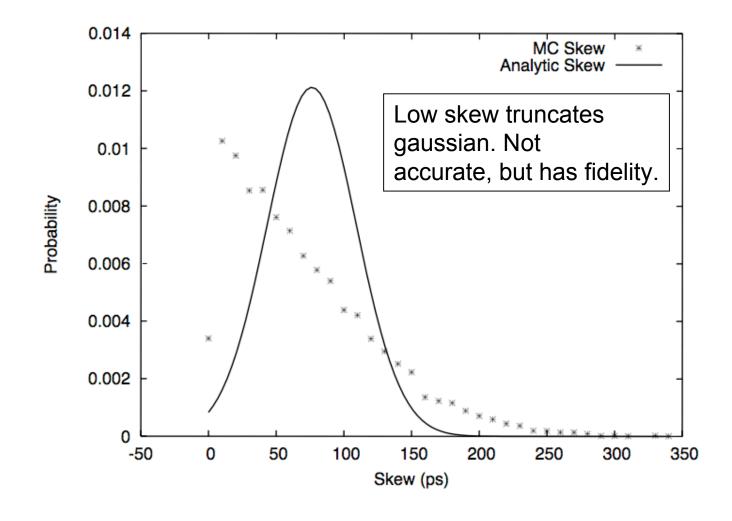


S1423, Buffered: Analytic vs. Monte Carlo



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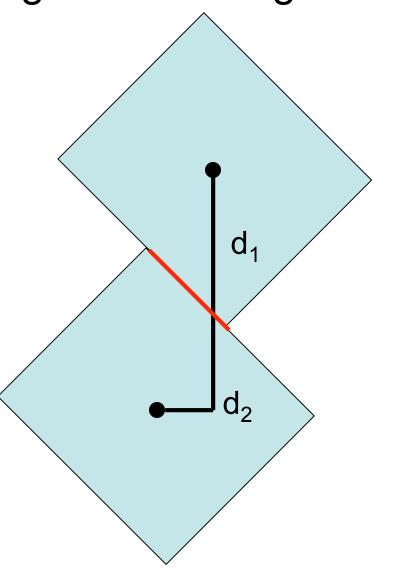
R1, No Buffers: Analytic vs. Monte Carlo

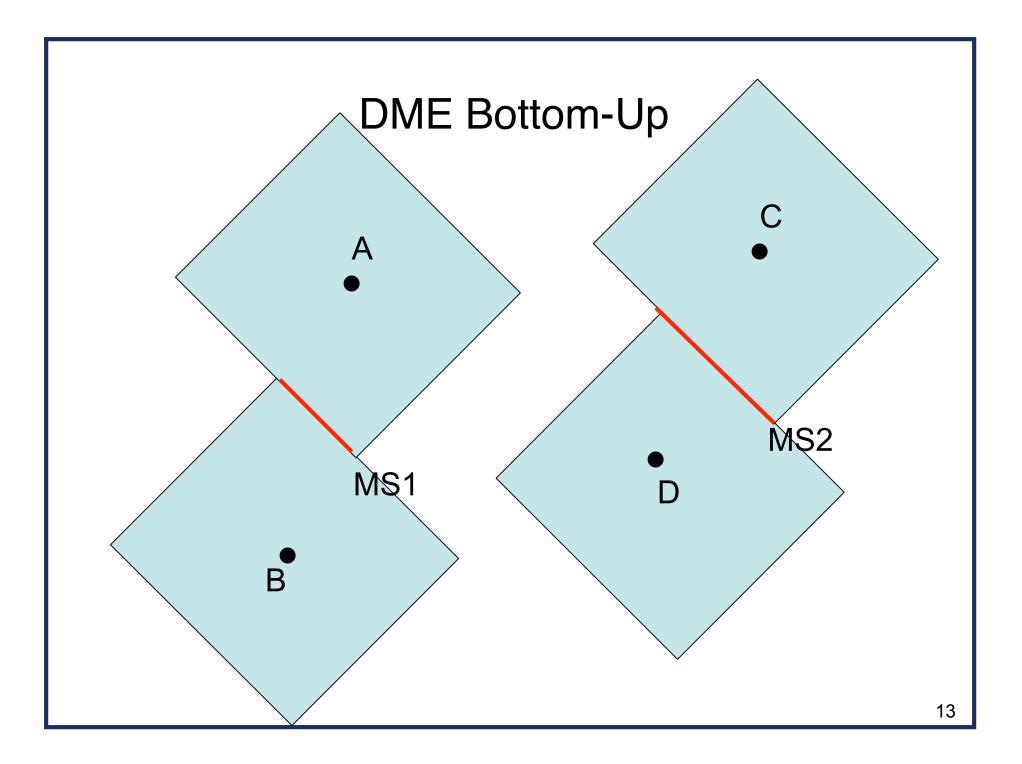


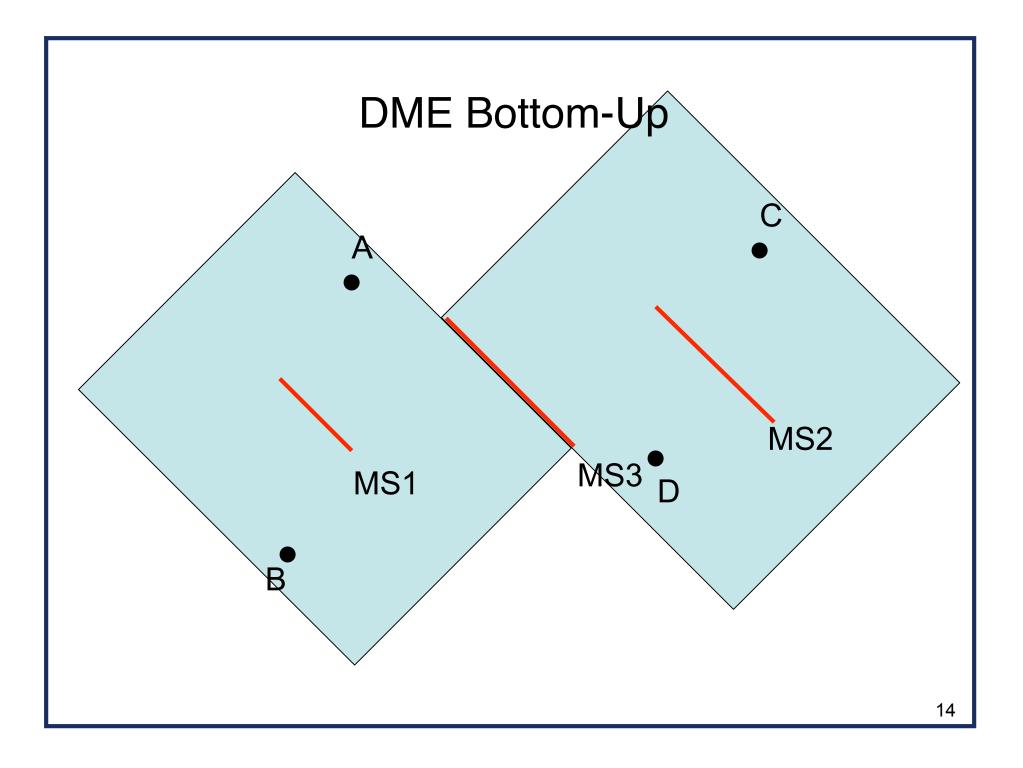
11

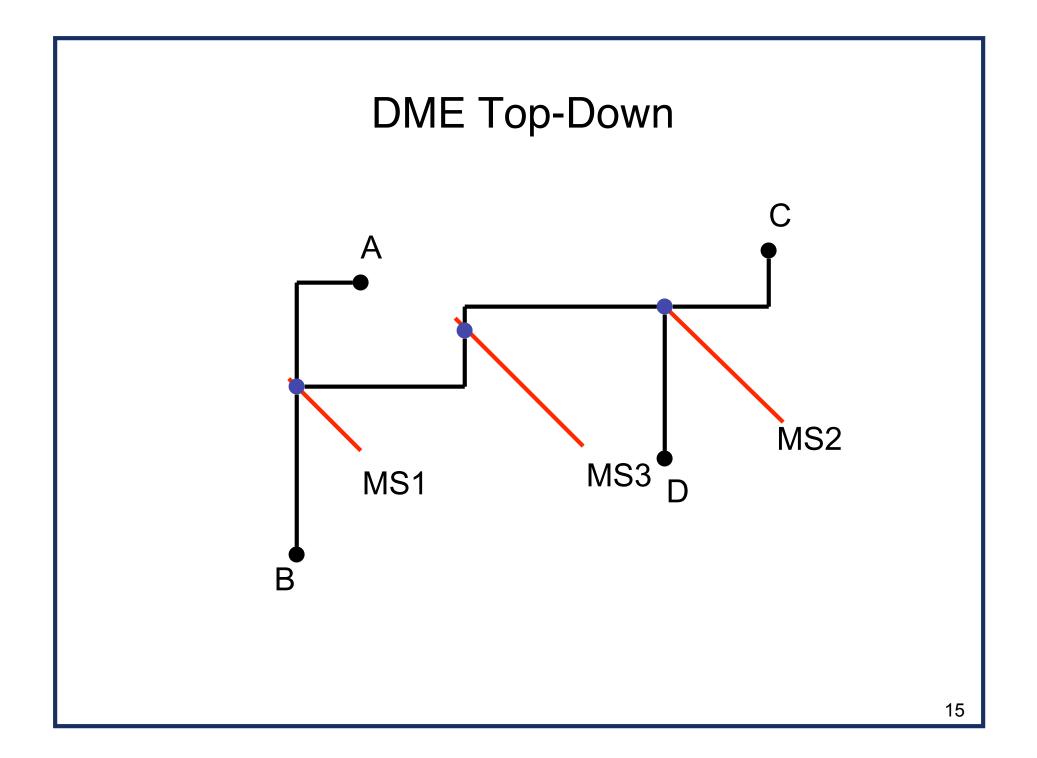
Deferred Merge Embedding

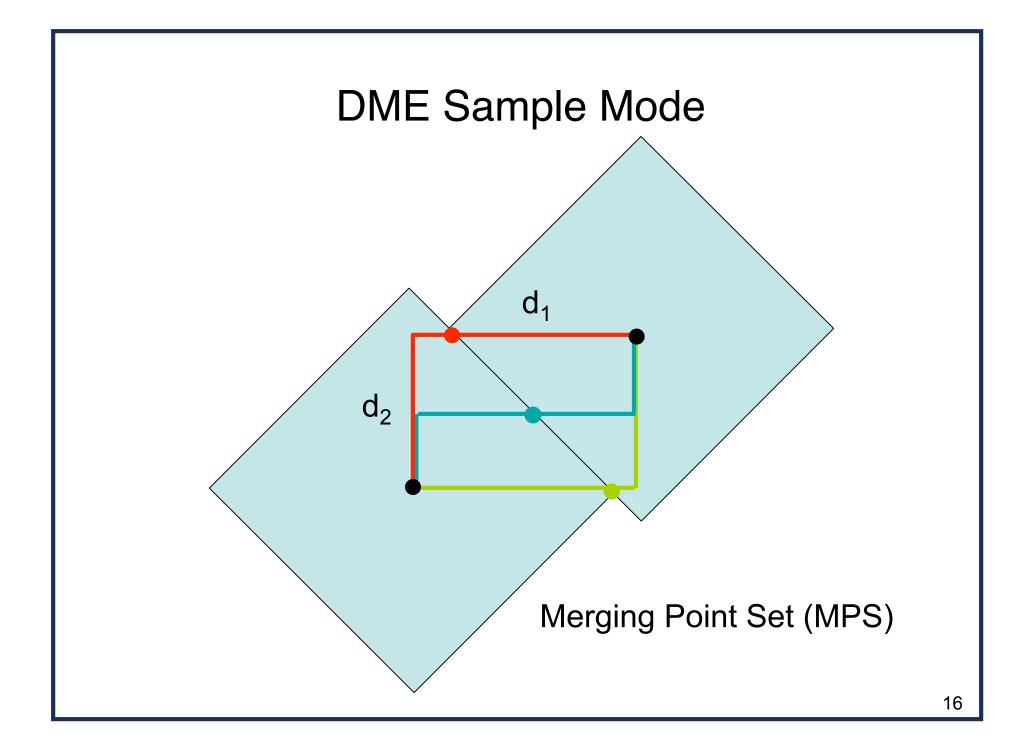
- d₁ and d₂ picked to equalize Elmore delay
- Extra wire jogs may be needed
- Topology is fixed

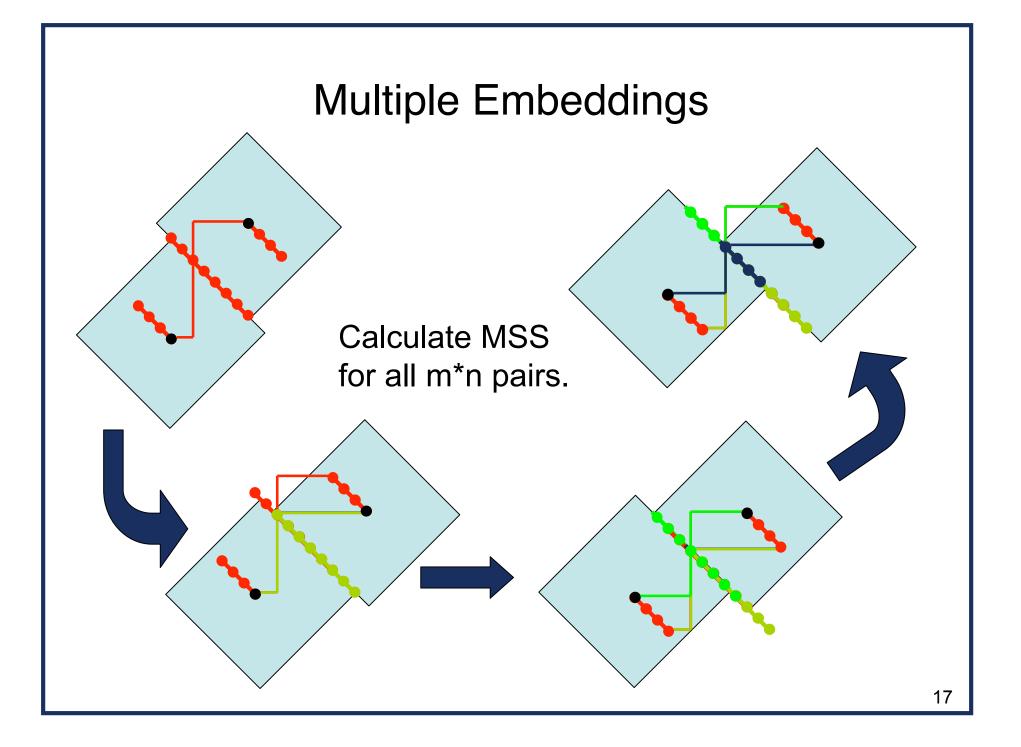






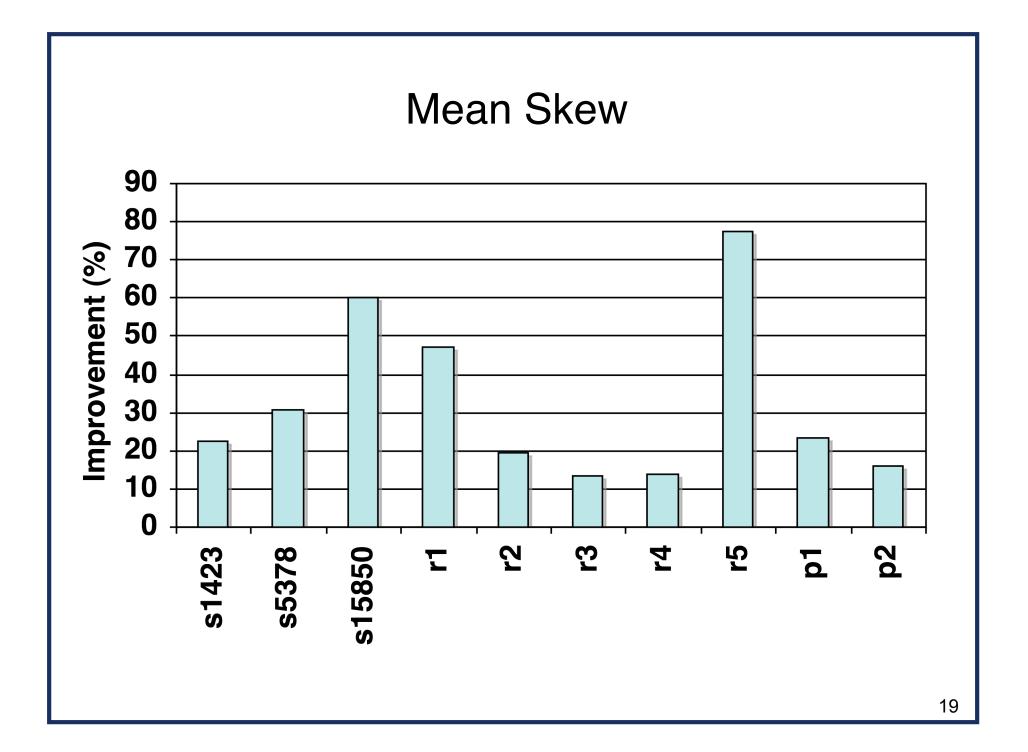


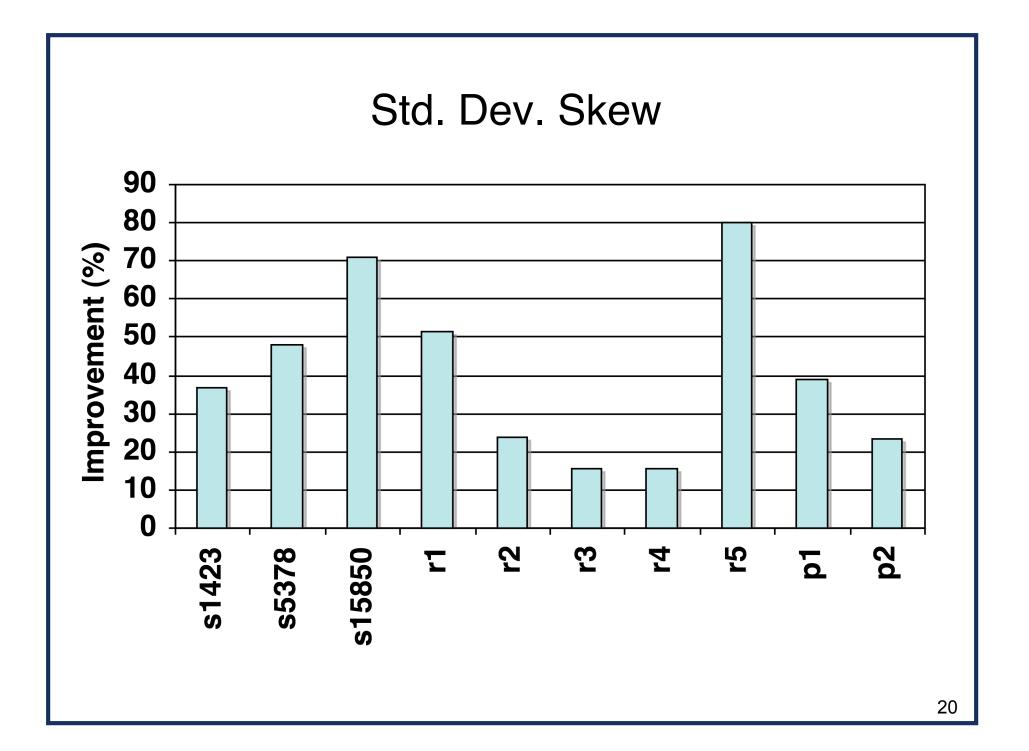


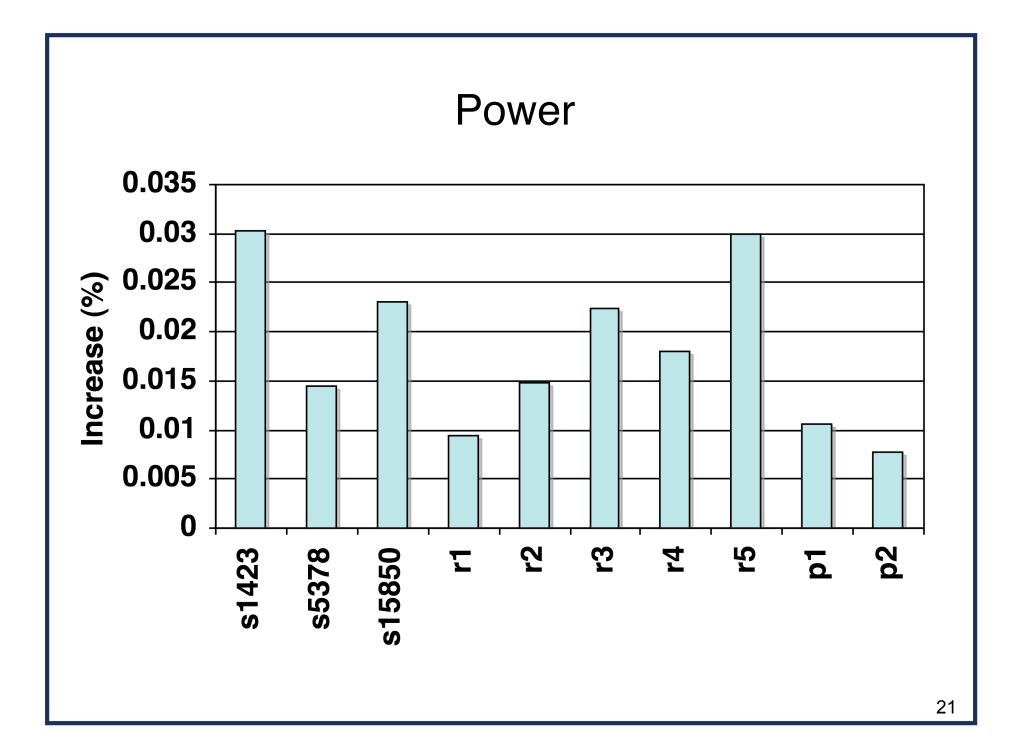


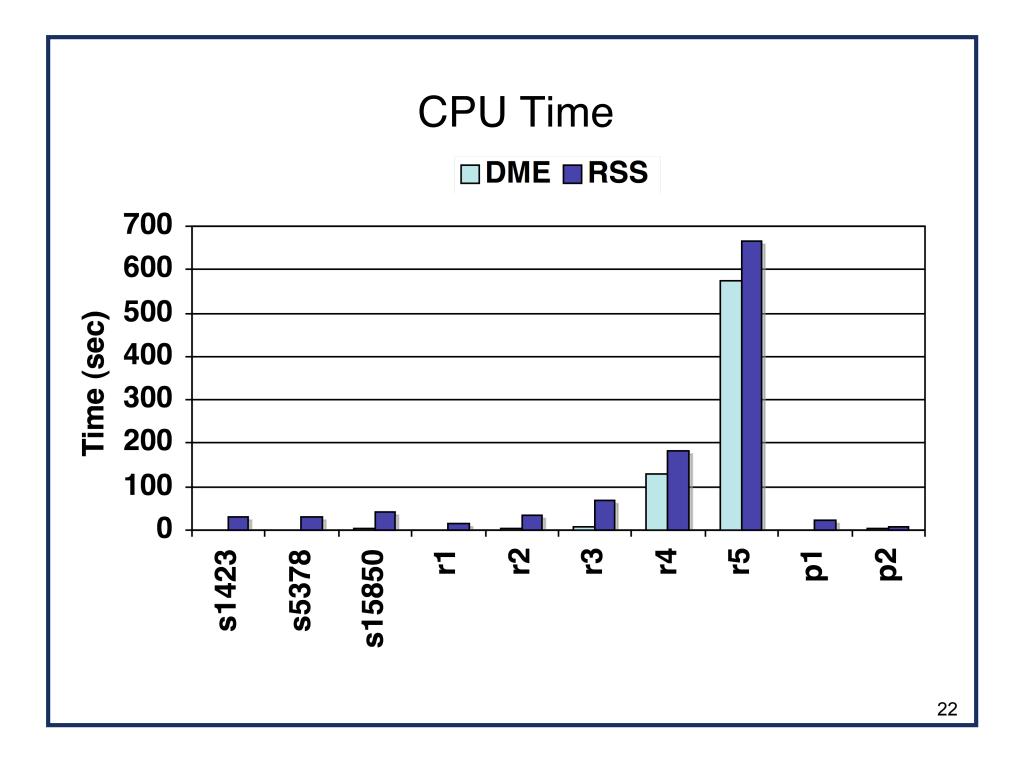
Pruning Strategies

- Parameterized Capacitance
 - Merging to same location with same sinks gives same cap.
 - Elmore does not have resistive shielding.
- Parameterized Delay
 - Delay difference is small, but present.
 - Whether to use D_{min} or D_{max} (or average) is unclear.
- Parameterized Local Skew
 - Keeping best mean skew candidate performs well.
 - Skew of any sub-tree limits the entire tree.









Conclusions

- 12-75% mean skew reduction
- 15-80% std. dev. skew reduction
- Less than 0.03% power increase
- Run-time can be traded for power suboptimality
- Future Work
 - Topology Generation
 - Buffer Insertion
 - Wire Width Tuning