A Low Dynamic Power and Low Leakage Power 90-nm CMOS Square-Root Circuit

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Power Reduction Techniques

1. Dynamic Power of the CMOS circuit

$$P_{AT} = f_c V_D^{\,2} \sum_{g=1}^{G} C_{Lg} = f_c V_D^{\,2} G(\text{ave.} C_{Lg}) = k_{AT} G V_D^{\,2}$$

To reduce P_{AT}, $V_D^{\,2}$ and G should be decreased, while f_c must be kept constant

2. Leakage Power of the CMOS circuit

$$P_{ST} = V_D \sum_{g=1}^{G} I_{Lg} = V_D G(\text{ave.} I_{Lg}) \approx k_{ST} G V_D$$

To decrease P_{ST}, G and V_D should be reduced

3. Clock Frequency & Supply Voltage

$$f_c = \frac{(V_D - V_t)^2}{V_D \sum_{g=1}^{G_c} \frac{C_{Lg}}{\beta_g}} \approx \frac{V_D - 2V_t}{\sum_{g=1}^{G_c} \frac{C_{Lg}}{\beta_g}}$$

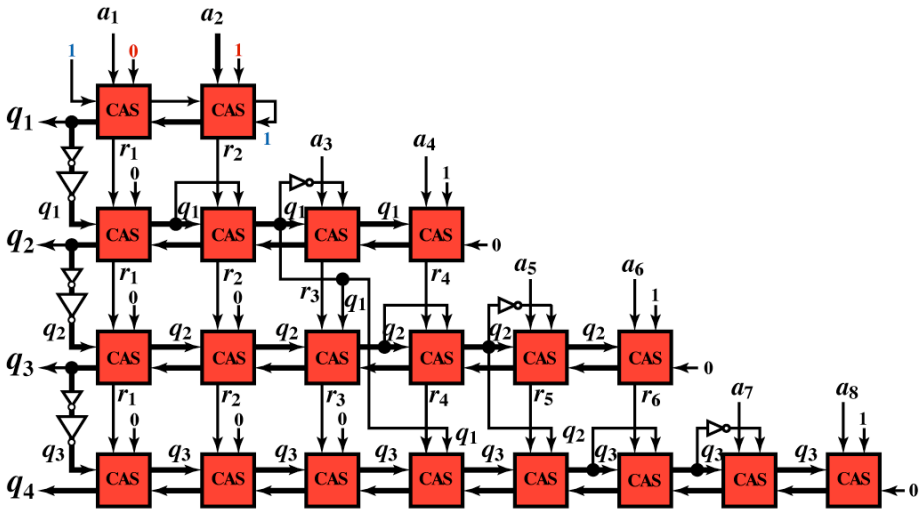
$$V_D - 2V_t \approx f_c \sum_{g=1}^{G_c} \frac{C_{Lg}}{\beta_g} = f_c G_c(\text{ave.} \frac{C_{Lg}}{\beta_g}) = k_{VD} G_c$$

To reduce V_D, G_c should be decreased

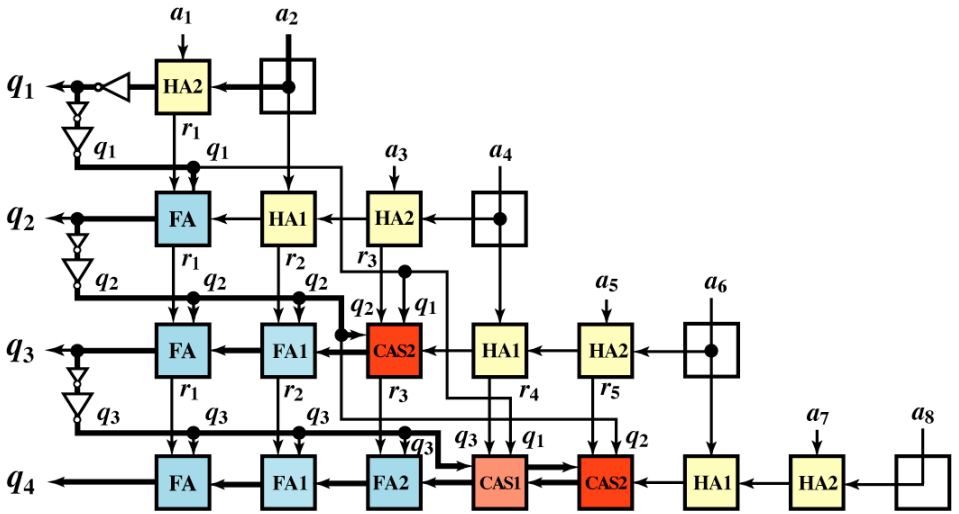
f_c = Clock frequency
V_D = Supply voltage
C_{Lg} = Load capacitance of the gth logic gate
I_{Lg} = Leackage current of the gth logic gate
G = Number of total logic gates
G_c = Number of critical path logic gates

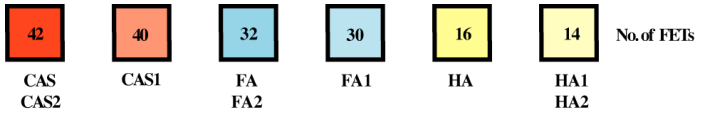
8-bit Square-Root (SR) Circuit

Conventional SR Circuit (C-SR)



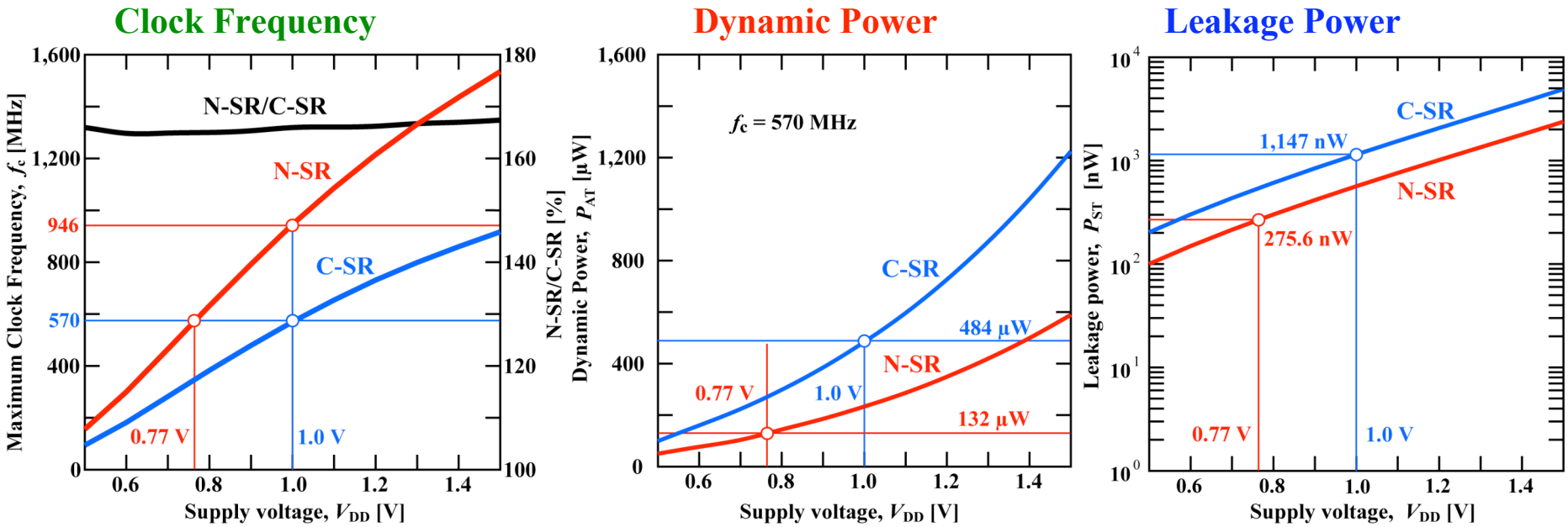
New SR Circuit (N-SR)





	C-SR	N-SR	N-SR/C-SR
No. of logic gates, G	$G = 189$	$G' = 89$	47.1%
No. of CP logic gates, G_c	$G_c = 62$	$G_c' = 30$	48.4%
Supply voltage, V_D	$V_D \approx k_{VD}G_c + 2V_t$	$V_D' \approx k_{VD}G_c' + 2V_t$	-
Active power, P_{AT}	P_{AT}	$P_{AT}' = (G'/G)(V_D'/V_D)^2 P_{AT}$	$(G'/G)(V_D'/V_D)^2$
Stand-by power, P_{ST}	P_{ST}	$P_{ST}' \approx (G'/G)(V_D'/V_D)\, P_{ST}$	$(G'/G)(V_D'/V_D)$

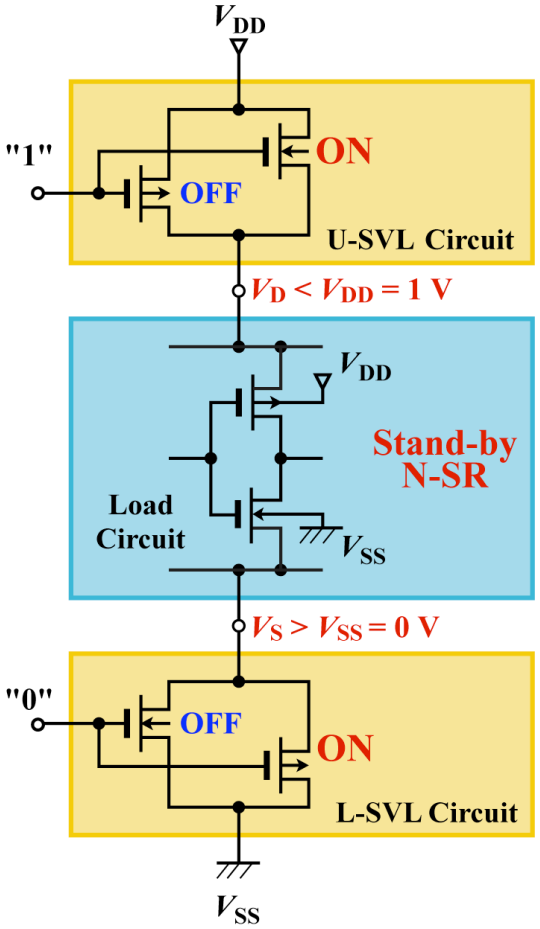
Max. Clock Freq. (f_c), Dynamic power (P_{AT}) & Leakage Power (P_{ST}) of 8-bit, 90-nm Square-Root Circuits



	C-SR	N-SR	N-SR/C-SR (%)	Note
No. of logic gates, G	189	89	47.1	
No. of CP logic gates, G_c	62	30	48.4	
Supply voltage, V_D [V]	1.00	0.77	77	
Active power, P_{AT} [µW]	484.0	131.9	27.1	at f_c = 570 MHz
Stand-by power, P_{ST} [nW]	1,147	275.6	24.0	

New Square-Root Circuit with SVL Circuits (N-SR-S)

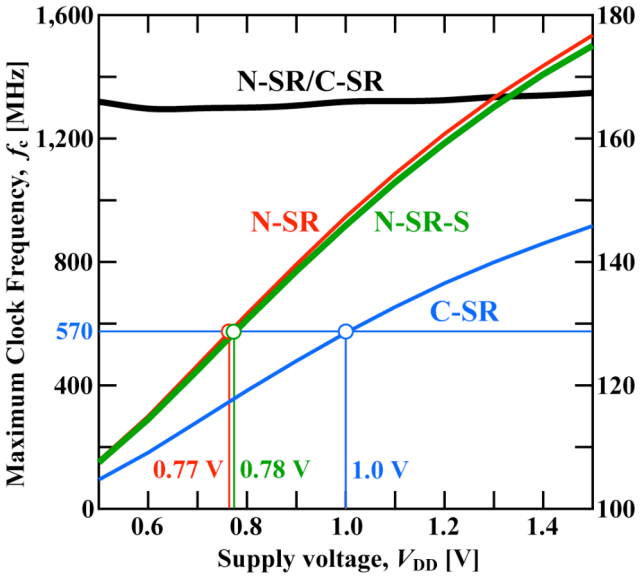
SVL; Self-controllable-Voltage-Level



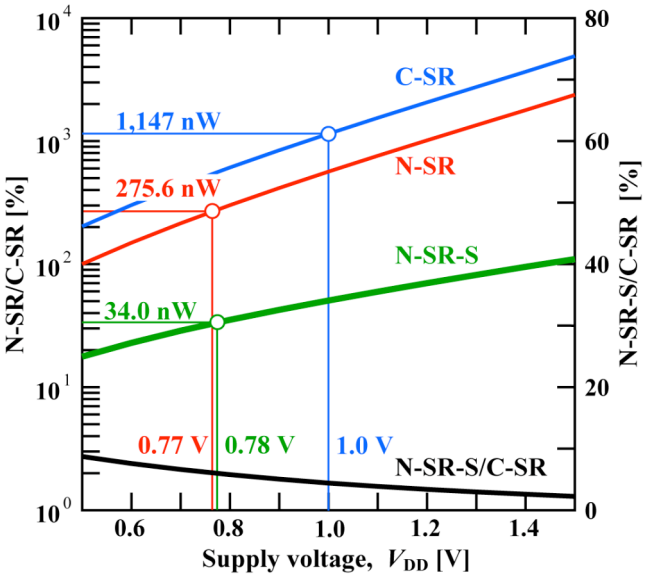
Upper SVL Circuit :
nMOS Switch is Turned on
V_D ($<V_{DD}$) is Supplied

Lower SVL Circuit :
pMOS Switch is Turned on
V_S ($>V_{SS}$) is Supplied

Clock Frequency

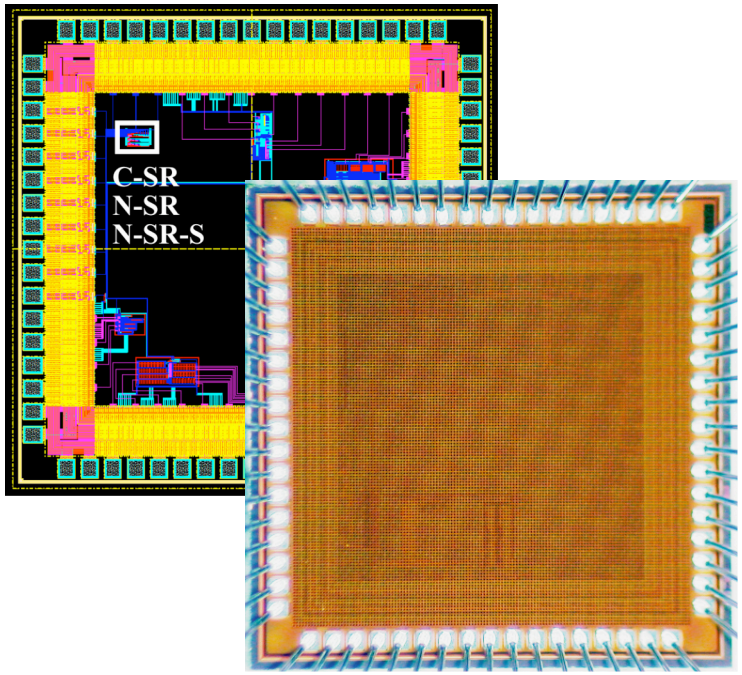


Leakage Power



	C-SR	N-SR	N-SR-S	N-SR-S/C-SR (%)
No. of logic gates, G	189	89	91	48.2
No. of CP logic gates, G_c	62	30	30	48.4
Supply voltage, V_D [V]	1.00	0.77	0.78	78
Active power, P_{AT} [μW] at f_c = 570 MHz	484.0	131.9	132.0	27.3
Stand-by power, P_{ST} [nW]	1,147	275.6	34.0	2.97

90-nm CMOS LSI Chips with 8-bit SR Circuits & Experimental Results



Technology: 90-nm, 6-Layer Cu, CMOS
Chip Size: 2.5 mm × 2.5 mm
V_{tn} = 0.222 V, V_{tp} = -0.241 V

	C-SR	N-SR	N-SR-S
No. of logic gates, G (Ratio [%])	189 (100)	89 (47.1)	91 (48.2)
Active area sizes, A [μm²] (Ratio [%])	972 (100)	505 (51.9)	558 (57.4)