High-Throughput Decoder for Low-Density Parity-Check Code

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Introduction

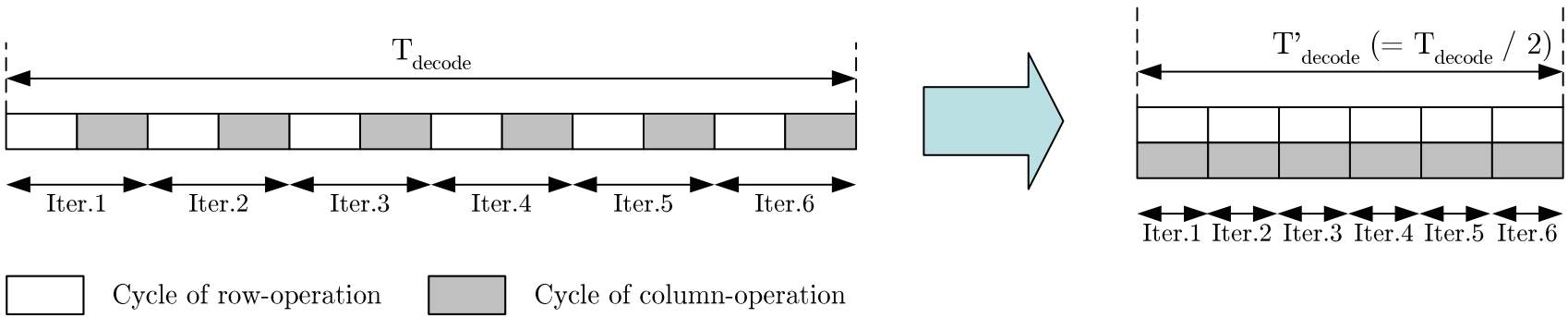
- Low-Density Parity-Check (LDPC) codes are the next generation of Error-Correcting Code

- Previous decoders
  - High-Throughput and short code-length about 1000-bit
    - 1 Gb/s and 1024-bit for optical fiber channel, etc.
  - Long code-length and slow less than 200 Mbps
    - 64800-bit and 135 Mb/s for DVB-S2

- ✓ Necessary to achieve both High-Throughput and long code-length for widely use

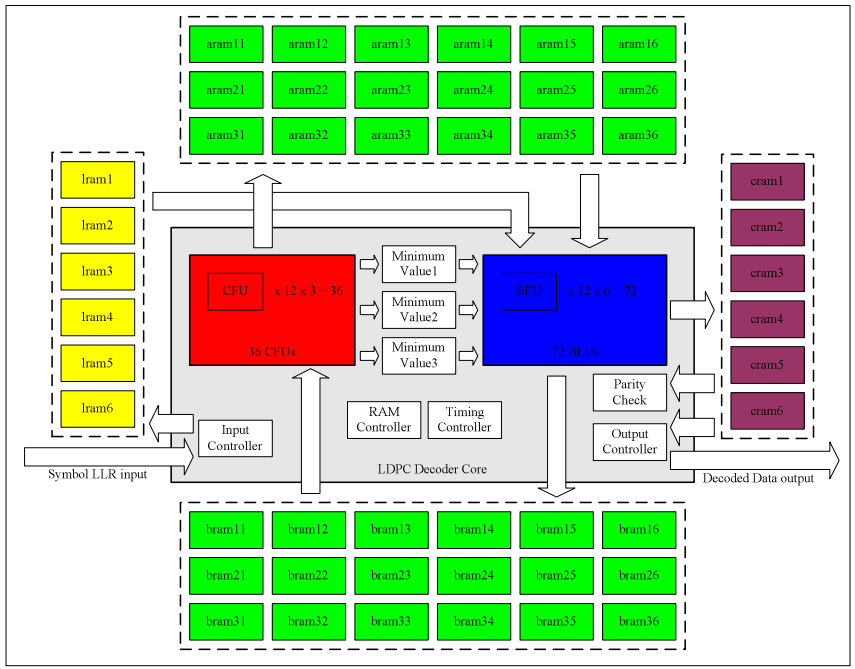
Two improved methods

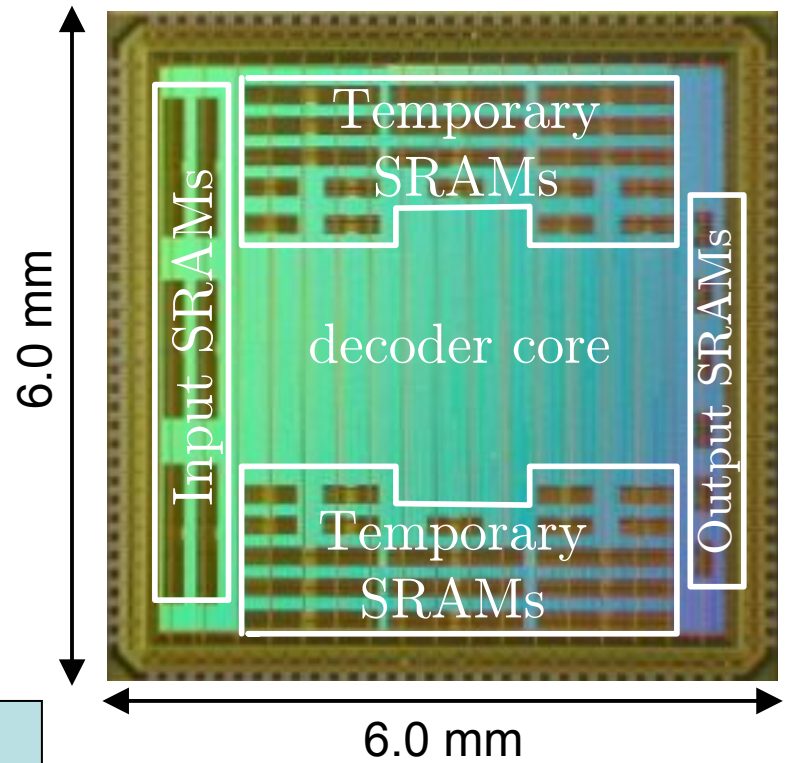
- ✓ High-Throughput
  - ◆Row-operations and Column-operations are operated concurrently



- ✓ Memory reduction for long code-length
  - ◆Using characteristic of Row-operation on Min-Sum algorithm
    - ➢ Two absolute values or Three signed values per row

Block diagram & Microphotograph





Check-node Function Unit

Bit-node Function Unit

decoder core

Input SRAMs

Output SRAMs

Temporary SRAMs

Specifications of LDPC decoder chip

LDPC code	(3,6) – 2304 bit, regular LDPC code
Design process	0.18 um, 6M, CMOS
Chip (die) size	6.0 mm x 6.0 mm
Gate count (Decoder core)	206,343 gates
Embedded SRAMs	85,248 bits (48 instances)
Clock frequency	147 MHz (Max.)
Throughput	530 Mb/s (@147MHz, 10 iterations)
Power consumption	3.6 W (@147MHz, 10 iterations)