Hardware Implementation of Super Minimum All Digital FM Demodulator

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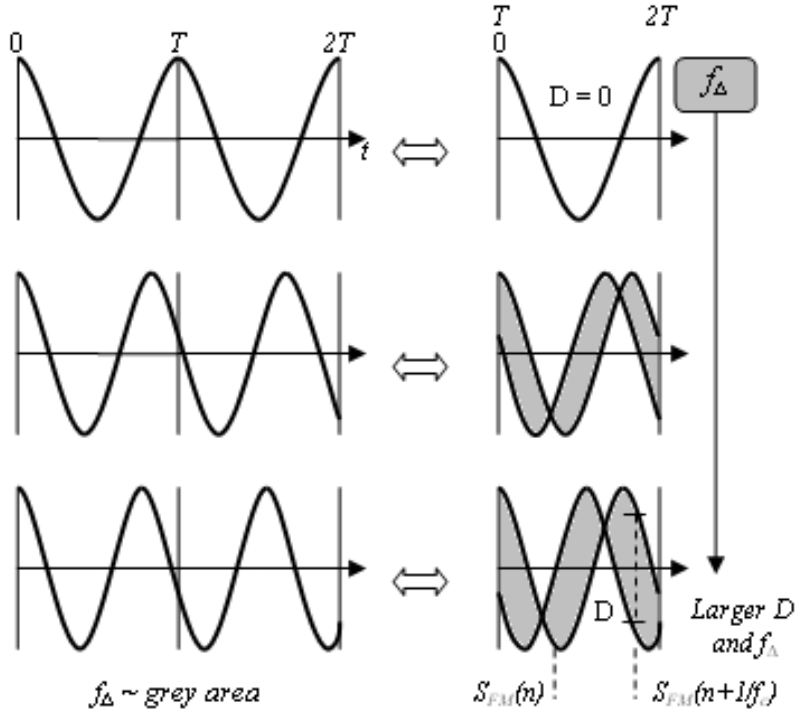
Introduction

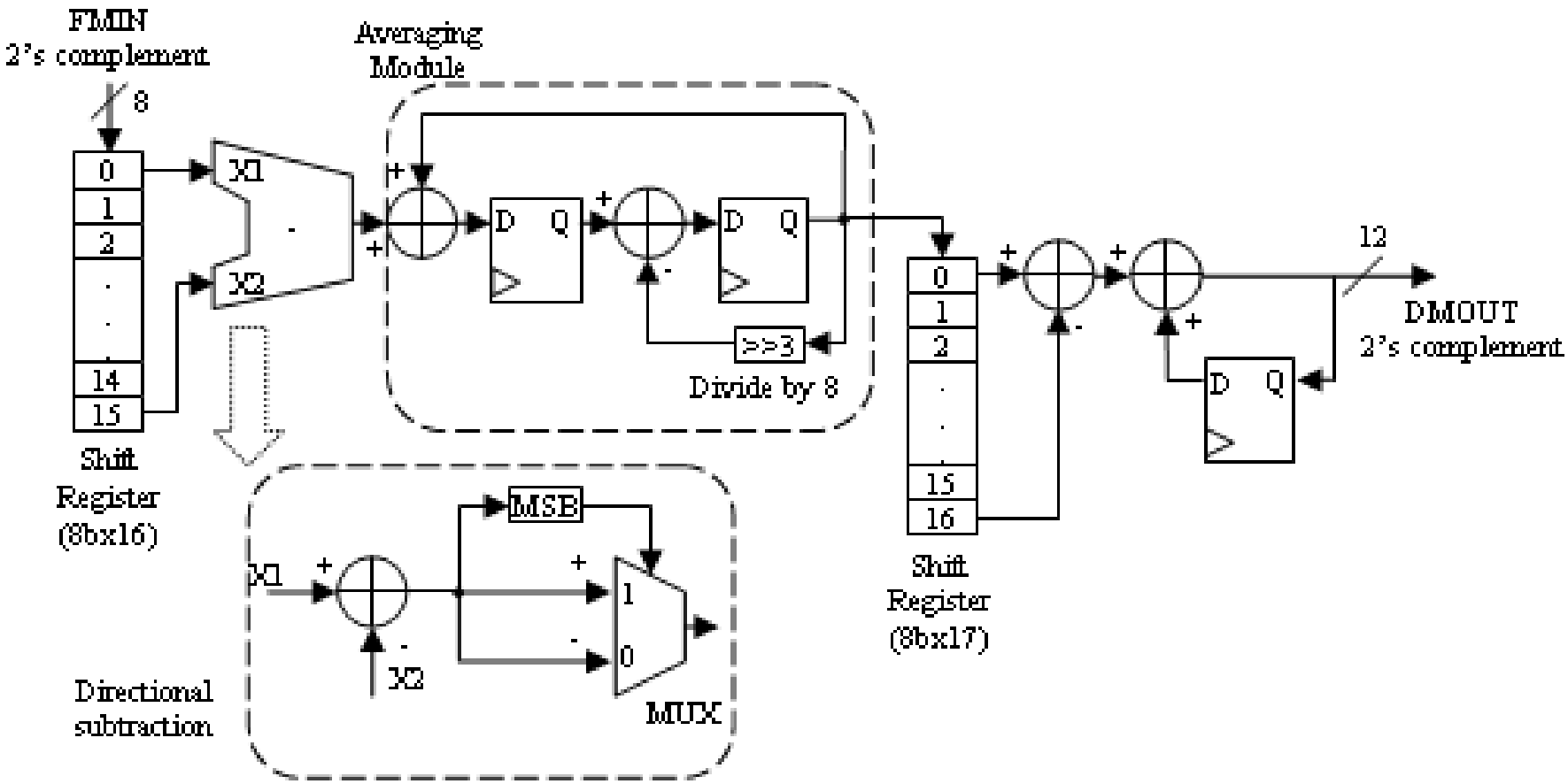
- We propose improvement for new architecture of all-digital FM demodulator.
- This work enhances signal quality, system clock frequency, and superior than well known PLL technique today.
- No more multiplier, no more ROM or table, compact size, and very fast in transient or state response, SNR = 30.6 dB
- Real implementation in Altera® APEX20K200 EBC652-1X PLD gives 348 logic elements and run up to 224.42 MHz.

New FM demodulation algorithm

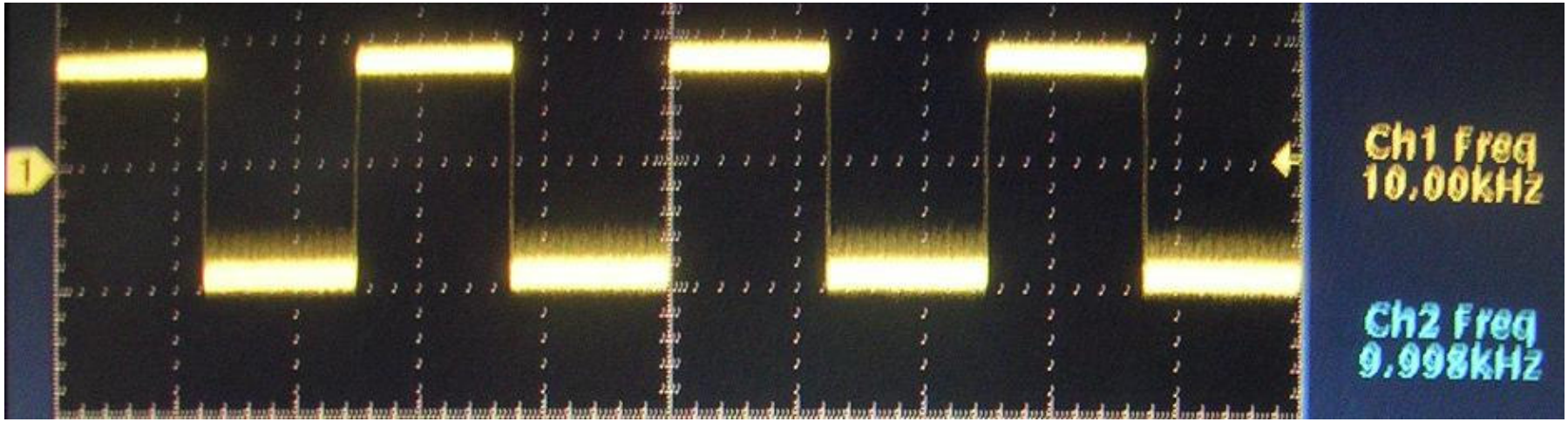
- The new algorithm assumes that process in FM demodulation is equivalent with tracking for frequency deviation. Tracking process is performed for each period of cycle



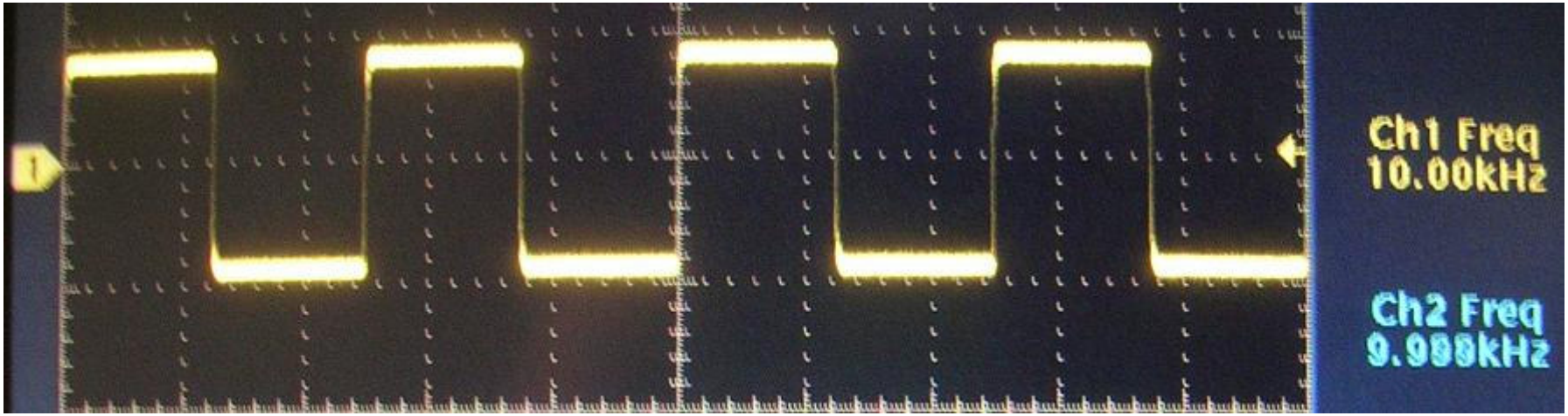
Proposed Architecture



Implementation Result



- Basic architecture



- Proposed architecture