Designing a Custom Architecture for DCT Using NISC Design Flow

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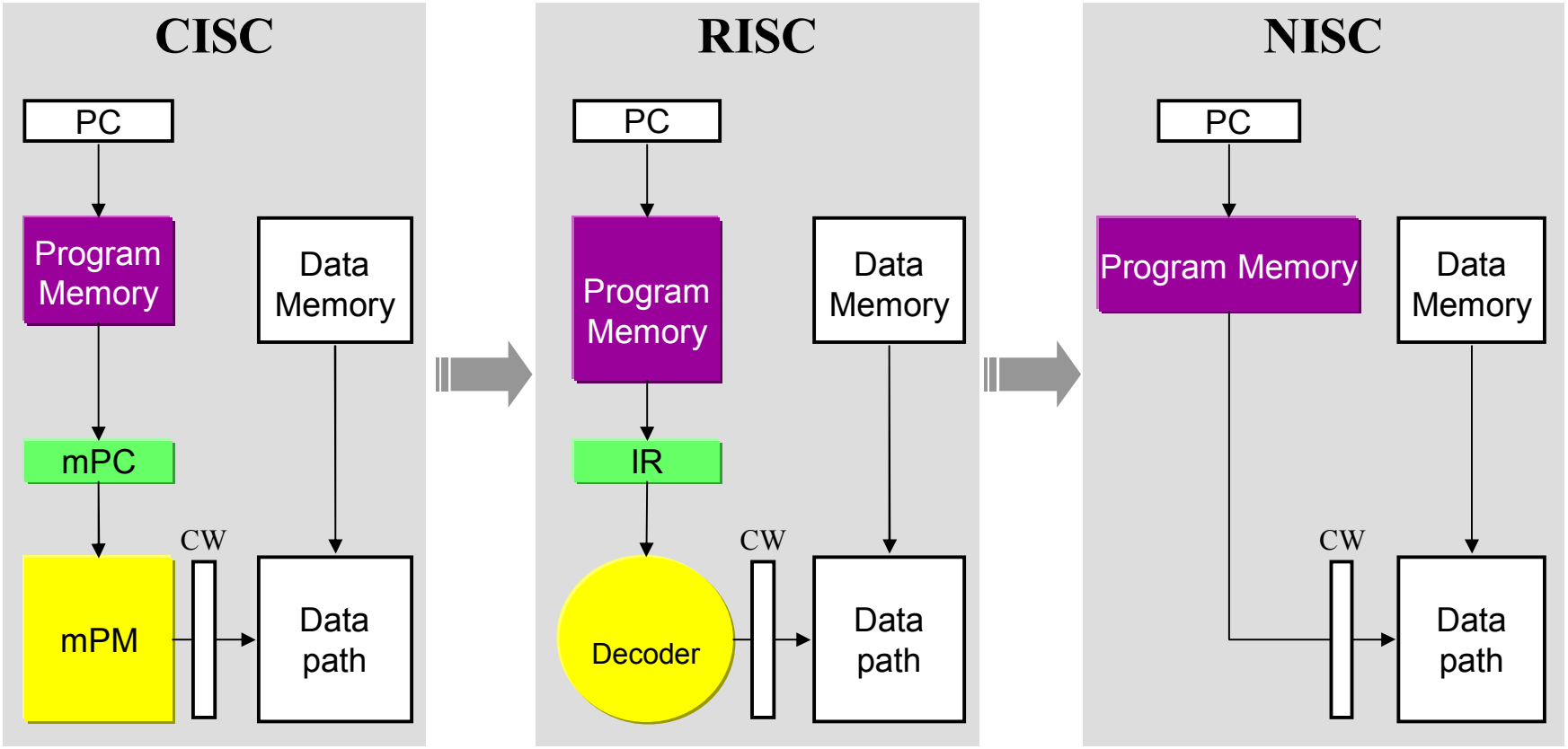
NISC Technology



Complex instructions
One instruction = several CW
PM standard

Simple instructions
One instruction = One CW
PM longer

No instructions
Several operations = One CW
PM shorter and wider

NISC Toolset

Web:
www.cecs.uci.edu/~nisc

Datapath

Application

NISC Tools

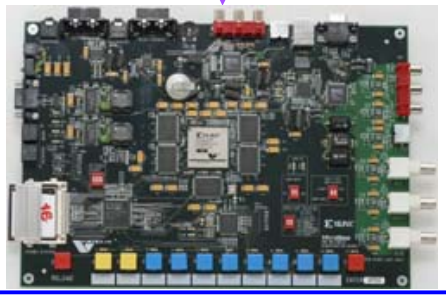
NISC Compiler

Refinement

RTL Generator

Simulator / Profiler

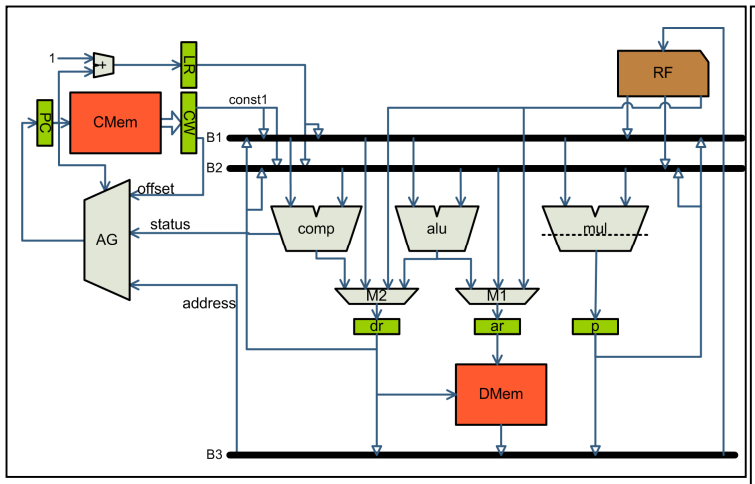
Commercial synthesis tool



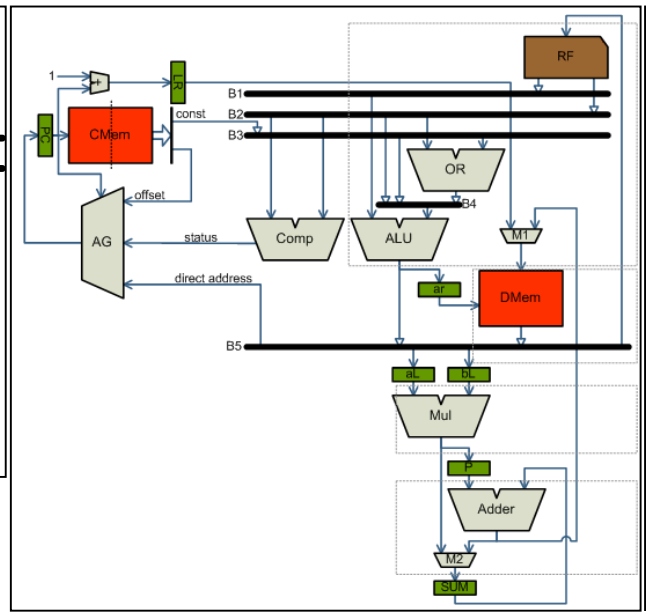
DCT example

- **Software transformations and hardware customizations**
  - Loop unrolling
  - Operation chaining
  - ALU and comparator optimization
  - Controller pipelining
  - Bit-width reduction

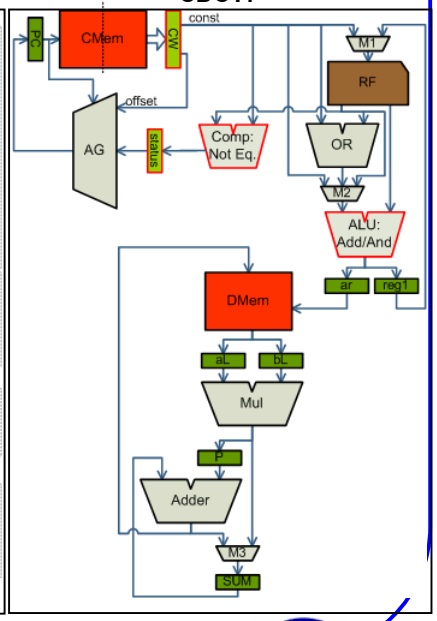
NMIPS



CDCT1

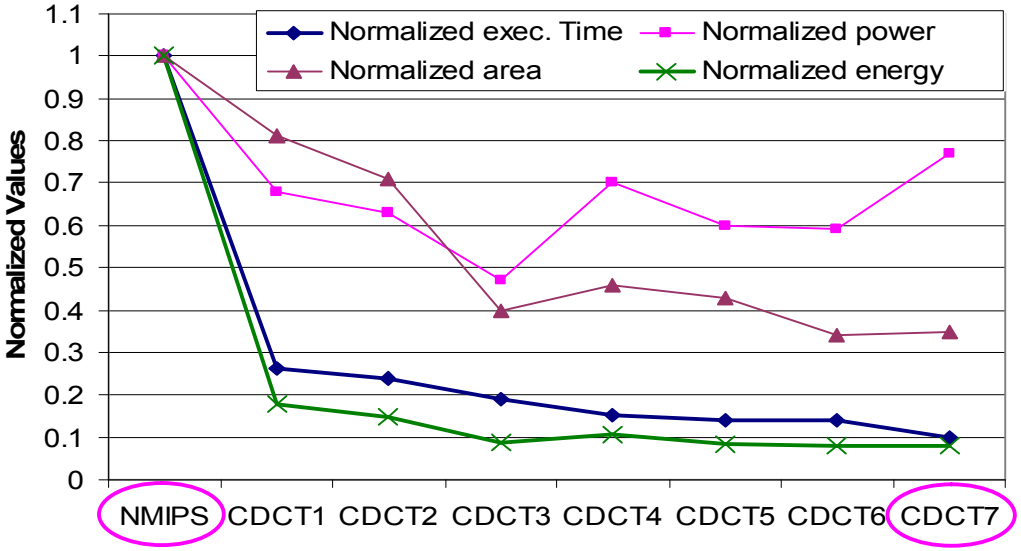


CDCT7



Summery of Results

- **Xilinx Virtex II 2000 FPGA**
- **NMIPS vs. CDCT7:**
  - 10 times performance improvement
  - 1.3 times power reduction
  - 12.8 energy reduction
  - 2.9 area reduction
- **Designs are available online**



	No. of cycles	Clock Freq (MHz)	DCT exec. Time (us)	Dynamic Power (mW)	Normalized area
NMIPS	10772	78.3	137.57	177.33	1.00
CDCT1	3080	85.7	35.94	120.52	0.81
CDCT2	2952	90.0	32.80	111.27	0.71
CDCT3	2952	114.4	25.80	82.82	0.40
CDCT4	3080	147.0	20.95	125.00	0.46
CDCT5	3208	169.5	18.93	106.00	0.43
CDCT6	3208	171.5	18.71	104.00	0.34
CDCT7	3460	250.0	13.84	137.00	0.35