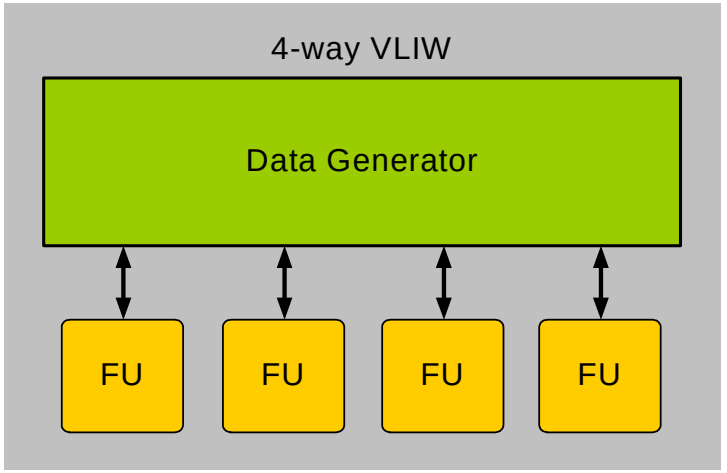
A 52mW 1200MIPS Compact DSP for Multi-Core Media SoC

Shih-Hao Ou, *Tay-Jyi Lin*, *Chao-Wei Huang*, *Yu-Ting Kuo*,
Chie-Min Chao, *Chih-Wei Liu*, and *Chein-Wei Jen*

Department of Electronics Engineering
National Chiao Tung University, Taiwan

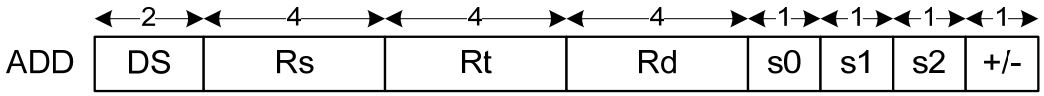
Data-Centric ISA

- Data-Centric ISA
  - The instructions specify the operands to be generated & collected by the data generator
  - Some additional control bits are also attached to the generated data operands



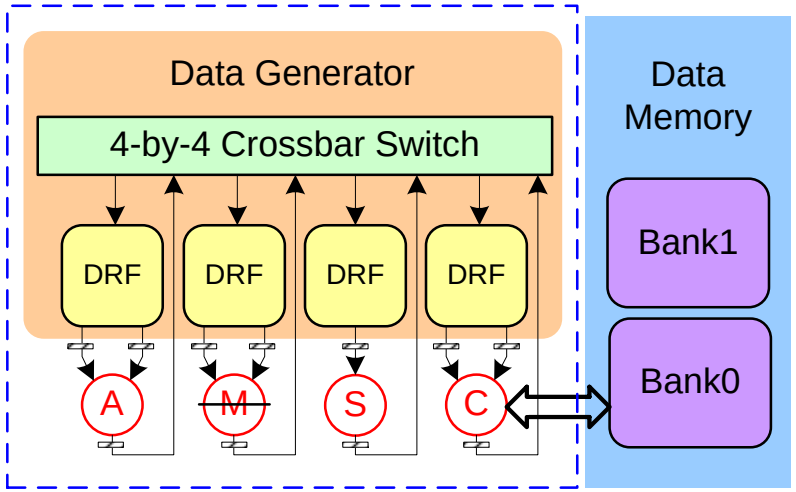
For example,

The ADD-site receives instructions as: **Rd=DS; (Rs>>+Rt>>)>>**



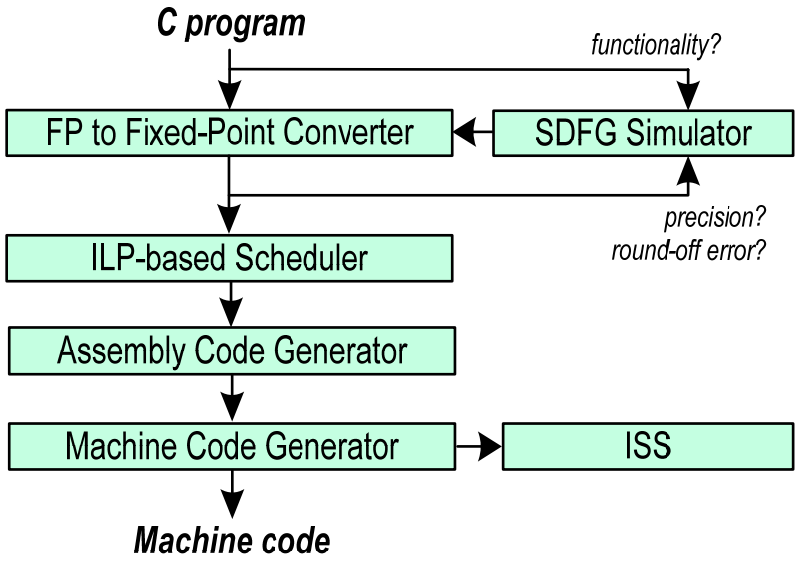
Modular & Latency-Insensitive Architecture

- Data generator
  - 4-by-4 crossbar
  - Distributed register files
- Independent sites
  - Adder
  - Multiplier
  - Shifter
  - Control site



Computing Engine

Automatic Code Generation



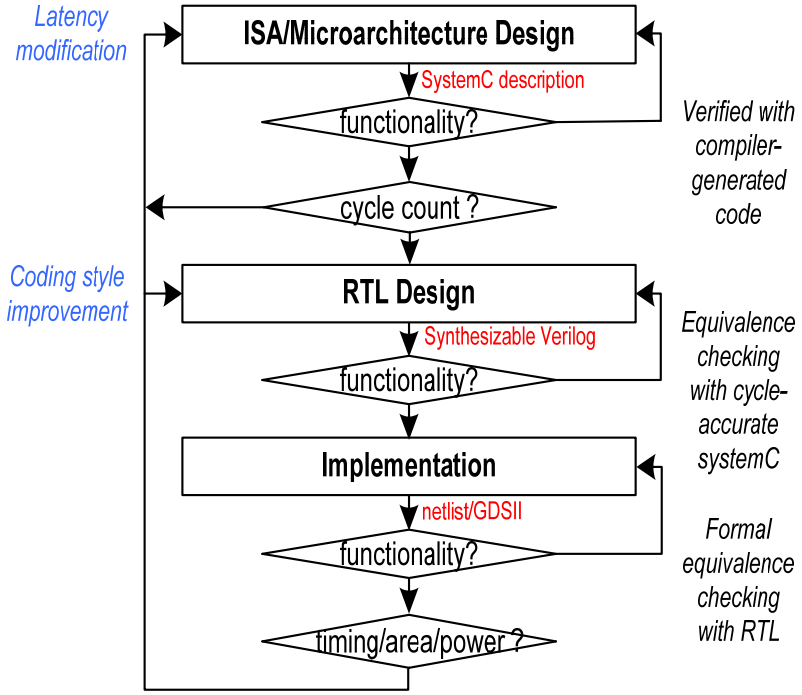
Round-off error comparison of 2D-DCT

	PSNR (dB)	Cycel count
Single-precision FP	--	624
16-bit integer	29.5183	848
32-bit interger	33.8020	656
Proposed 16-bit	**40.0468**	**656**
Proposed 32-bit	**64.1201**	**624**

Performance evaluation

	Lattice	Biquad	FFT	2D-DCT
ADSP-218x	32	13	874	2,452
TI C'55	12	5	367	1,082
Proposed DSP	**12**	**16**	**268**	**688**

Silicon Implementation



Chip spec.

Technology	UMC 0.18um 1P6M CMOS
Core size	1.5 x 1.5 mm^2
Transistor/Gate Count	197,655
Power dissipation	52 mW
Max. frequency	314 MHz
On-chip memory size	16KB (8KB data /8KB instruction)