Configurable Multi-Processor Architecture and its Processor Element Design

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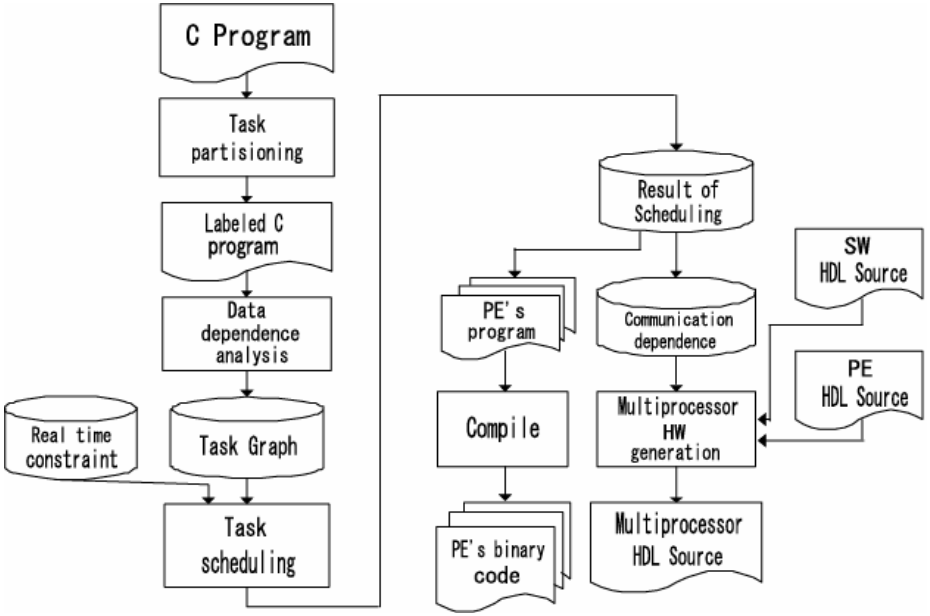
Multi-processor generation system

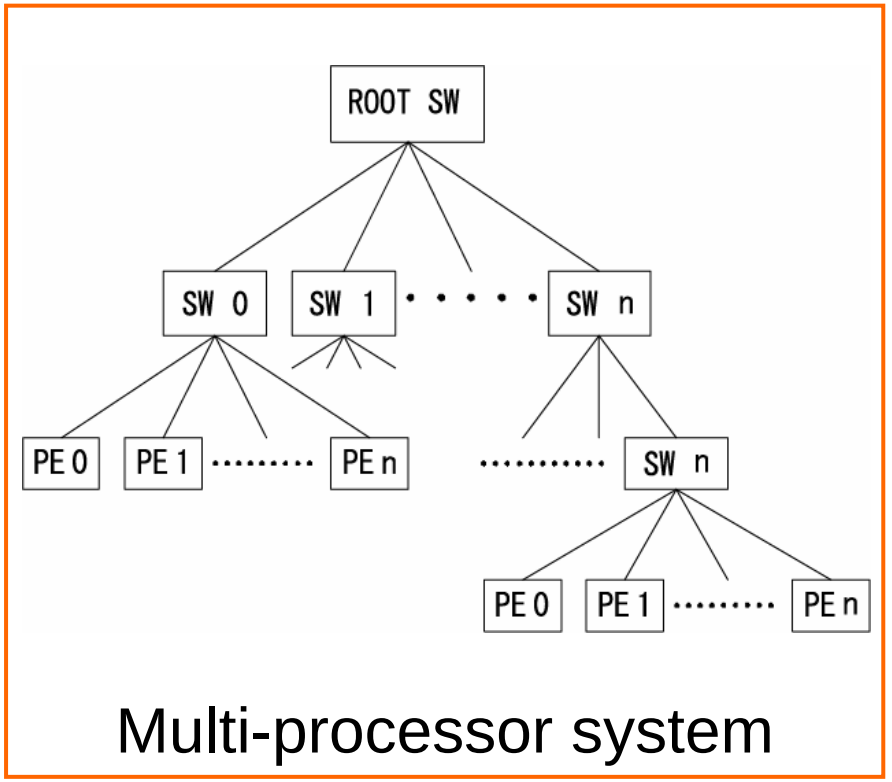
- Goal
  - To solve problem of multi-processor
  - To eliminate mismatch between hardware and software
- Source
  - C program
- Objectives
  - HDL of multi-processor
  - Software of each PE



Generation flow

Multi-processor architecture

- Feature
  - Distributed memory type multi-processor
  - Hierarchical tree structure
  - Composed as matrix switch
- Advantage
  - High scalability
  - Flexibility



Multi-processor system

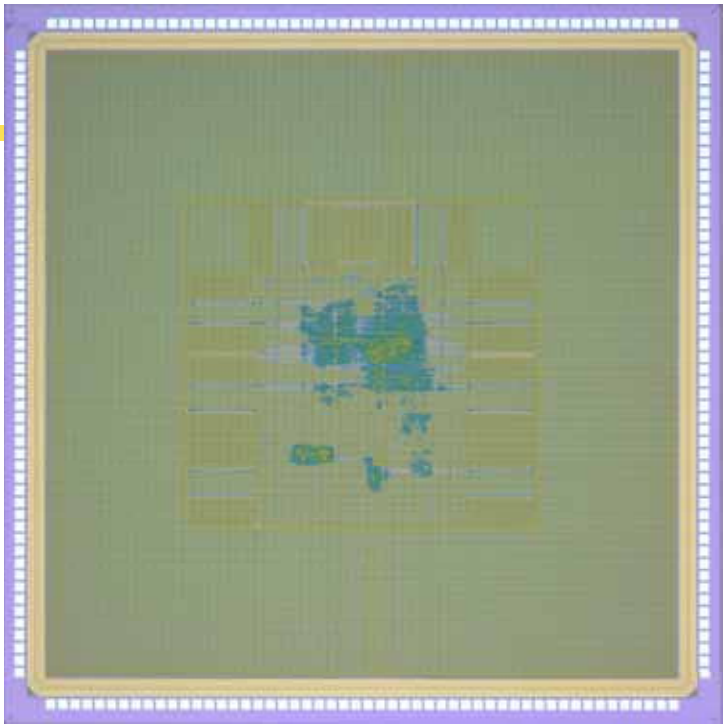
Performance of multi-processor

	Single (clocks)	Multi (clocks)	Ratio (multi/single)
1024-FFT	2,283,931	490,950	4.65 times
DFT	1,931,629	138,648	13.93 times

- Simulation by software simulator
  - Simulator is made by C++

LSI implementation

- LSI prototype
  - Processor element
  - Switch
- To achieve multi-processor
- This chip can operate at 33 MHz



•0.18um CMOS

•208 pins

•Die size: 6,166×6,166um

•37,528 gates

•Memory: IMEM 512words
DMEM 4Kwords
(1word = 32bit)