A 16-Bit, Low-Power Microsystem with Monolithic MEMS-LC Clocking

Robert M. Senger

Eric D. Marsman

Michael S. McCorquodale

University of Michigan

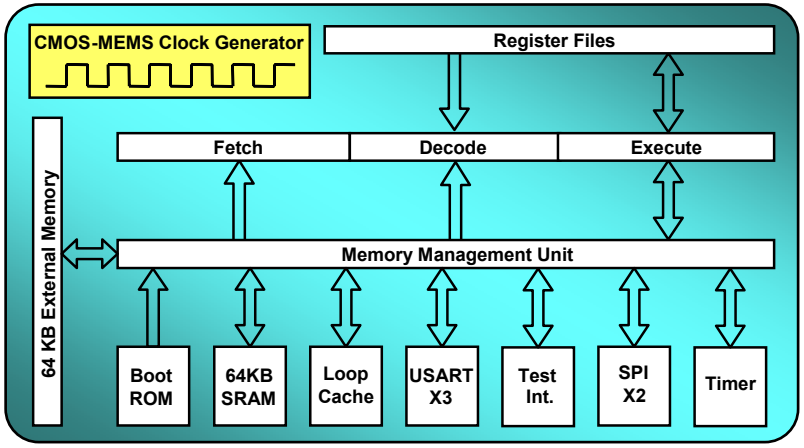
Richard B. Brown

University of Utah

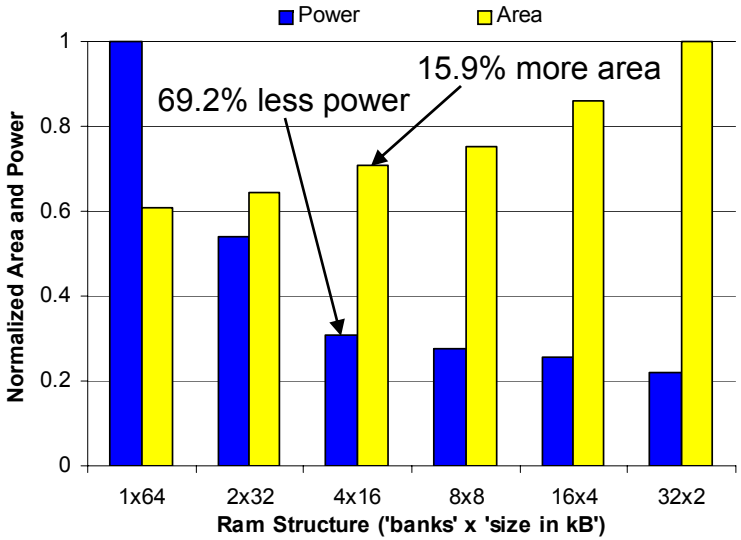
11th Asia and South Pacific Design Automation Conference
January 24 - 27, 2006 Yokohama, Japan

Microsystem Architecture

- 16/24-bit, 3-stage pipeline
- Load-Store architecture
- 77 instructions, 8 address modes
- Windowed registers
- Hardware support for one level of interrupts and subroutines
- 4x16KB banked memory architecture with external memory interface
- Peripheral interfaces
- 512B loop cache
- Register controlled clock interface
- Low latency, glitch-free dynamic frequency scaling



Microsystem architecture

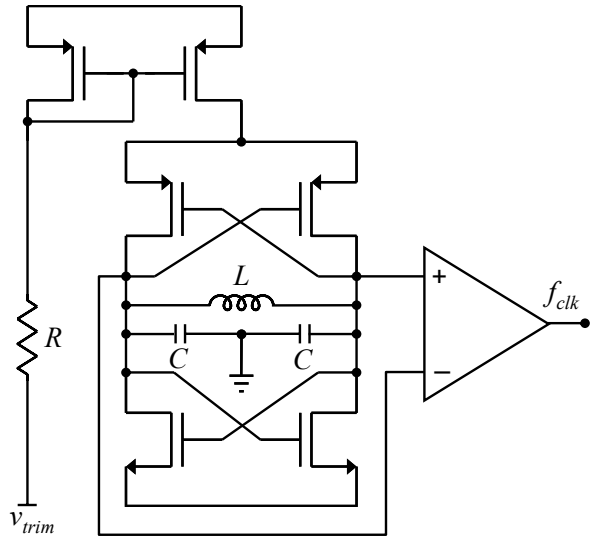


SRAM energy/area tradeoffs

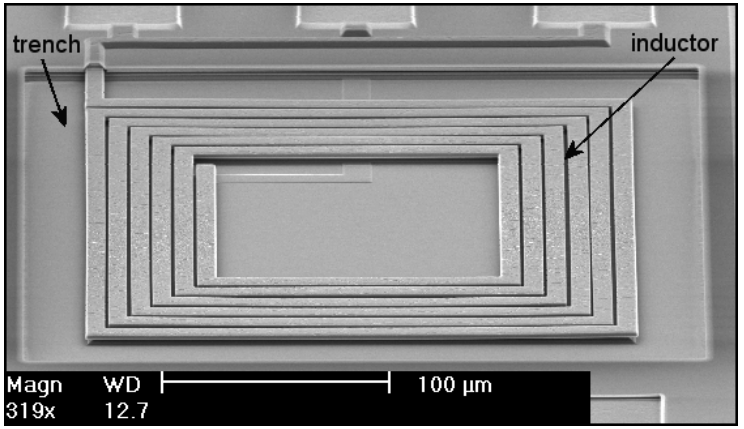
Monolithic Clock Generation

- **Complementary, cross coupled, negative-transconductance tank**
- **CMOS compatible suspended inductor**
  - Post processing etch using PAD cut
- **Frequency trimming via modulation of tail current v_{trim}**
- **High frequency accuracy so no external reference or DLL/PLL**

Metric/Parameter	*LC* Clock
Reference frequency	**1056MHz**
Frequency precision (no trim)	**±2%**
Trimmed frequency accuracy	**100ppm**
Worst case duty cycle	**48/52**
Worst case RMS period jitter	**<300ppm**
Temperature stability (-40 to 100C)	**±0.9%**
Power dissipation	**17.28mW**
Start-up latency (25C/125C)	**18ns/28ns**



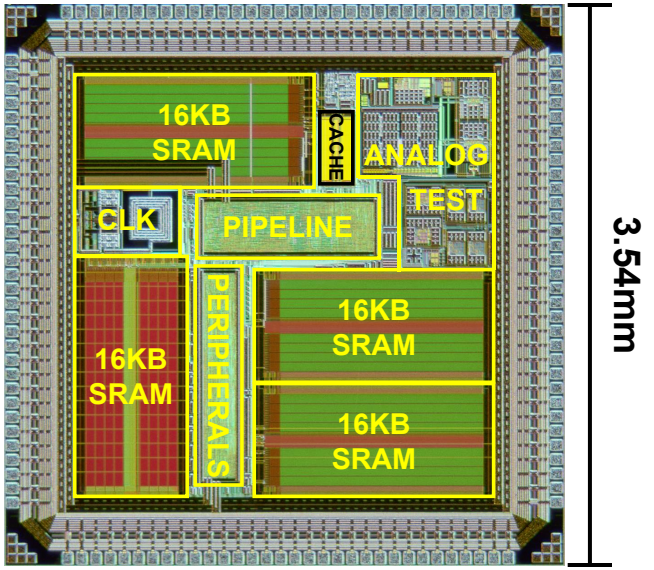
LC tank schematic

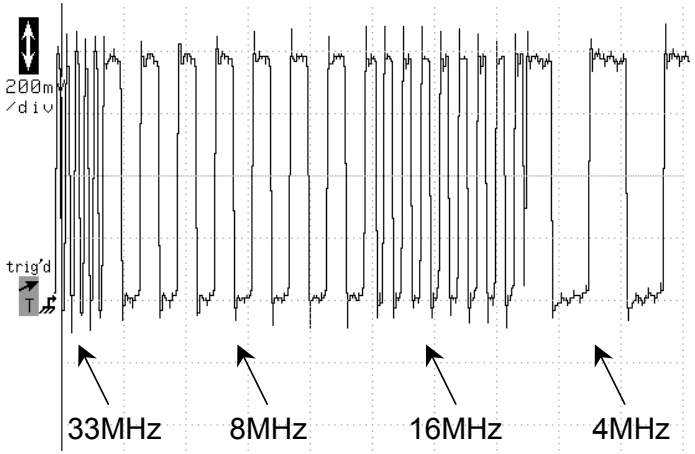


Suspended inductor

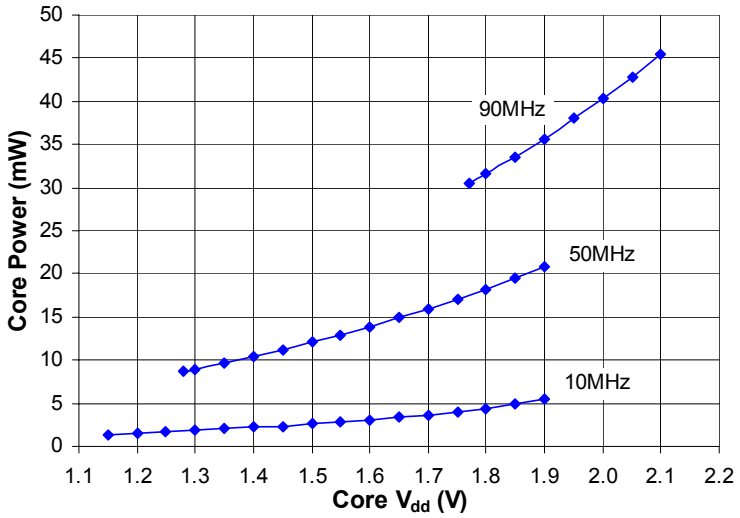
Microsystem Measured Results

- TSMC 0.18μm MM/RF bulk CMOS
- 3.5 million transistors
- 33.9mW core power @ 92MHz & 1.8V
- 1.4mW core power @ 10MHz & 1.1V
- 740μW sleep power @ 1.1V
- Static loop cache utilization provides 4 to 20% energy savings





Low latency (37.45ns), glitch-free dynamic clock frequency scaling



Measured power as V_{dd} is scaled for 10, 50, and 90MHz

Conclusion

- **Highly-functional, low-power microsystem for remote and bio-medical applications**
- **Dynamic frequency scaling**
  - 33.9mW @ 90MHz
  - 1.4mW @ 10MHz
  - 740μW in sleep mode
- **Monolithic clock reference decreases system size, cost, and power dissipation**
- **Power-aware compiler leverages custom ISA, loop cache, register windows**

	This Work	Berkeley SmartDust	TI MSP-430F21x1	National CP3000	AMD AM186ER	ARM922T
Maximum Frequency	92MHz	0.5MHz	16MHz	24MHz	50MHz	250MHz
Active Current	188μA / MHz	11.8μA / MHz (logic only)	200μA / MHz	500μA / MHz	3900μA / MHz	250μA / MHz
Power Supply	1.8V	1.0V	1.8 - 3.6V	2.5V	3.3V	1.2V
Program Memory	64kB SRAM	2.2kB SRAM	8kB Flash	256kB Flash	32kB SRAM	8kB SRAM (cache)
Data Memory		1kB SRAM	256b SRAM	10kB SRAM		8kB SRAM (cache)
Instruction / Data Width	16 / 16-bit	17 / 8-bit	16 / 16-bit	16 / 16-bit	16 / 16-bit	16 (Thumb) / 32-bit
Peripherals	Timer, USART, SPI, GPIO	Timer	Timer, UART	USB, CAN, USART, SPI, GPIO, Timer, Bluetooth	Timer, USART, UART	-