UCLA COMPUTER SCIENCE DEPARTMENT

A Robust Detailed Placement for Mixed-Size IC Designs

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Outline

- Review of Existing Works
- Robust Mixed-size Detailed Placement
- Experiment Results
- Conclusions and Future Work

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- Review of Existing Works
- Robust Mixed-size Detailed Placement
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Review of Existing Works

- Legalization of macros during global placement
  - Capo [Adya et al, ICCAD04]
  - mPG-MS [Cong and Yuan, ASPDAC03]
  - Dragon [Taghavi et al, ISPD05]
  - PolarBear [Cong et al, ICCAD05]
- Legalization of macros during detailed placement
  - Aplace [Kahng and Wang, ICCAD04]
  - BonnPlace [Vygen, DAC97]
  - FDP [Vorwerk et al, ICCAD04]
  - Fengshui [Khatkhate et al, ISPD04]
  - UPlace [Yao et al, ISPD05]
  - FastPlace [Viswanathan et al, ASPDAC06]

Review of Existing Works

- Limitations of most legalizations in second category
  - Some may not produce a legal solution
  - May cause significant perturbation to global placement

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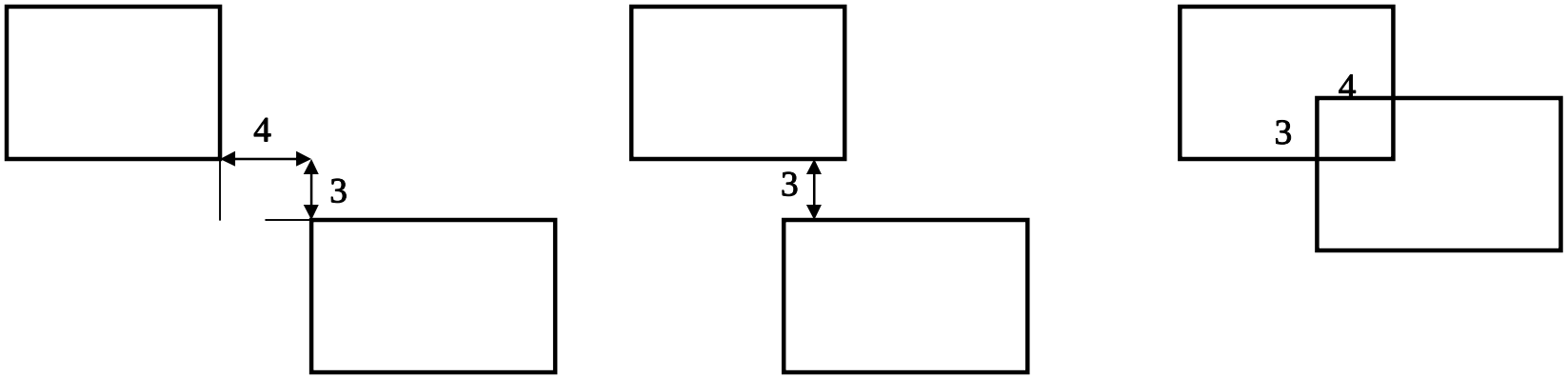
Algorithm Overview

- Constraint Graph Based Macro Legalization
- Enhanced Standard Cell Legalization
- Sweeping Window Based Refinement

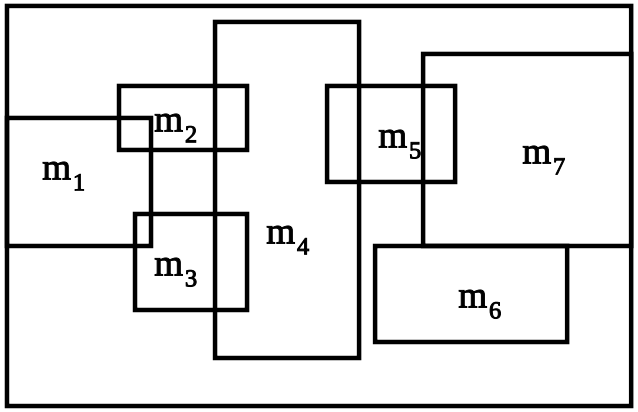
Phase I. Constraint Graph based Macro Legalization -- Constraint Graph Generation



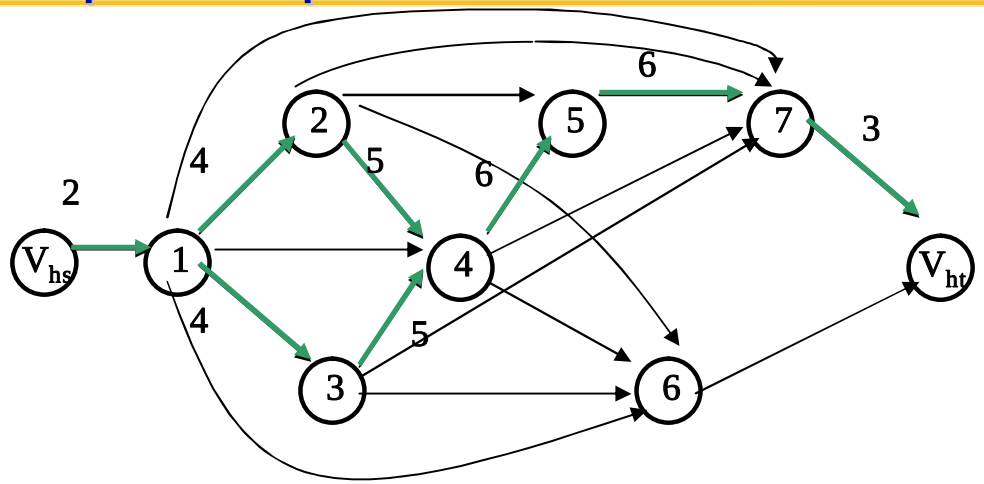
horizontal vertical vertical

- Model pairwise non-overlapping constraints with constraint edges
- Constraint edge direction to the one that incurs the least amount of overlap

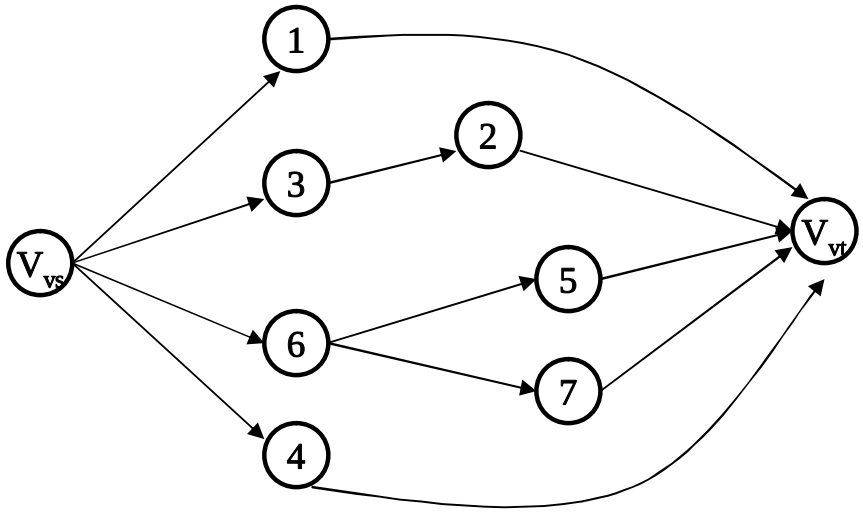
Phase I. Constraint Graph based Macro Legalization -- Constraint Graph Example



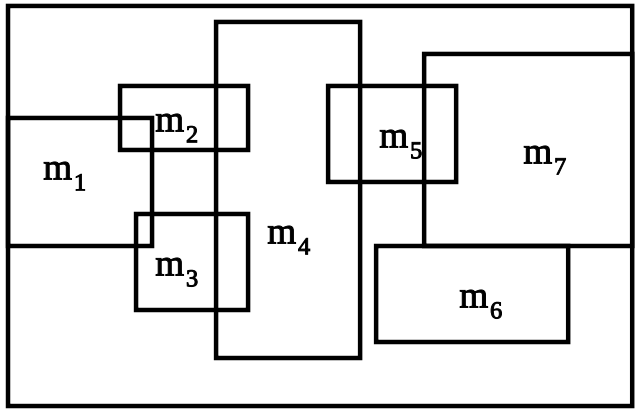
Chip Dimension : 25 x 10

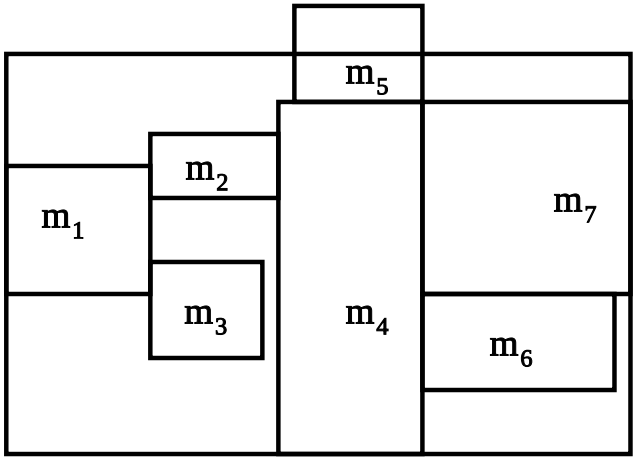


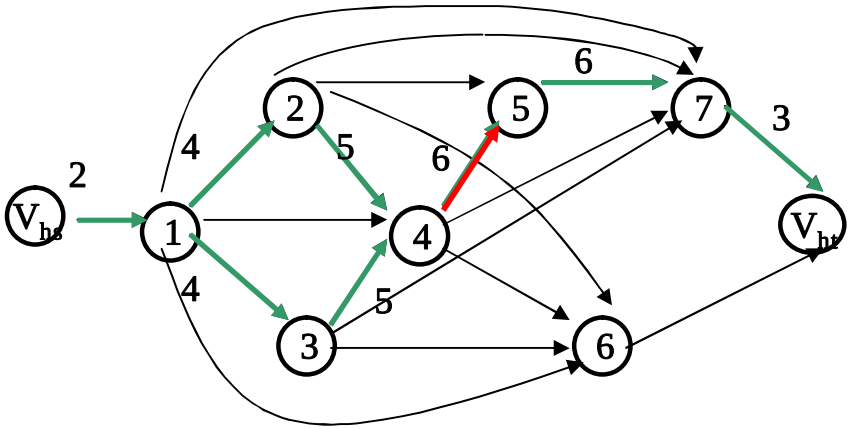
Macro	Height	Width
m1	4	4
m2	2	4
m3	3	4
m4	9	6
m5	4	6
m6	3	6
m7	6	6



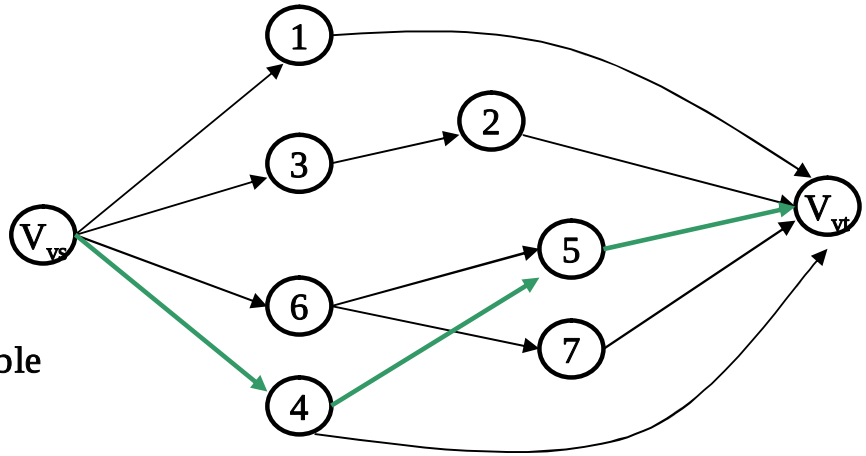
Phase I. Constraint Graph based Macro Legalization -- Constraint Graph Example



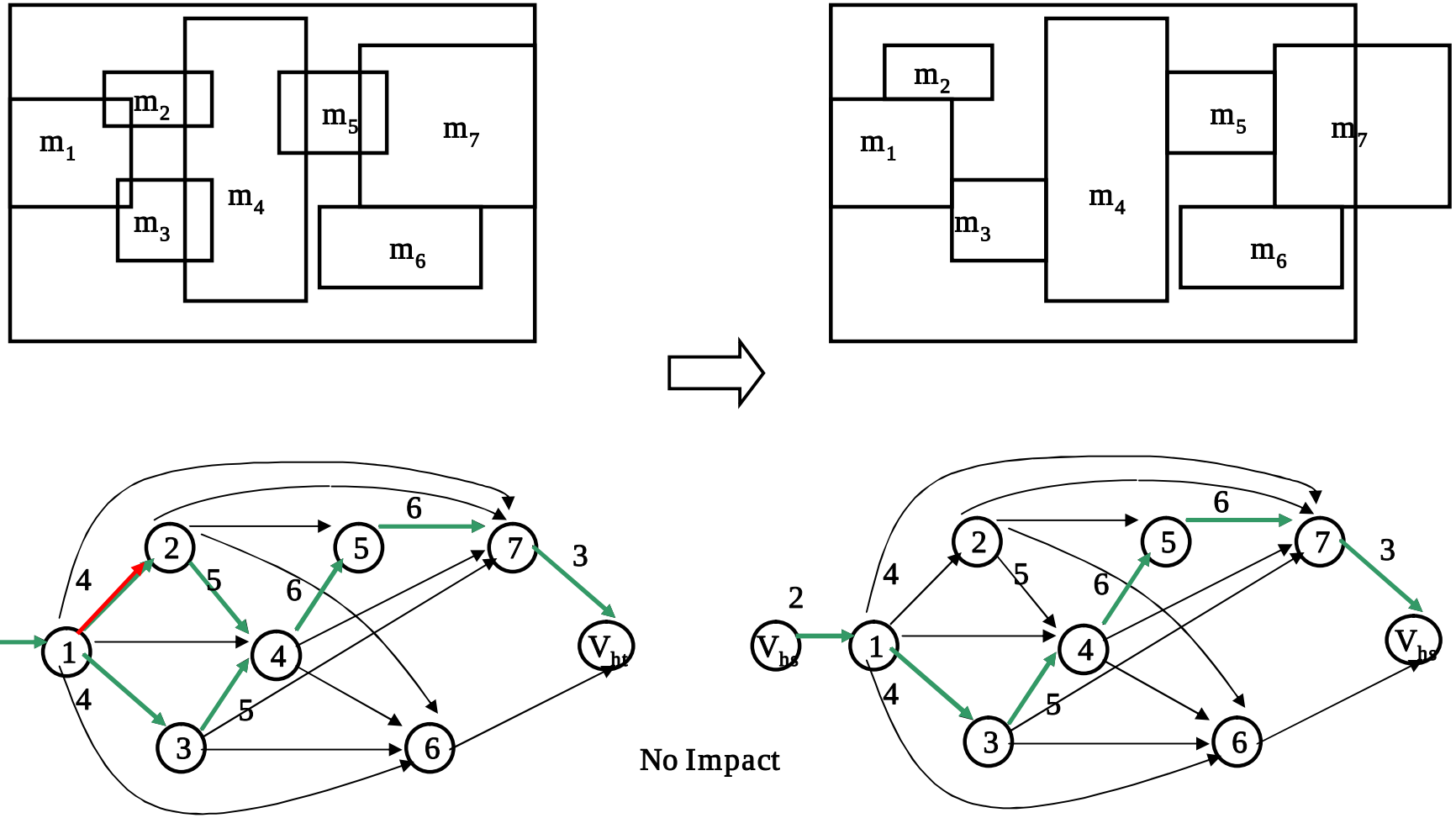




Infeasible



Phase I. Constraint Graph based Macro Legalization -- Constraint Graph Example

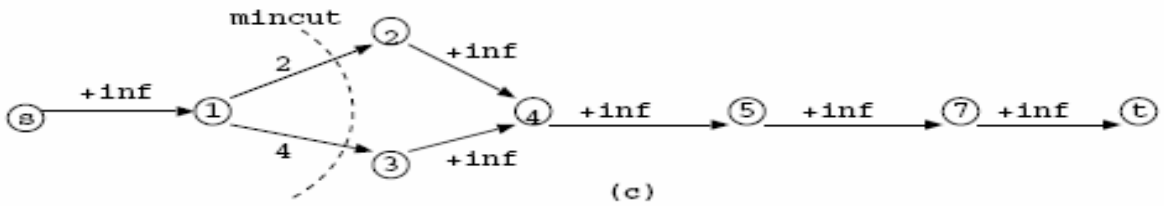


Phase I. Constraint Graph base Macro Legalization -- Constraint Graph Adjustment

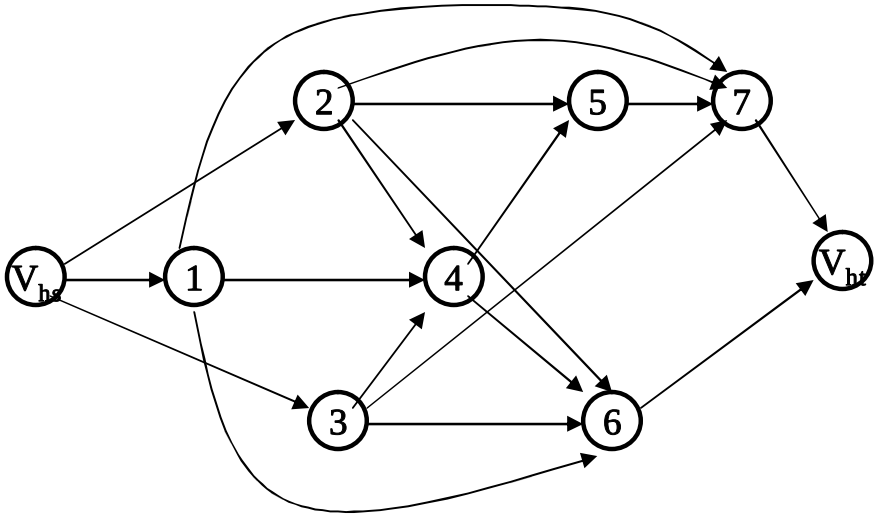
- Extract the epsilon-network of the constraint graph
  - Subgraph made up of critical edges
- Search for a min-cut on the epsilon-network
  - Used in logic synthesis for timing [Singh 92, Xu 00, Ph.D Thesis]
- Heuristic edge capacity assigned as

$$c(e_{ij}) = \begin{cases} +\infty \text{ if orthogonal infeasible} \\ \max(y_i - R(v_j) + \frac{h_i + h_j}{2}, 0) + \max(L(v_i) + \frac{h_i + h_j}{2} - y_j, 0) \end{cases}$$

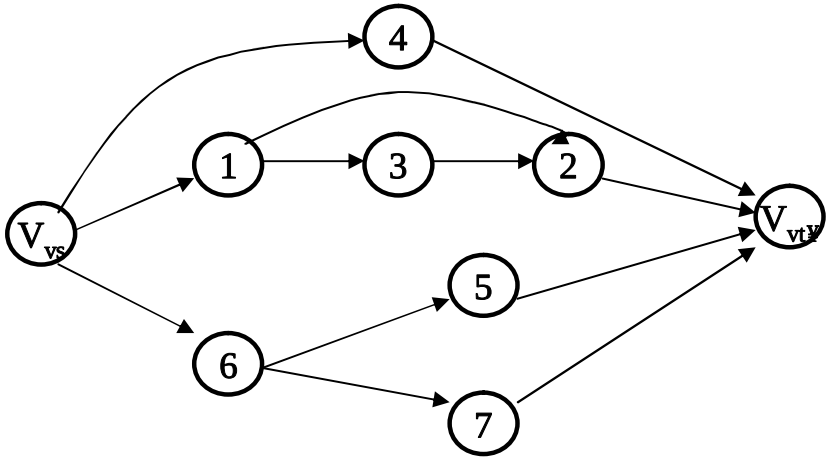
- Corresponding epsilon network for the example



Phase I. Constraint Graph base Macro Legalization – Final Constraint Graph



Final Horizontal Constraint Graph



Final Vertical Constraint Graph

Phase I. Constraint Graph base Macro Legalization -- Macro Coordinate Assignment

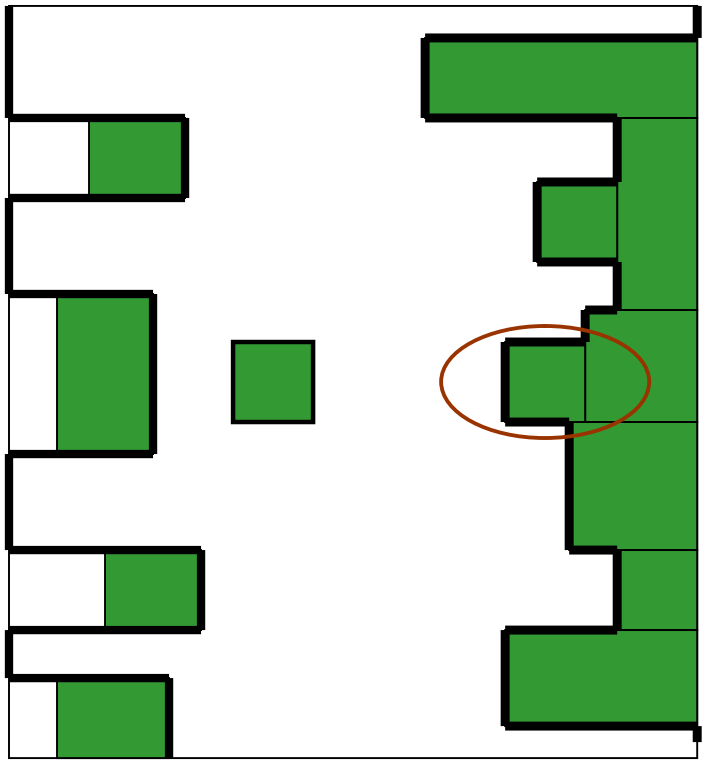
- Determine the location of macros by minimizing total perturbation from global placement
- Linear constraints based on the edges derived in the constraint graph
  - Similar formulation in [Vygen, DATE98, Tang et al, ASPDAC 2005]

$$\min \sum_{i=1}^{n} \left| x_i' - x_i \right| + \sum_{i=1}^{n} \left| y_i' - y_i \right|$$

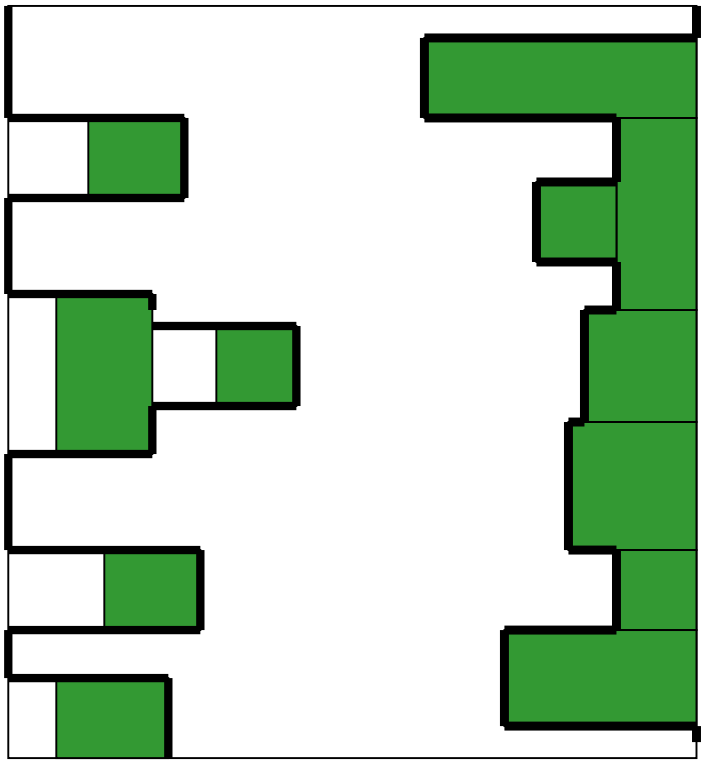
$$\text{s.t.} \begin{cases} x_{i2}' - x_{i1}' \geq \dfrac{w_{i1} + w_{i2}}{2} & \text{For } i^{\text{th}} \text{ horizontal constraint edge} \\ y_{i2}' - y_{i1}' \geq \dfrac{h_{i1} + h_{i2}}{2} & \text{For } i^{\text{th}} \text{ vertical constraint edge} \end{cases}$$

- LP formulation can be enhanced to consider weights, WL, etc

Phase II. Enhanced Cell Legalization



Front end Back end

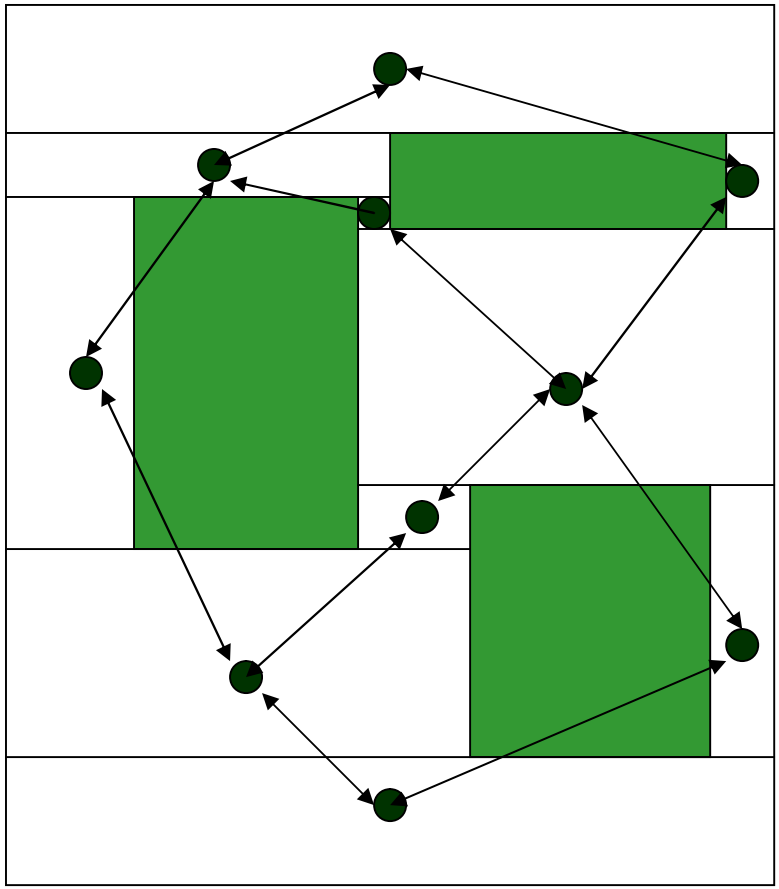


Front end Back end

Enhanced greedy legalization [Hill, US Patent 02, Khatkhate ISPD04]

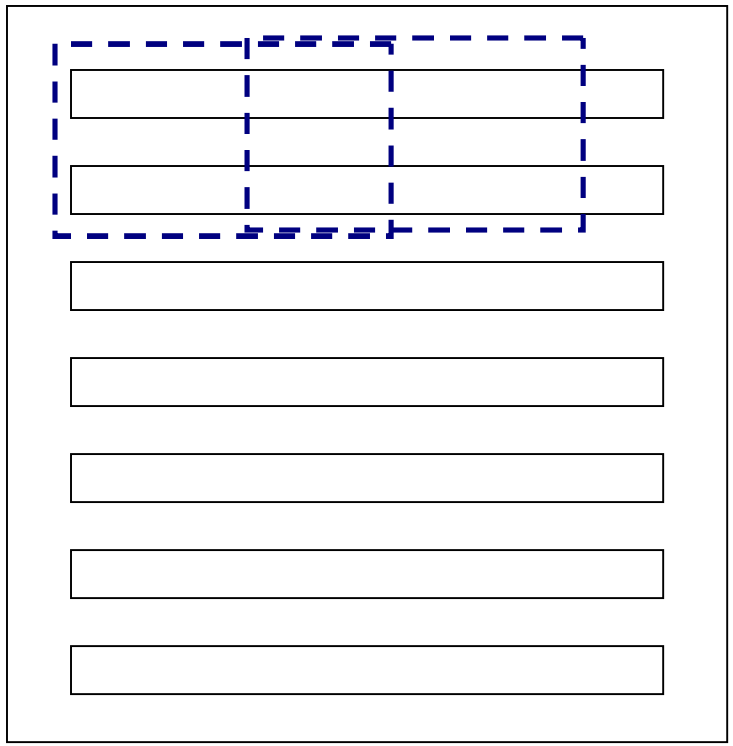
Macros are only allowed to move horizontally during cell legalization

Phase II. Enhanced Cell Legalization



- Network flow based cell evening as post processing
  - [Vygen DATE98]
- Occurrence depends on the global placement
  - 5 out of 18 examples tested

Phase III. Greedy Cell Swapping



- Optimization window spanning multiple rows
- Enumerate all cell permutations within each window
- Accept the configuration giving the shortest wirelength
- Slide the window by half window width once done

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ICCAD-MS 2004

circuit	#cell	#macro	#pad	#net	#row	utilization
ibm01	12507	246	246	14111	144	80%
ibm02	19343	271	259	19584	203	80%
ibm03	22854	290	283	27401	219	80%
ibm04	27221	295	287	31970	213	80%
ibm05	28147	0	1201	28446	148	80%
ibm06	32333	178	166	34826	204	80%
ibm07	45640	291	287	48117	240	80%
ibm08	51024	301	286	50513	256	80%
ibm09	53111	253	285	60902	293	80%
ibm10	68686	786	744	75196	482	80%
ibm11	70153	373	406	81454	322	80%
ibm12	70440	651	637	77240	425	80%
ibm13	83710	424	490	99666	350	80%
ibm14	147089	614	517	152772	375	80%
ibm15	161188	393	383	186608	422	80%
ibm16	182981	458	504	190048	507	80%
ibm17	184753	760	743	189581	454	80%
ibm18	210342	285	272	201920	406	80%

Detailed Placement Result Comparison

-- Global Placements by mPL

circuit	GPWL	Aplace		Fengshui		XDP	
		FWL	RT(s)	FWL	RT(s)	FWL	RT(s)
ibm01	2.10E+06	N/A		2.23E+06	13	2.18E+06	37
ibm02	4.54E+06	5.12E+06	70	5.09E+06	22	4.74E+06	70
ibm03	6.94E+06	N/A		Overlap		6.65E+06	54
ibm04	7.37E+06	7.84E+06	98	N/A		7.54E+06	75
ibm05	9.36E+06	9.79E+06	80	9.80E+06	38	9.74E+06	66
ibm06	6.39E+06	N/A		N/A		5.97E+06	64
ibm07	1.00E+07	1.04E+07	150	Overlap		1.01E+07	120
ibm08	1.25E+07	1.25E+07	192	1.25E+07	68	1.19E+07	157
ibm09	1.37E+07	1.32E+07	233	1.38E+07	81	1.27E+07	146
ibm10	3.01E+07	N/A		Overlap	105	2.95E+07	321
ibm11	1.76E+07	N/A		1.91E+07	131	1.82E+07	206
ibm12	3.67E+07	N/A		N/A		3.44E+07	330
ibm13	2.26E+07	N/A		2.40E+07	145	2.36E+07	242
ibm14	3.62E+07	N/A		3.65E+07	540	3.53E+07	443
ibm15	5.57E+07	5.27E+07	1230	5.24E+07	420	5.01E+07	552
ibm16	5.73E+07	5.55E+07	1425	5.59E+07	447	5.31E+07	671
ibm17	6.67E+07	6.70E+07	1103	6.71E+07	493	6.53E+07	923
ibm18	4.41E+07	4.41E+07	1472	4.42E+07	550	4.31E+07	724
Avg.		1.03	1.52	1.03	0.60	1.00	1.00

- Best performance among the three placers compared

Detailed Placement Result Comparison

-- Global Placements by APlace

circuit	GPWL	Aplace		Fengshui		XDP	
		FWL	RT(s)	FWL	RT(s)	FWL	RT(s)
ibm01	2.16E+06	2.14E+06	24	Overlap		2.08E+06	24
ibm02	4.84E+06	4.65E+06	50	N/A		4.65E+06	53
ibm03	6.95E+06	6.71E+06	58	N/A		6.73E+06	52
ibm04	7.57E+06	7.57E+06	62	N/A		7.48E+06	64
ibm05	9.83E+06	9.69E+06	54	9.84E+06	59	9.59E+06	72
ibm06	6.38E+06	6.02E+06	76	Overlap		6.11E+06	73
ibm07	1.04E+07	1.00E+07	111	Overlap		9.94E+06	119
ibm08	1.29E+07	1.25E+07	131	Overlap		1.24E+07	152
ibm09	1.26E+07	1.21E+07	154	Overlap		1.21E+07	140
ibm10	3.11E+07	2.88E+07	296	Overlap		2.90E+07	324
ibm11	1.96E+07	1.87E+07	215	Overlap		1.87E+07	199
ibm12	3.50E+07	3.34E+07	279	Overlap		3.38E+07	260
ibm13	2.34E+07	2.28E+07	279	Overlap		2.30E+07	239
ibm14	3.74E+07	3.59E+07	445	Overlap		3.55E+07	413
ibm15	4.88E+07	4.68E+07	648	Overlap		4.67E+07	565
ibm16	5.83E+07	5.45E+07	798	Overlap		5.43E+07	666
ibm17	6.69E+07	6.57E+07	735	Overlap		6.53E+07	667
ibm18	4.48E+07	4.20E+07	706	Overlap		4.17E+07	672
Avg.		1.00	1.00	1.03	0.73	1.00	0.98

- Comparable performance as the native DP of Aplace

Impact of LP for Macro Coordinate Assignment

circuit	Greedy		LP	
	FWL	RT(s)	FWL	RT(s)
ibm01	2.22E+06	30	2.18E+07	37
ibm02	5.00E+06	87	4.77E+07	70
ibm03	6.67E+06	58	6.68E+07	54
ibm04	7.52E+06	66	7.59E+07	75
ibm05	9.76E+06	66	9.76E+07	66
ibm06	6.00E+06	66	6.06E+07	64
ibm07	1.01E+07	123	1.02E+07	120
ibm08	1.21E+07	152	1.19E+07	157
ibm09	1.29E+07	145	1.28E+07	146
ibm10	2.91E+07	340	2.90E+07	321
ibm11	1.82E+07	195	1.80E+07	206
ibm12	3.52E+07	380	3.48E+07	330
ibm13	2.35E+07	242	2.34E+07	242
ibm14	3.55E+07	452	3.54E+07	443
ibm15	5.04E+07	650	5.03E+07	552
ibm16	5.32E+07	665	5.31E+07	671
ibm17	6.52E+07	948	6.52E+07	923
ibm18	4.32E+07	715	4.31E+07	724
Avg.	1.01	1.02	1.00	1.00

- LP helps to reduce the final WL by 1%

Impact of Movable Macros

circuit	Fixed		Movable	
	FWL	RT(s)	FWL	RT(s)
ibm01	2.25E+06	37	2.18E+07	37
ibm02	4.83E+06	62	4.77E+07	70
ibm03	6.93E+06	63	6.68E+07	54
ibm04	7.97E+06	67	7.59E+07	75
ibm05	9.75E+06	68	9.76E+07	66
ibm06	6.21E+06	66	6.06E+07	64
ibm07	1.09E+07	138	1.02E+07	120
ibm08	1.18E+07	117	1.19E+07	157
ibm09	1.31E+07	123	1.28E+07	146
ibm10	3.10E+07	236	2.90E+07	321
ibm11	1.90E+07	175	1.80E+07	206
ibm12	3.90E+07	320	3.48E+07	330
ibm13	2.53E+07	244	2.34E+07	242
ibm14	3.62E+07	354	3.54E+07	443
ibm15	5.13E+07	490	5.03E+07	552
ibm16	5.34E+07	466	5.31E+07	671
ibm17	6.65E+07	746	6.52E+07	923
ibm18	4.45E+07	635	4.31E+07	724
Avg.	1.04	0.89	1.00	1.00

- Allowing macros to move helps to reduce final WL by 4%

Impact of Backend Contour

circuit	w/o backend		w backend	
	FWL	RT(s)	FWL	RT(s)
ibm01	N/A		2.18E+07	37
ibm02	N/A		4.77E+07	70
ibm03	N/A		6.68E+07	54
ibm04	N/A		7.59E+07	75
ibm05	9.76E+07	67	9.76E+07	66
ibm06	6.06E+07	65	6.06E+07	64
ibm07	N/A		1.02E+07	120
ibm08	N/A		1.19E+07	157
ibm09	N/A		1.28E+07	146
ibm10	N/A		2.90E+07	321
ibm11	1.80E+07	205	1.80E+07	206
ibm12	N/A		3.48E+07	330
ibm13	N/A		2.34E+07	242
ibm14	3.54E+07	445	3.54E+07	443
ibm15	5.03E+07	5.65E+02	5.03E+07	552
ibm16	5.31E+07	674	5.31E+07	671
ibm17	6.52E+07	943	6.52E+07	923
ibm18	4.31E+07	943	4.31E+07	724

- Having the backend contour significantly enhances the robustness

Outline

- Motivation and Existing Work
- Robust Mixed-size Detailed Placement
- Experiment Results
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Conclusions and Future Work

- A Robust Mixed-size Detailed Placement
  - Constraint graph based macro legalization
  - LP based macro coordinate assignment
  - Enhanced standard cell legalization
  - Best for mPL's global placement
  - Comparable to Aplace on its global placement
- Extension to Other Constraints
  - Both fixed and movable macros
  - Timing, routability, etc

Acknowledgements

- Thanks to Prof. Andrew Kahng for providing APlace 2.0
- Thanks to Prof. Patrick Madden for providing Fengshui 5.0

The End

Thank You!