ASP-DAC 2006

Electrothermal Engineering in the Nanometer Era: From Devices and Interconnects to Circuits and Systems

Kaustav Banerjee, Sheng-Chih Lin and Navin Srivastava

University of California, Santa Barbara

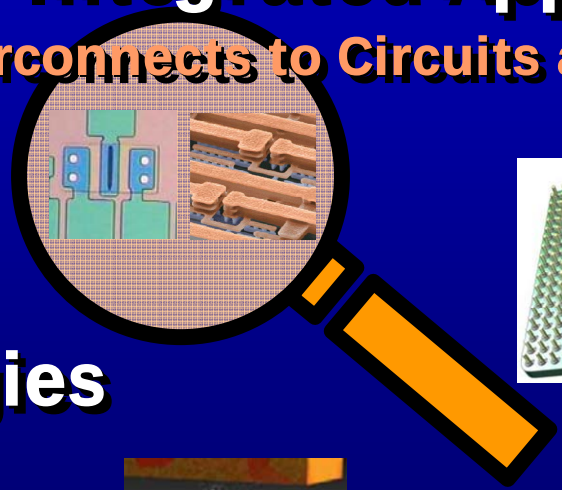
Outline

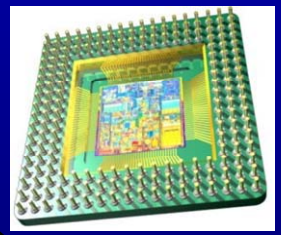
What is Electrothermal Engineering?

Micro-scale vs. Macro-scale

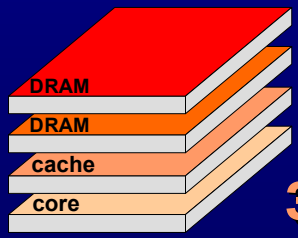
Temperature-Aware Integrated Approach

From Devices and Interconnects to Circuits and Systems

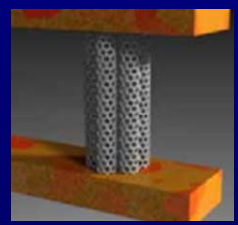




Emerging Technologies



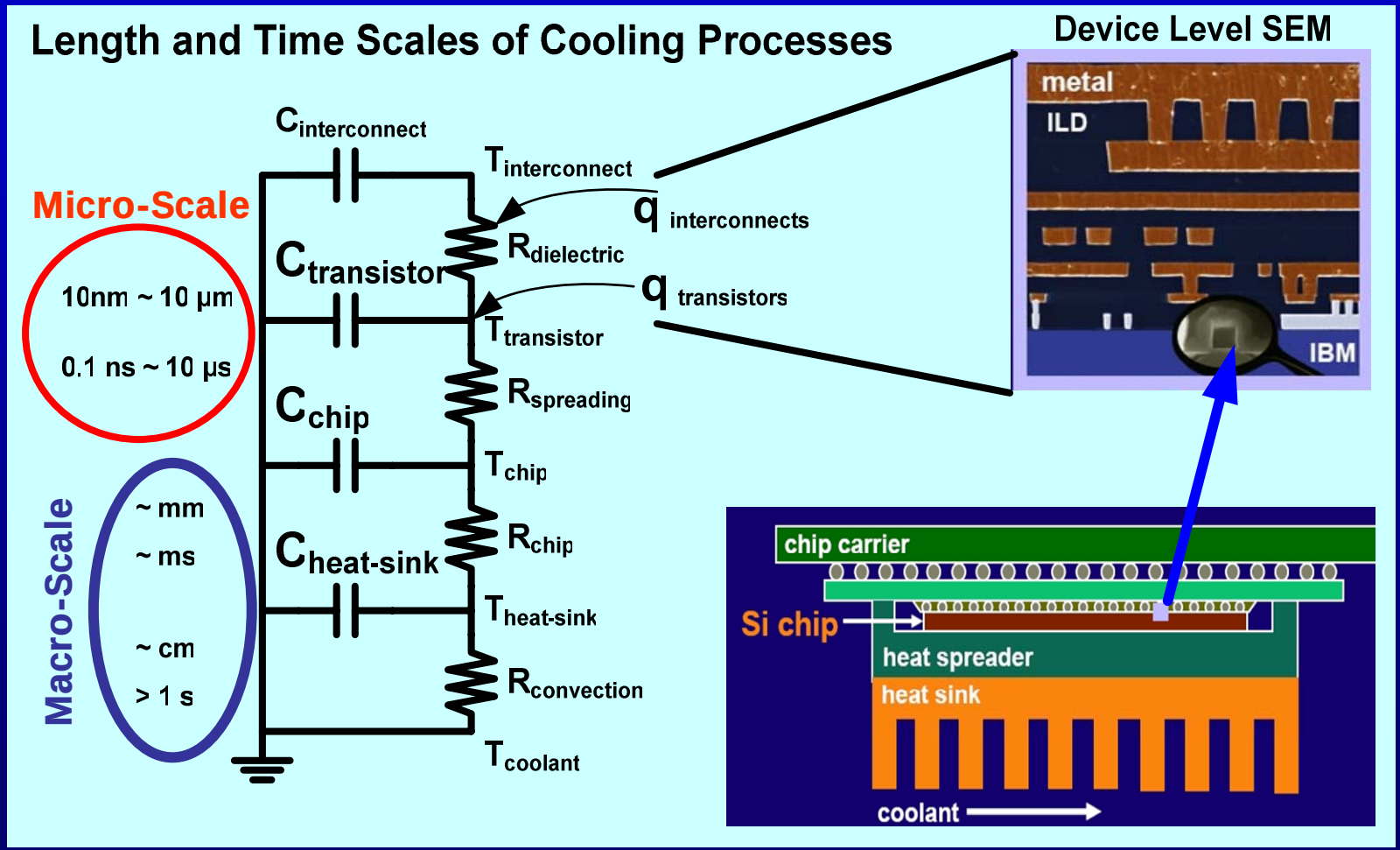
3-D IC Technology



Hybrid CNT-Cu Technology

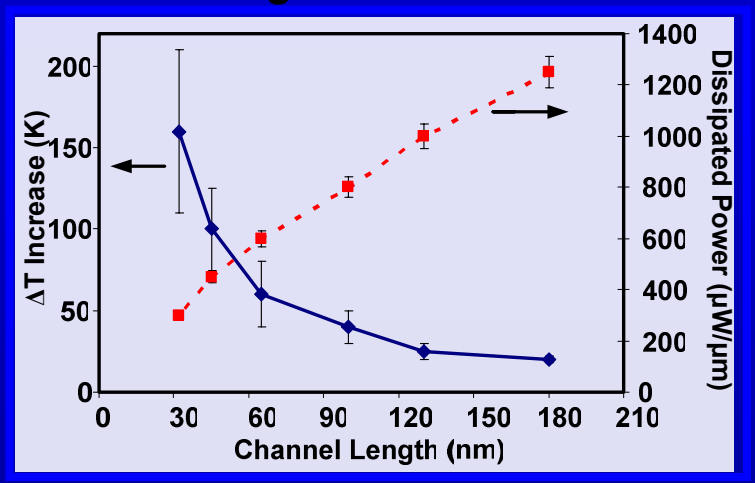
Micro-Scale vs. Macro-Scale

Global View of IC Heat Transfer….



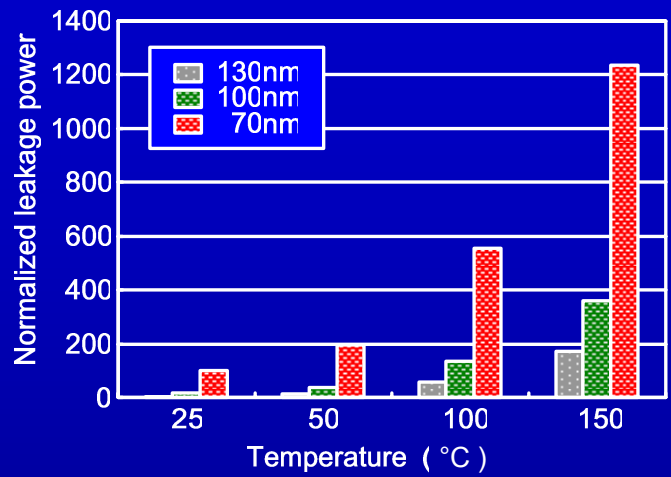
Device

Self-Heating increases……



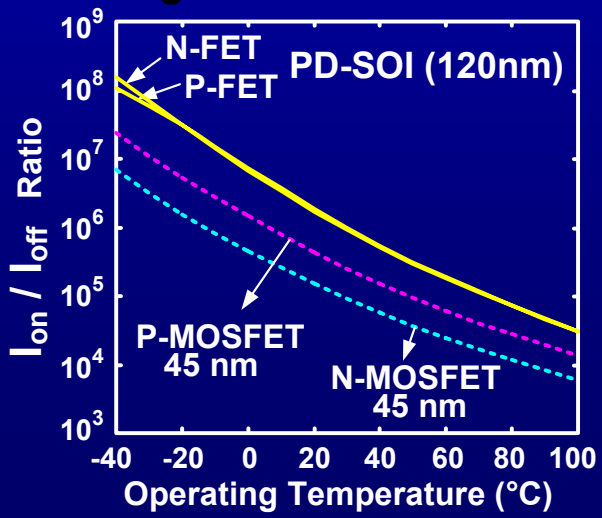
Pop et al. IEDM 2001

Leakage increases……



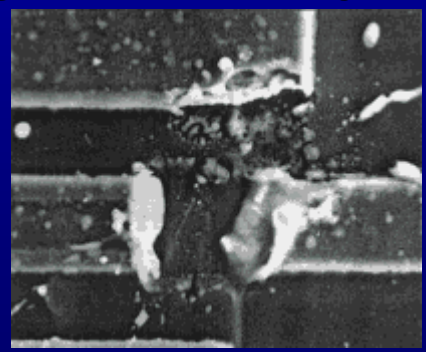
Banerjee et al. IEDM 2003

Degrades Performance……



Lin et al. IEDM 2005

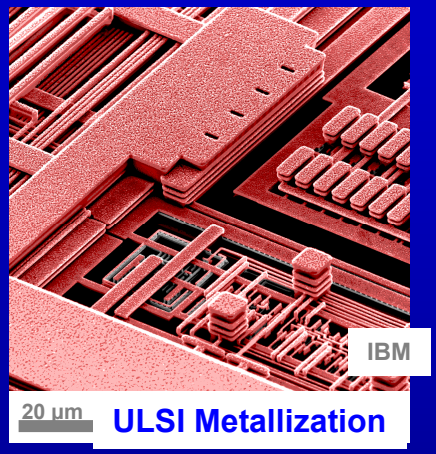
Degrades Reliability……



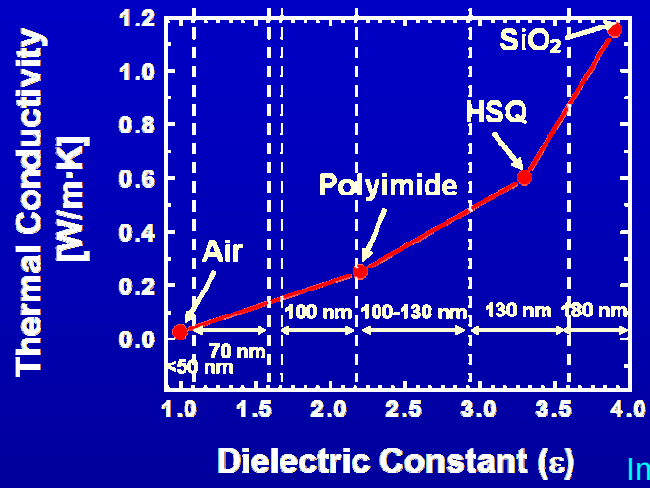
ESD Failure (Texas Instruments)

Interconnect

Number of metal layers increases....
Current density increases....

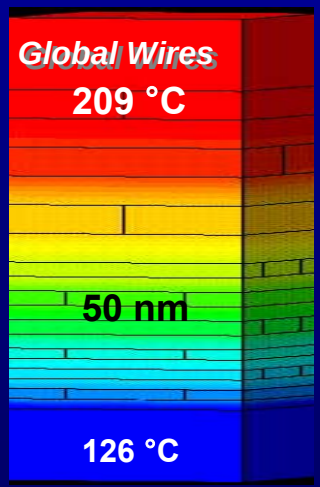


Low-k dielectrics increase self-heating



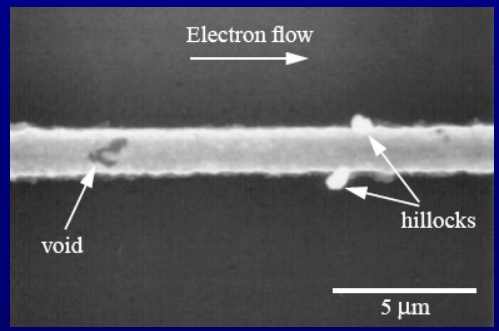
Im and Banerjee, IEDM 2000

Back-end thermal Profile!!



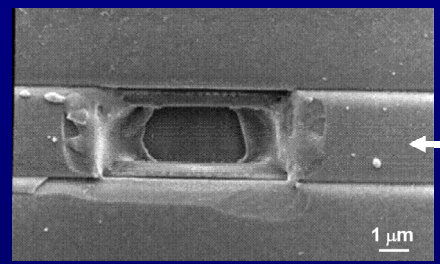
Im and Banerjee, IEDM 2000

Electromigration failure



Ryu et al. IRPS 1997

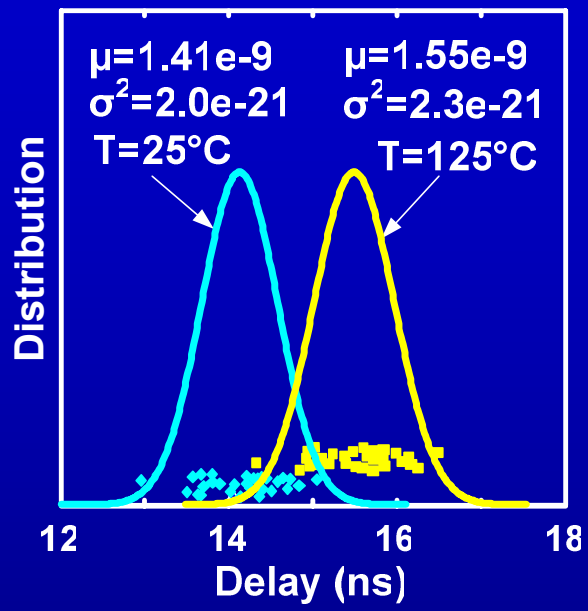
ESD failure



Banerjee et al. IRPS 2000

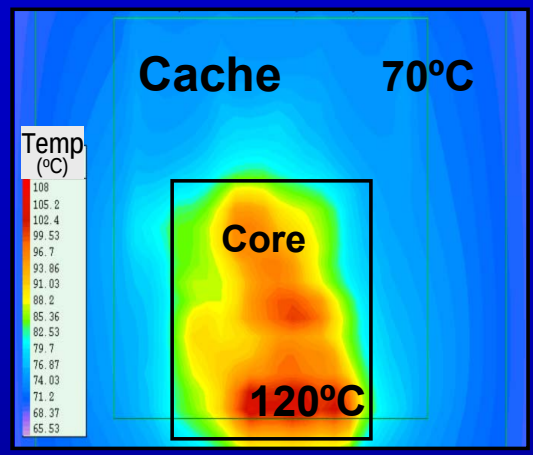
Circuit

Increased delay and variance….



Lin et al. IEDM 2005

Chip temperatures are non-uniform…



Courtesy of S. Borkar, Intel

- **Reliability**
- **Leakage and yield estimation**
- **Power / performance optimization**

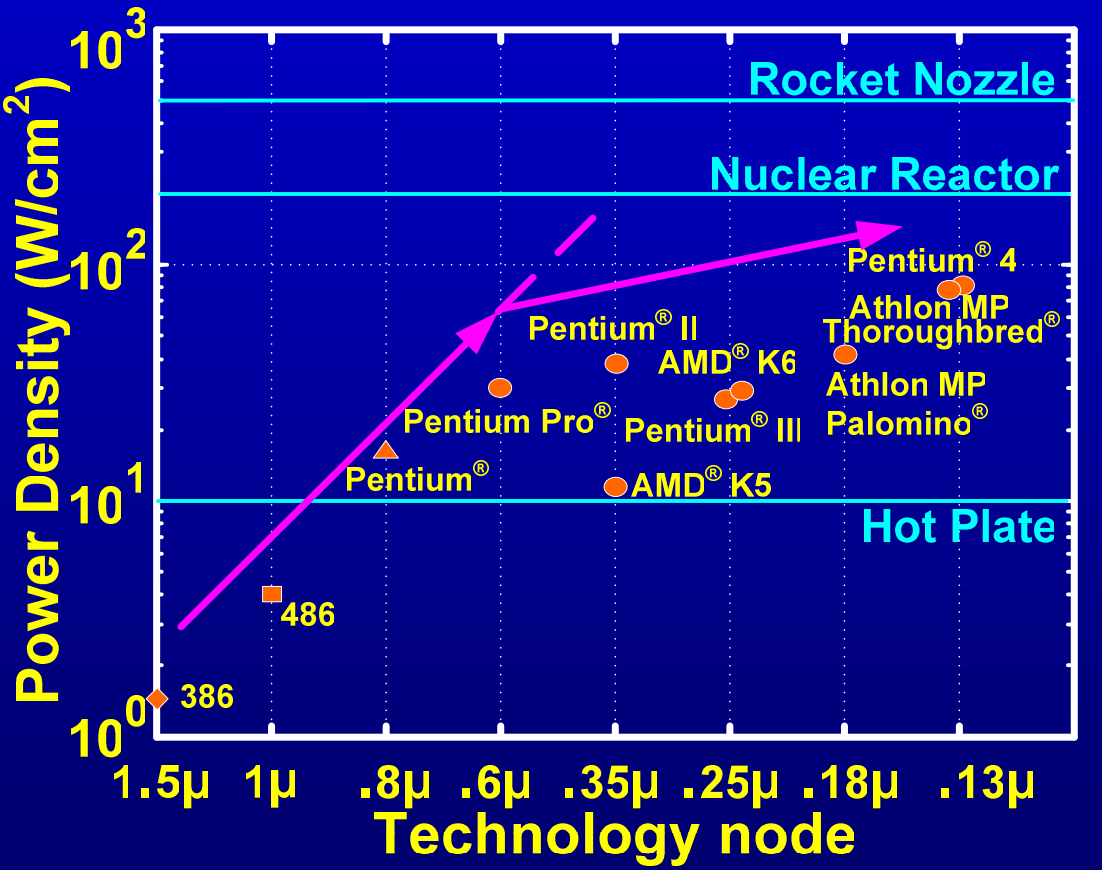
Zhang et al. ISLPED 2004
Lin et al. ICCD 2005

- **Wire delay and clock skew**
- **Buffer insertion**
- **Voltage drop**

Ajami et al., TCAD 2005, JAICSP 2005

System

Power density increases……



source : Intel, AMD

System

Impact of higher power dissipation and density (hot-spots) on system

- **System Performance and Stability**
  - degrades performance
  - Heat-induced failure and instability

M. Miller, AMD

- **Product Lifetime and Reliability**
  - Most reliability mechanisms are highly temperature sensitive

- **Operating Cost**
  - More complex cooling solutions

Electrothermal Engineering

Temperature awareness at every level…
Integrated approach…

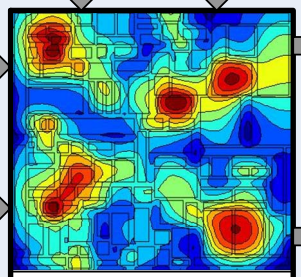
Fourier's Law – Heat Transfer
Microstructure Heat Transfer

Active Power
Device
Interconnect

Leakage Power
Device

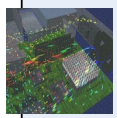
Layout geometry

Packaging
Cooling

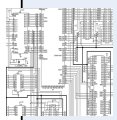


Full chip power dissipation and temperature profile estimation

System level
- Packaging / Cooling solutions
- System power dissipation
- System performance



Circuit level
- Timing
- Placement / Routing
- Buffer insertion

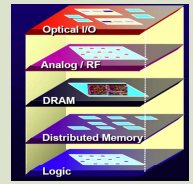


Device / Interconnect level
- Self-Heating
- Leakage mechanisms
- Reliability (EM, ESD)

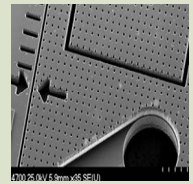
Temperature-Aware Design

Wider implications for emerging technology

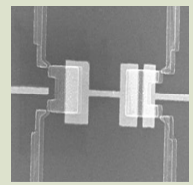
3D ICs



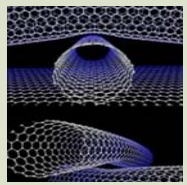
MEMS



SET

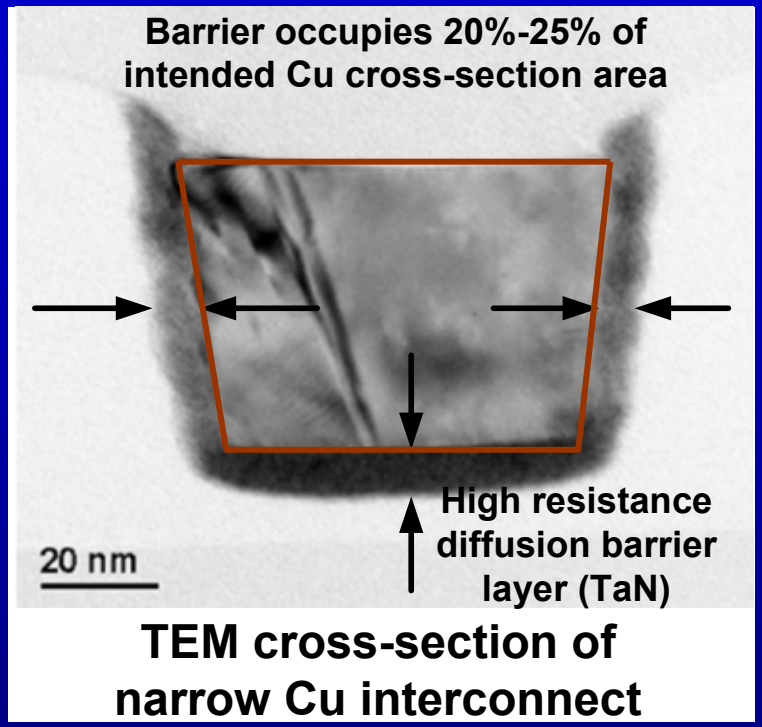


CNT

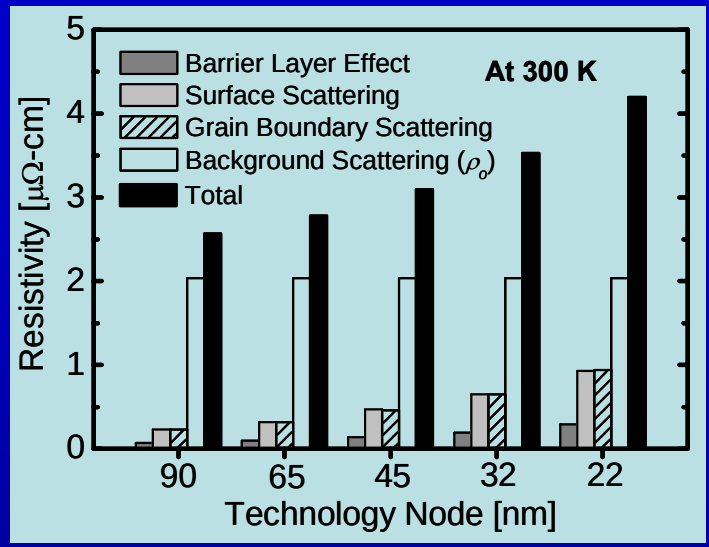


Interconnect Scaling Effects

Size effect on wire resistivity……



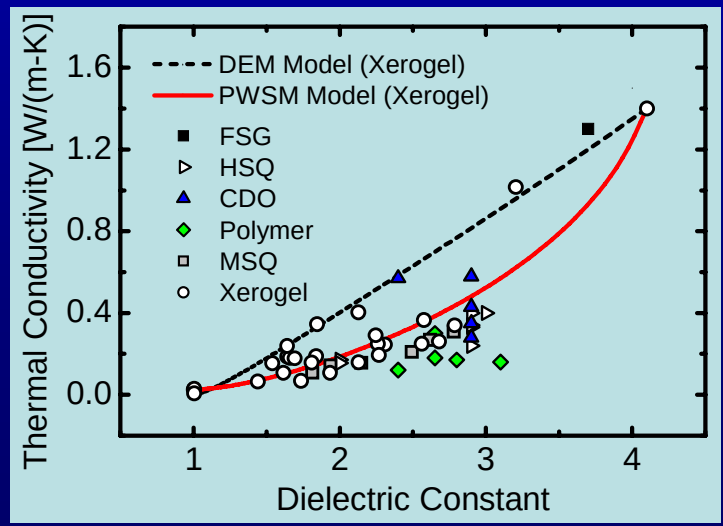
TEM cross-section of narrow Cu interconnect



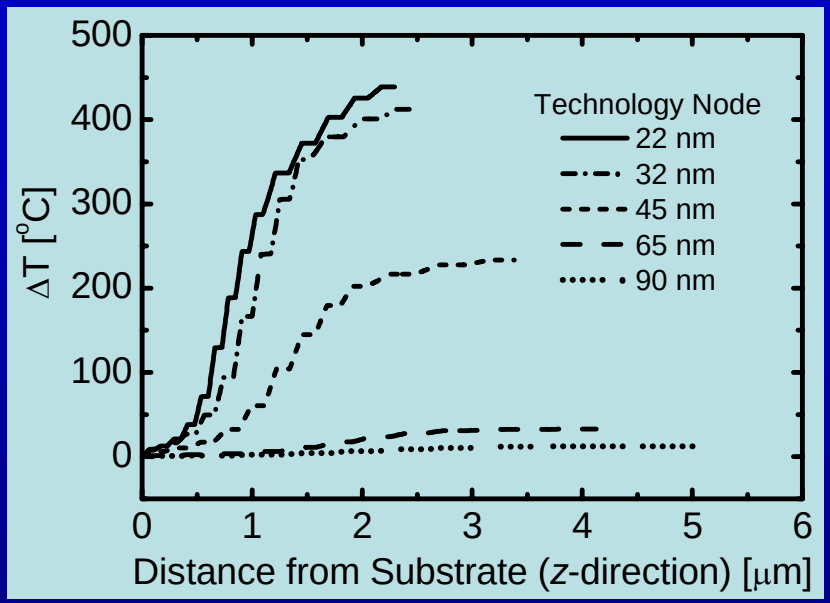
Im et al., IEEE TED, Dec. 2005

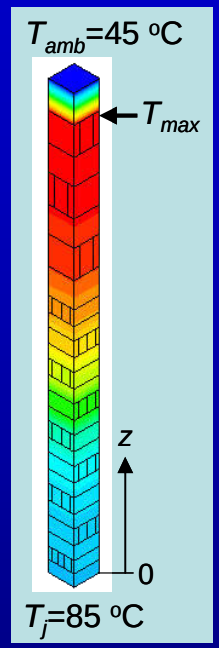
Bruggemann Effective Medium Theory: relates dielectric constant to porosity

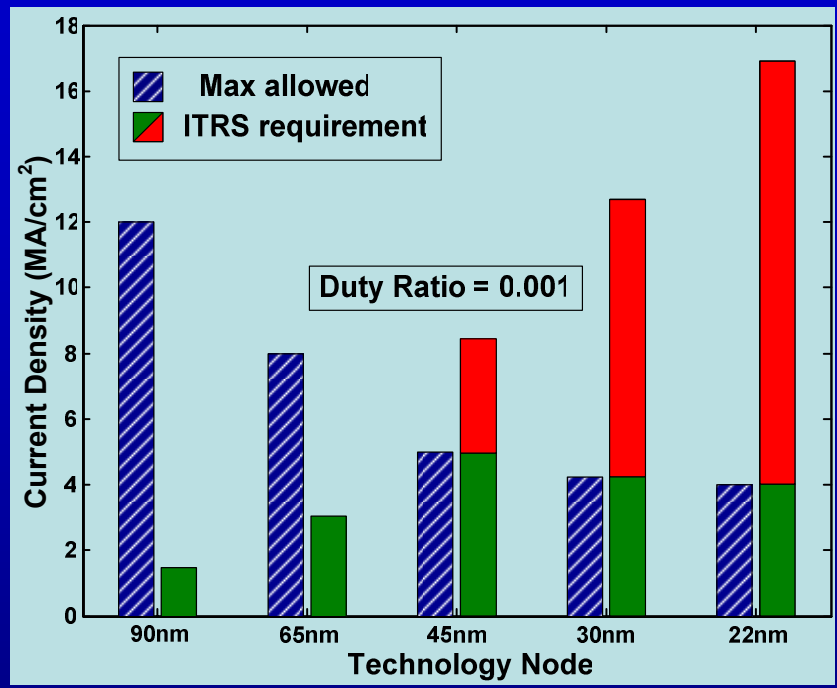
DEM or PWSM Models: relate thermal conductivity to porosity



Back-end Thermal Issues





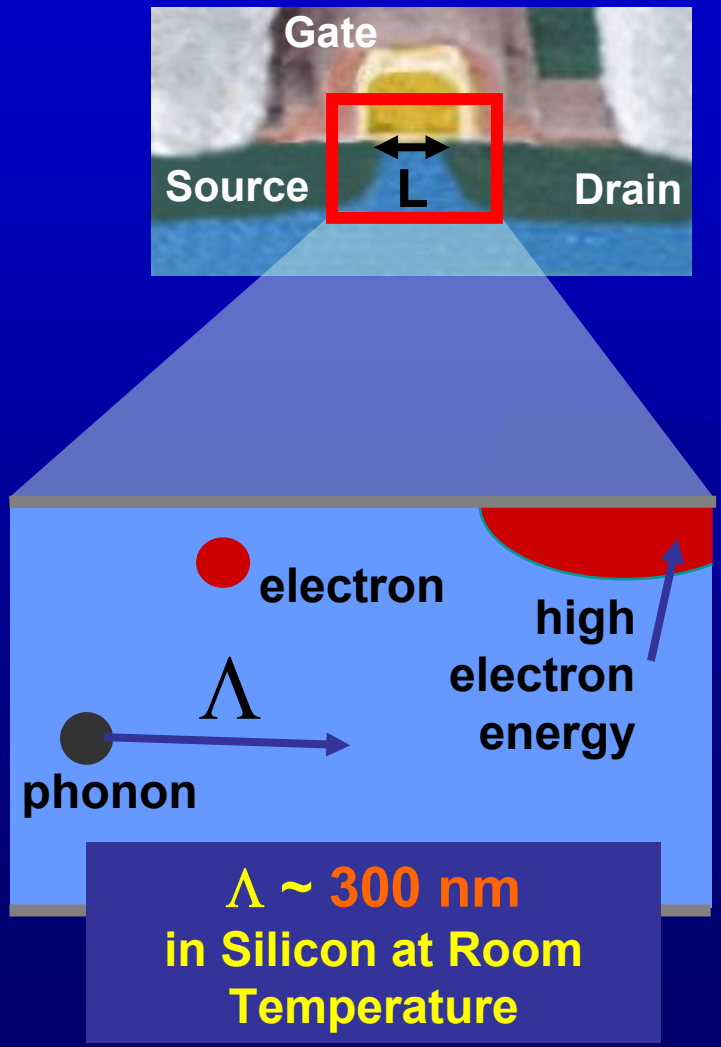


Im et al., IEEE TED, Dec. 2005

Im et al., IEDM 2002; Srivastava et al., VMIC 2004

- High temperature will become a major concern for interconnect reliability: maximum current density will be severely limited
- Accurate interconnect thermal profile important for various analysis: delay, skew, IR-drop etc

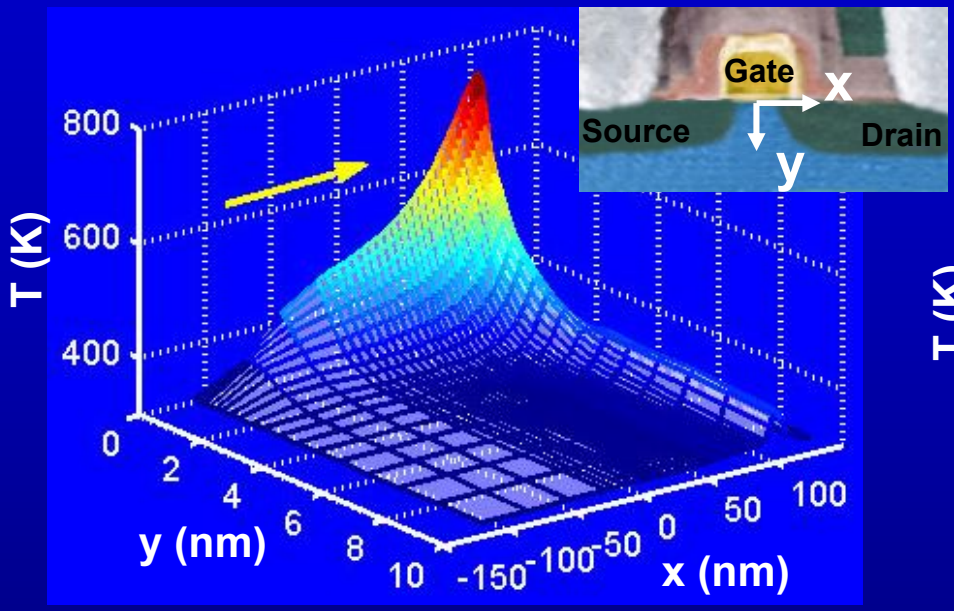
Electrothermal Effects in Nanoscale Devices

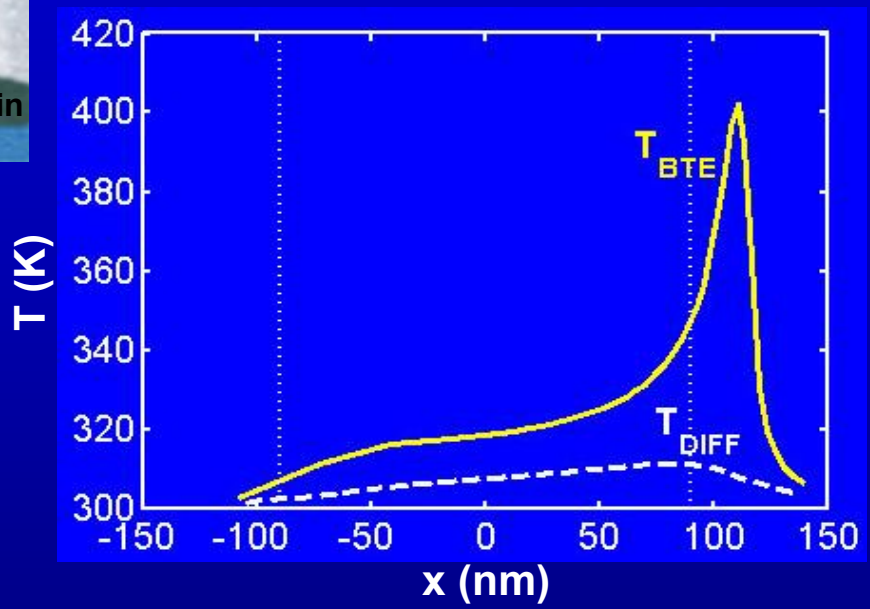


- Traditional CMOS scaling assumes isothermal problem
- High E field at drain → hot electrons
- Phonon hot spot near drain (as $\Lambda > L$)
- Affects device behavior
- Need to solve phonon Boltzmann Transport Equation (BTE)

Device Temperature Profile

Local hot-spot temperature rises well beyond the diffusion theory prediction.....





Pop et al. IEDM 2001

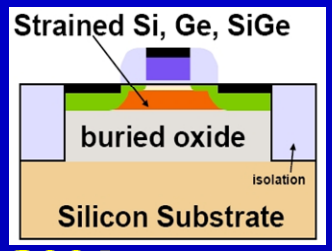
Indirectly verified against ESD failure pulses....

Sverdrup et al. SISPAD 2000

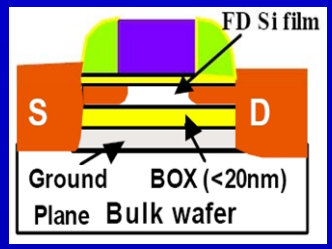
- **Important implications for device performance and leakage**
- **Critical for estimating failure conditions under ESD events**

Implications for Emerging CMOS

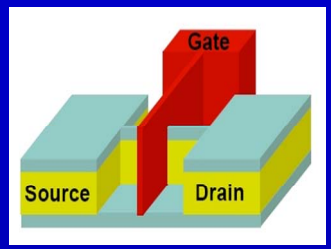
Transport-Enhanced



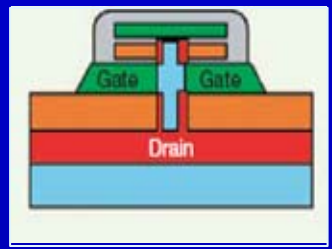
Ultra-Thin Body SOI



FinFET



Vertical Conduction

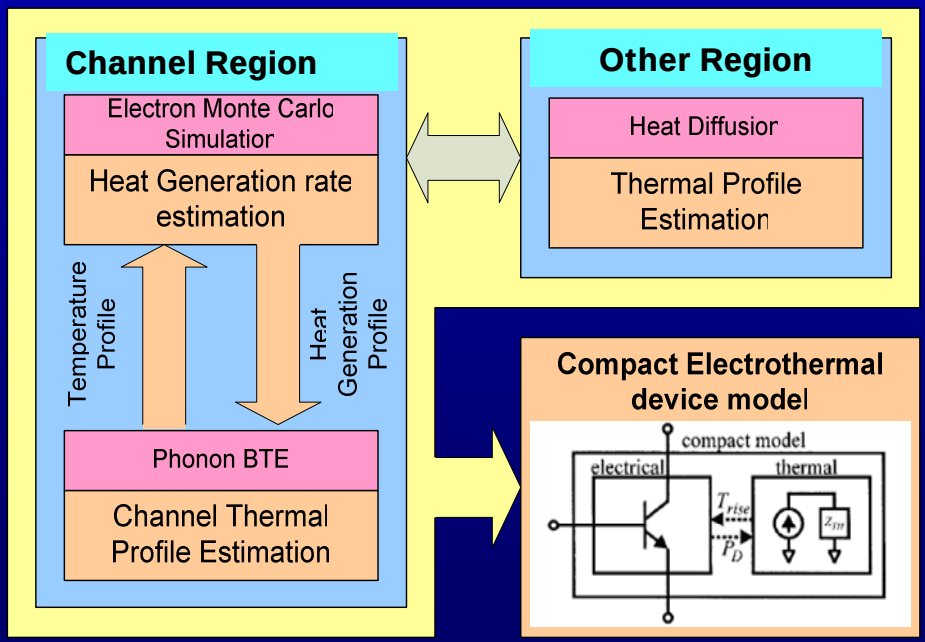


2004 Single Gate MOSFETs — Multiple Gate MOSFETs **2020**

65 nm → 10 nm

ITRS 2004

Electrothermal Device Modeling and Simulation



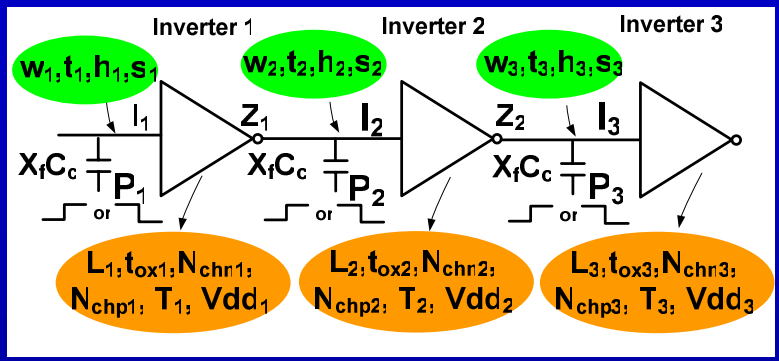
Due to confined geometry and poor thermal conductivity materials, emerging CMOS devices will exhibit severe localized heating effects !!

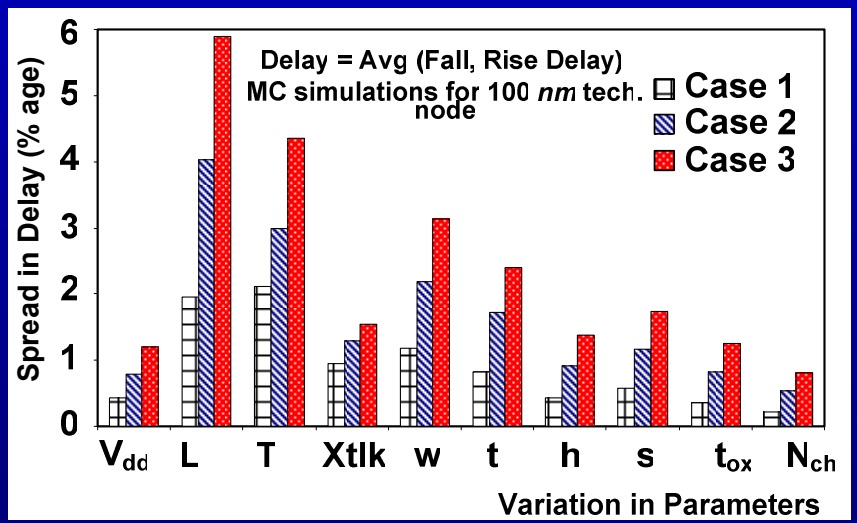
Ongoing Research:

Collaboration with Stanford, IBM and TI

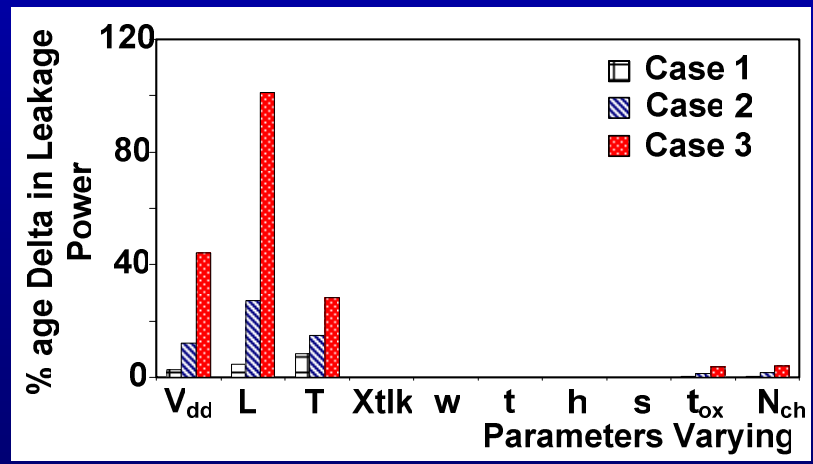
Circuit Level ET Issues (1)

Impact of temperature variations on buffered interconnect systems…..





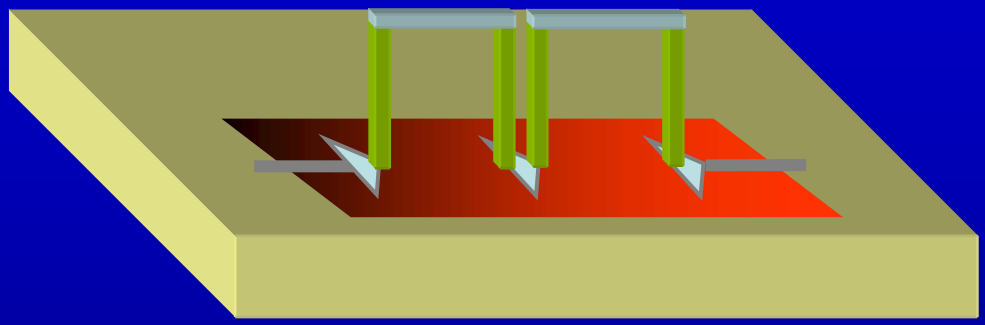
Wason and Banerjee, ISLPED 2005



Temperature variation has a strong impact on both delay and leakage power…..

Circuit Level ET Issues (2)

Impact of Substrate Thermal Gradients

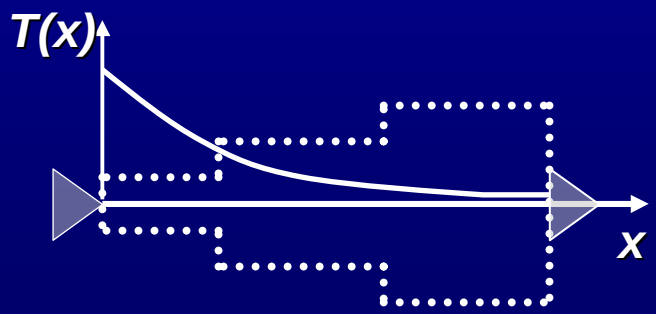


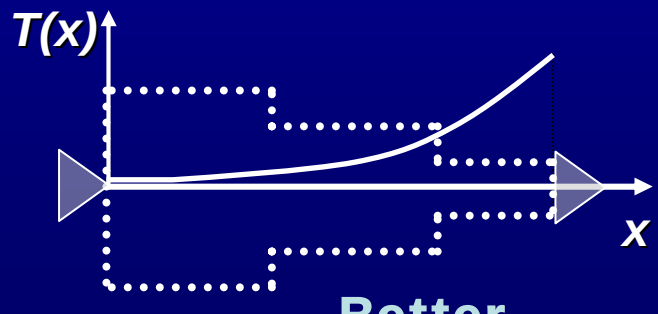
Delay/skew analysis for non-uniform interconnect temperature

Ajami et al., DAC 2001

Direction dependence of thermal gradient….

Increasing thermal profile has better performance than that of decreasing thermal profile (optimal wire sizing)



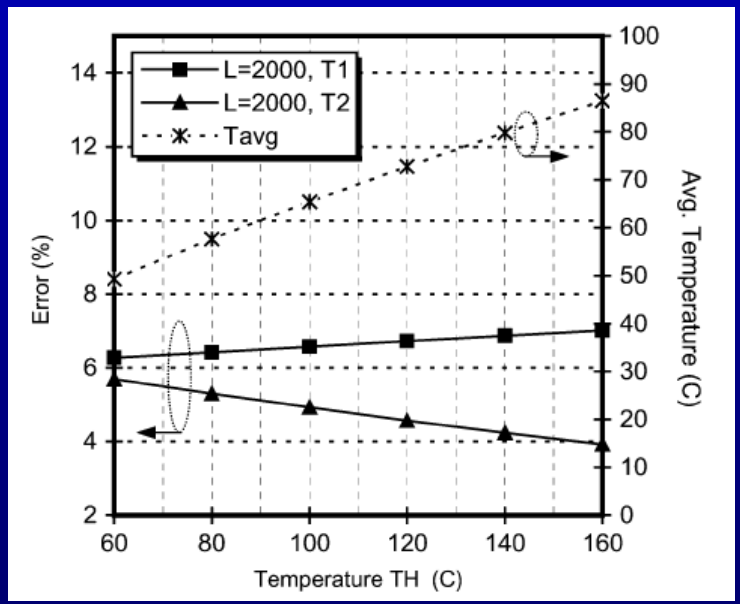


Better

Implications of Substrate Thermal Gradients

Impact on delay estimation.....

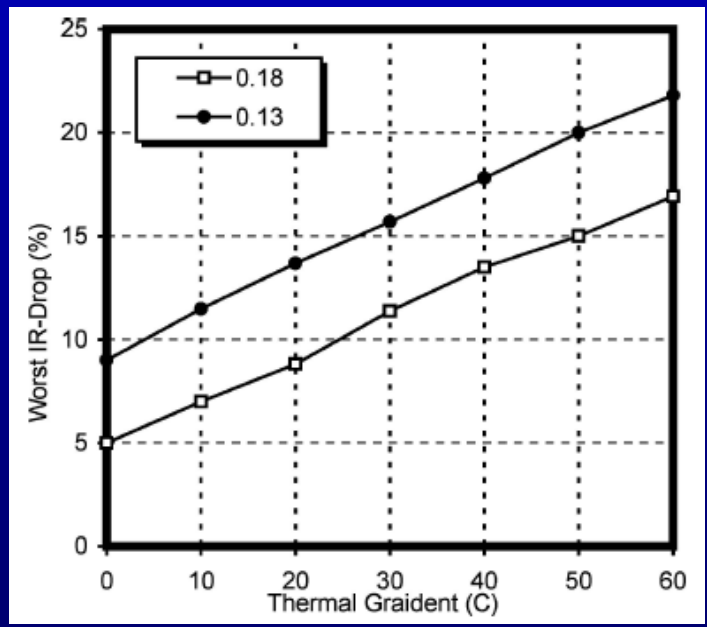
T1: positive exponential gradient
T2: negative exponential gradient
For a fixed T_Low



Ajami et al., TCAD 2005

Impact on IR-drop analysis.....

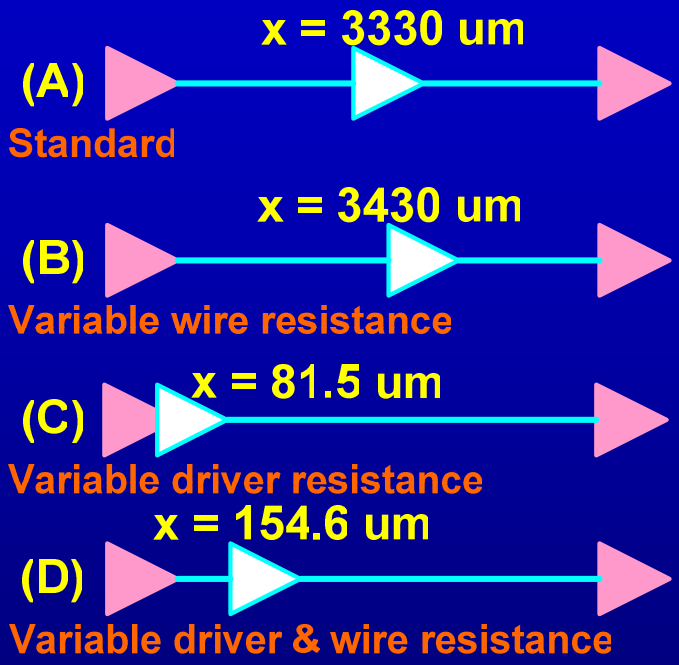
Worst-case voltage-drop (V_{IR}/V_{dd}) increases in the presence of thermal gradients

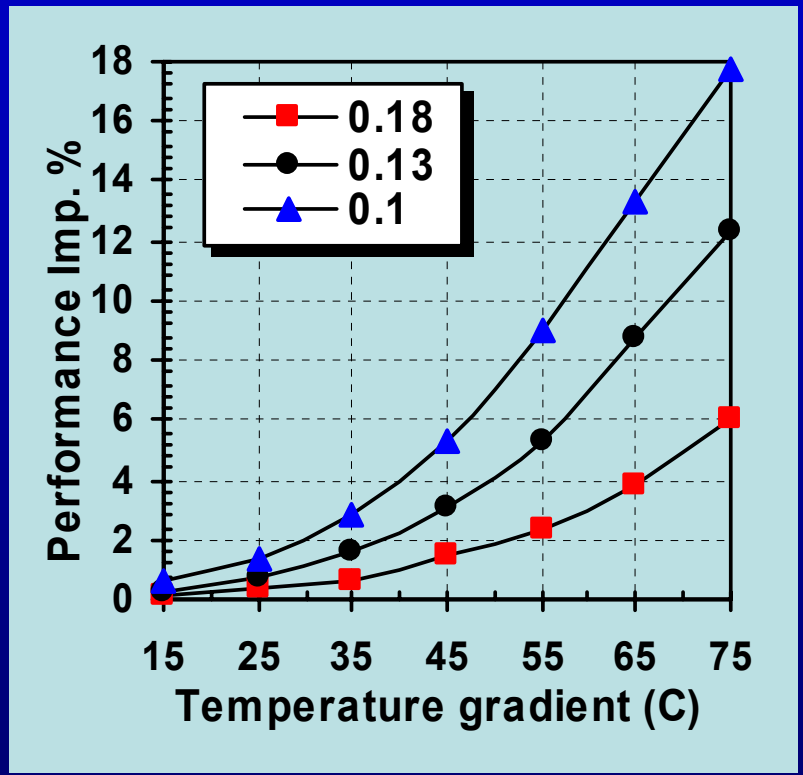


Ajami et al., JAICSP, 2005

Impact on Buffer Insertion

Buffer movement in a 6660 um line (180 nm node)





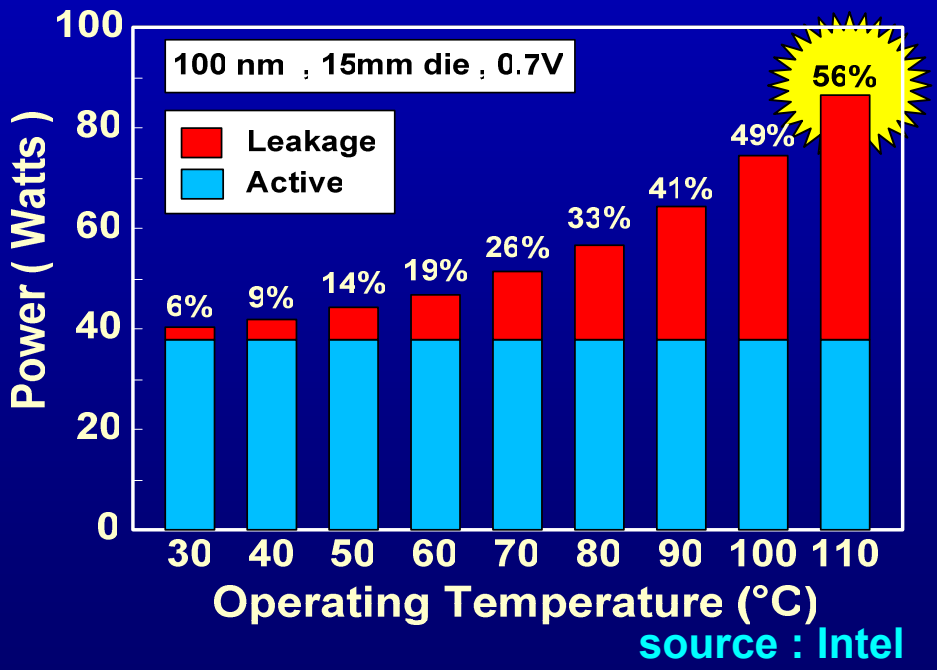
Ajami et al., ICCAD 2001

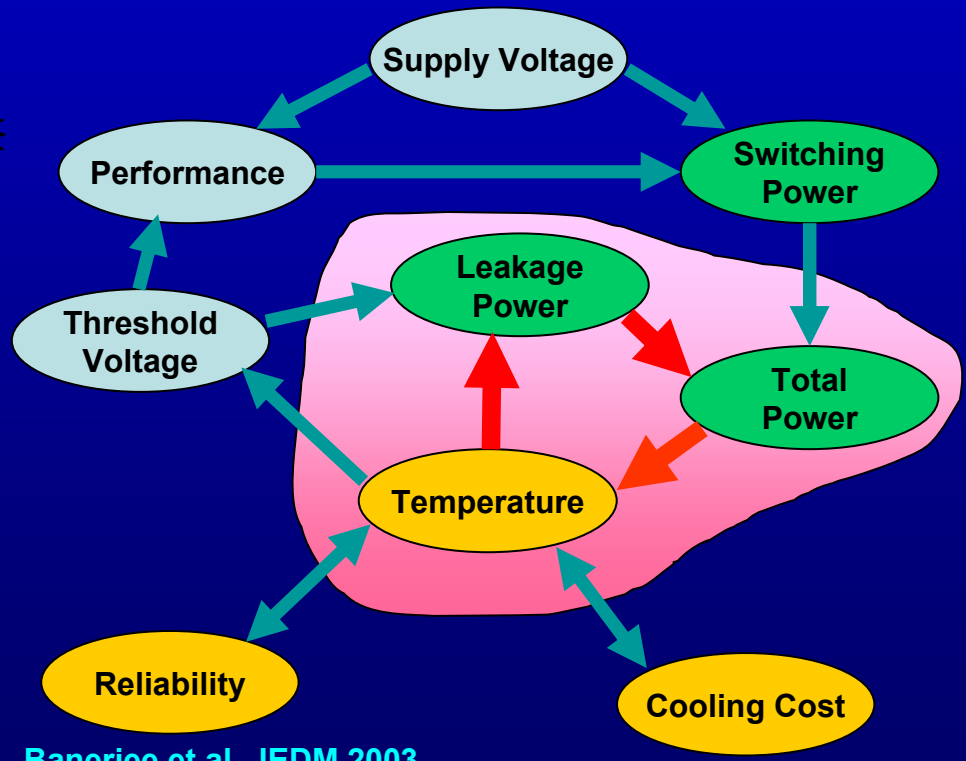
Delay improvement after thermally-aware buffer insertion

System Level: ET-Couplings

- Technology scaling
- Parameter variations
- Higher operating temperature

→ More leakage power → More Heat

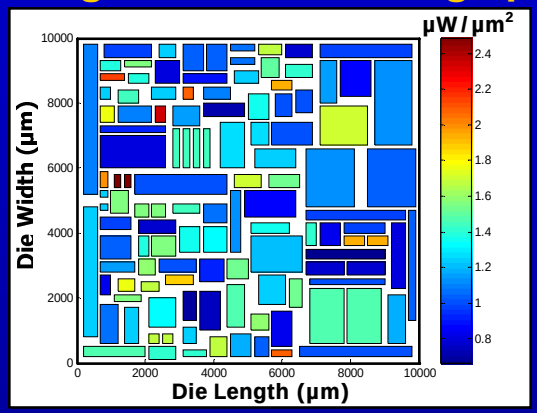




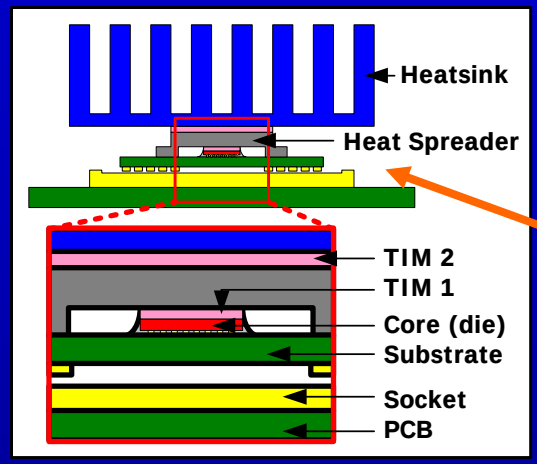
Banerjee et al., IEDM 2003

Self-Consistent ET Analysis Tool

Layout geometry & power Dissipation
(Including active and leakage power)



Packaging / Cooling Model



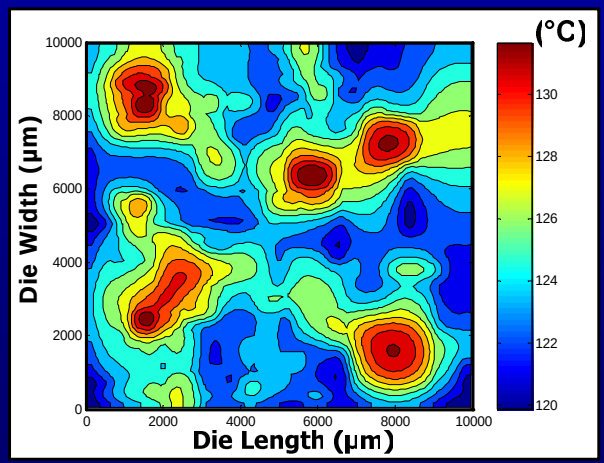
Realistic packaging structure

Boundary Conditions

Parabolic Heat PDEs

Electrothermal Couplings

3D Electrothermally-Aware Spatial Temperature Estimation



Lin et al. IEDM 2005

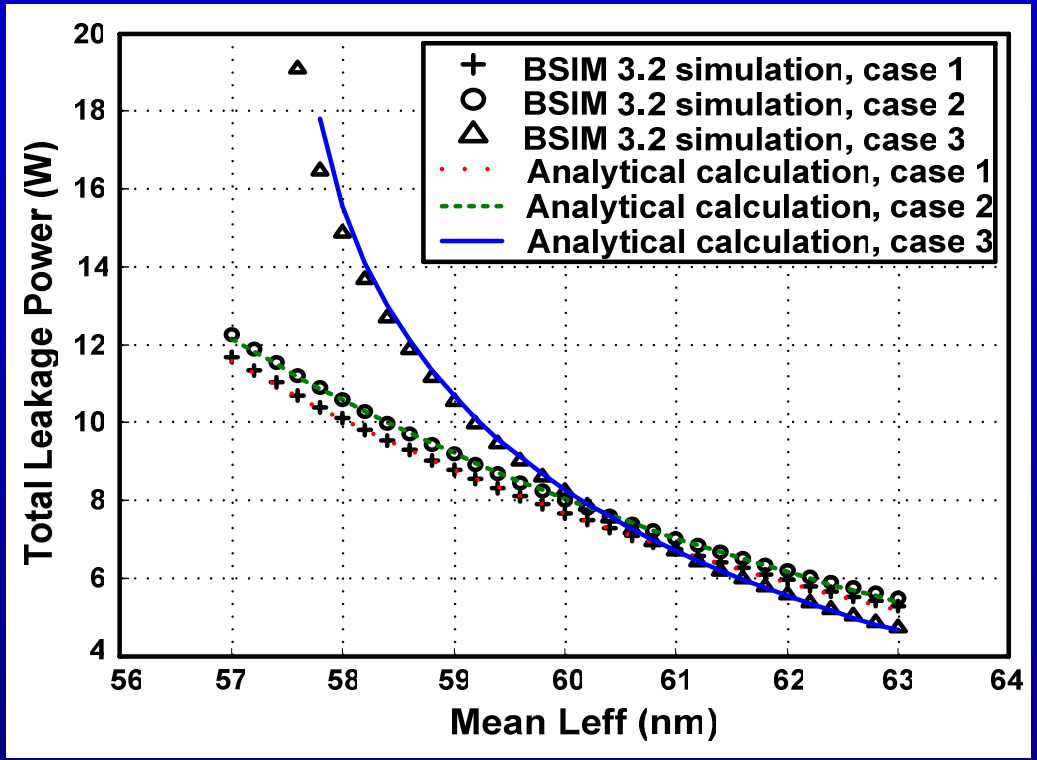
Self-Consistent Substrate Thermal Profile

Application-1: Full-Chip Leakage Estimation

Case 1: Die-to-die channel length variations

Case 2: Case1 + Within-die variations

Case 3: Case 2 + Die-to-die temperature variations



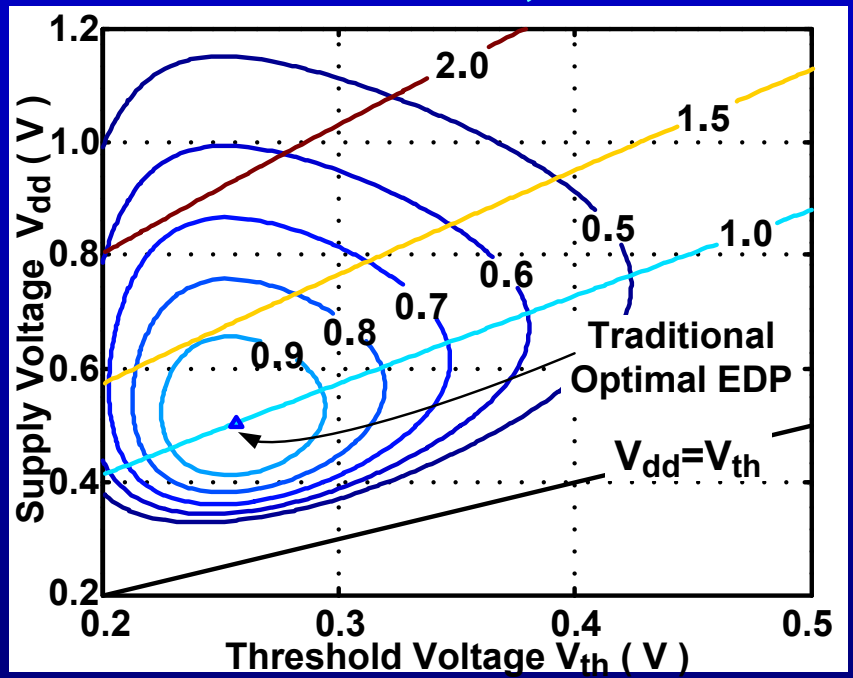
Zhang et al. ISLPED 2004

Die-to-die temperature variations significantly increases the leakage power

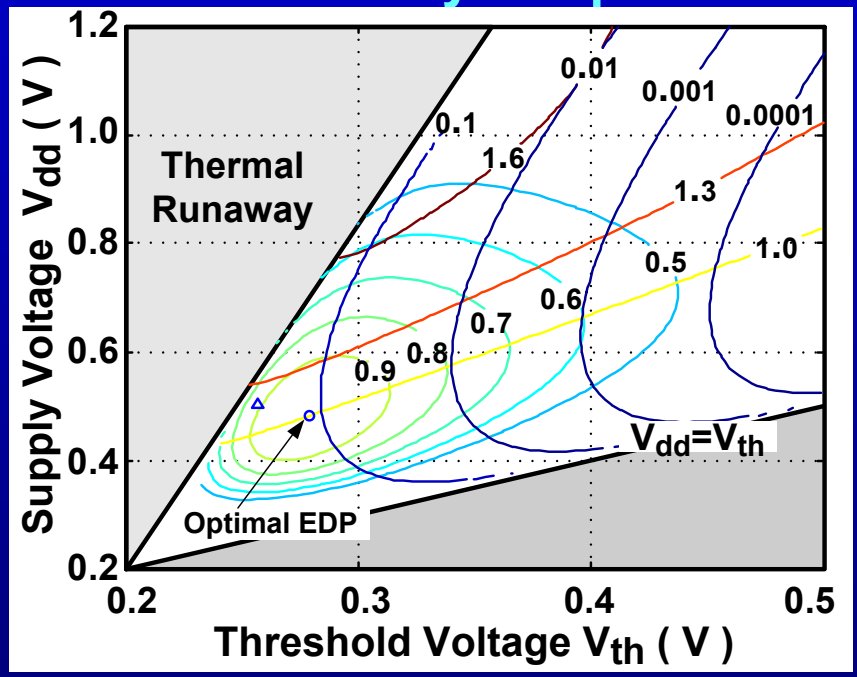
Application-2: Power-Performance Tradeoff

Vdd-Vth optimization using Energy-Delay Product (EDP)

Mark Horowitz, 1997



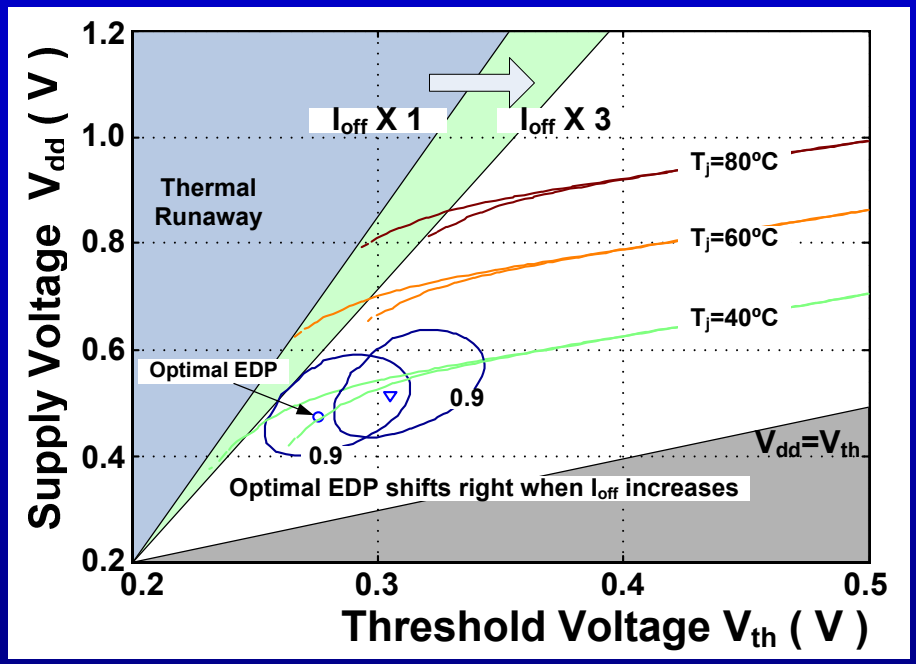
Electrothermally Coupled EDP

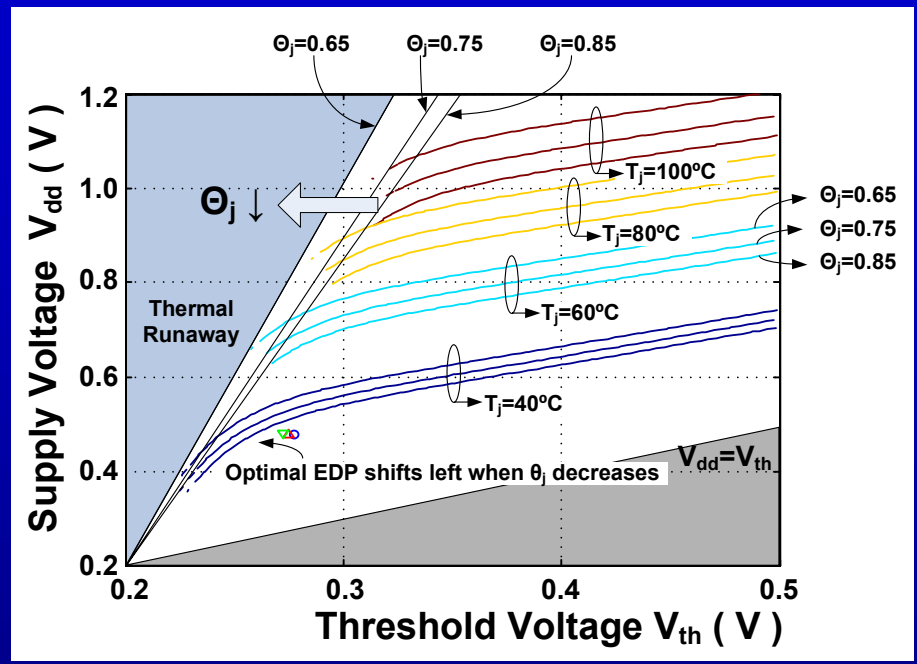


DAC 2004

- A shift in optimal point, EDP and performance contours
- An overall change in shape of EDP contours
- Operation region restricted by electrothermal constraints

Application-3: Leakage and Packaging Aware Design Space





Banerjee et al. IMAPS 2005

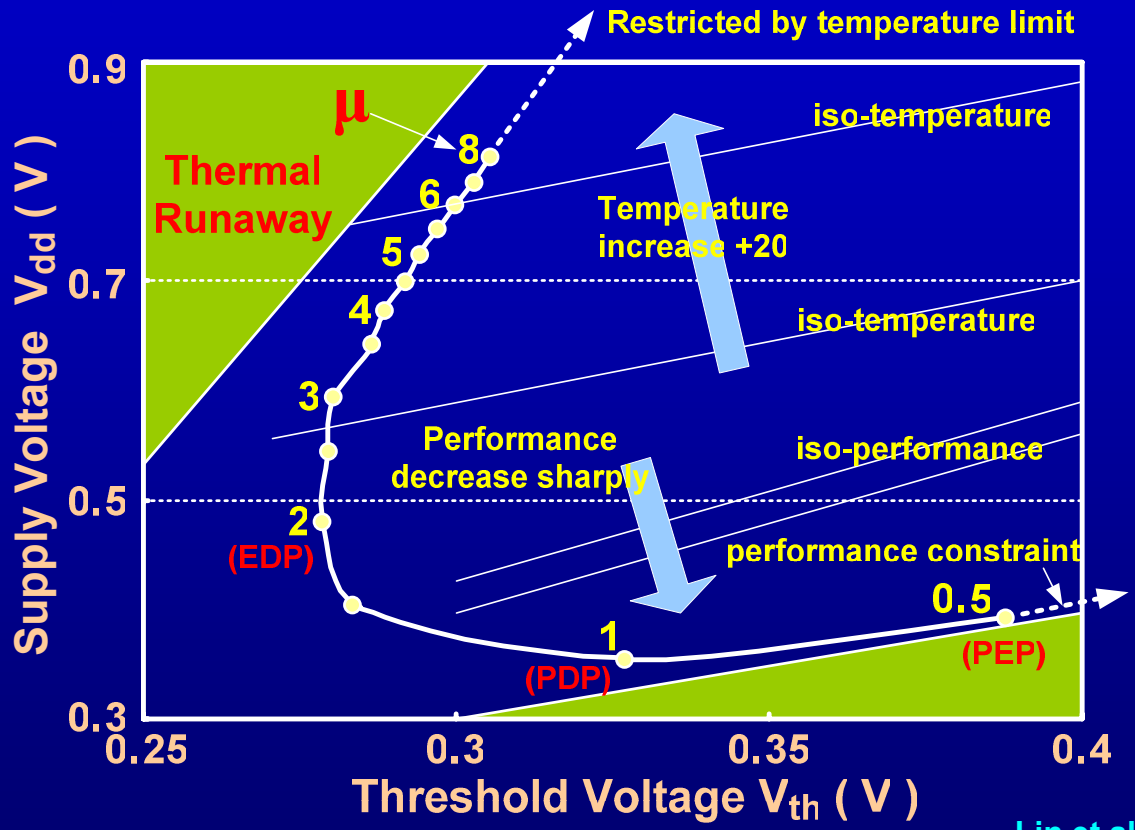
While the leakage increases due to technology scaling or process variations, the operation region prohibited by thermal runaway expands

Lowering of the junction temperature by employing advanced packaging and cooling techniques with lower thermal impedance (θ_j) will expand the design space

Allows circuit designers to comprehend reliability and packaging constraints.....

Application-4: Thermally-Aware Design-Specific Optimization

Different metrics result in different optimization……



Lin et al. ICCD 2005

Metric : PT^{μ}

ratio of the exponents of delay over power

EDP: PT^2 $\mu=2$

PDP: PT $\mu=1$

PDP: P^2T $\mu=0.5$

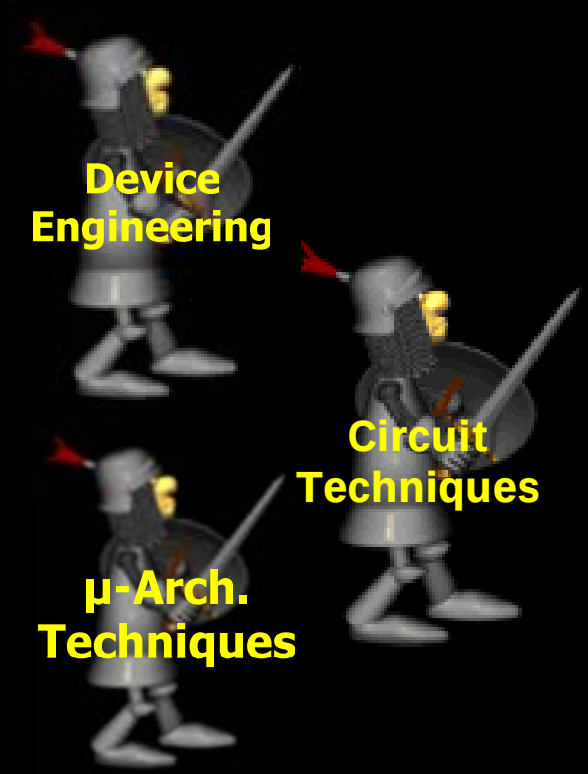
μ is bounded by thermal and performance requirements

Application-5: Power Management

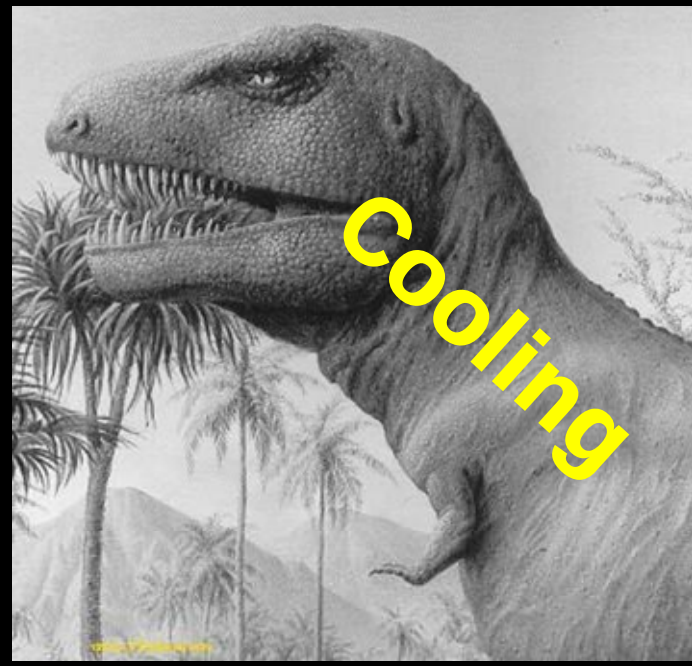
Efforts on Low Power….without hurting performance

- **Device Engineering**
  - Enhanced Channel Mobility
  - Reduced Gate Leakage
    - High-K Gate, Nitrogen Doped
- **Circuit Level**
  - Adaptive body-biasing, Dual V_{th}
  - Sleep Transistor, Clock/Power Gating
- **Micro-Architecture Level**
  - Multi-Core

Why Cooling

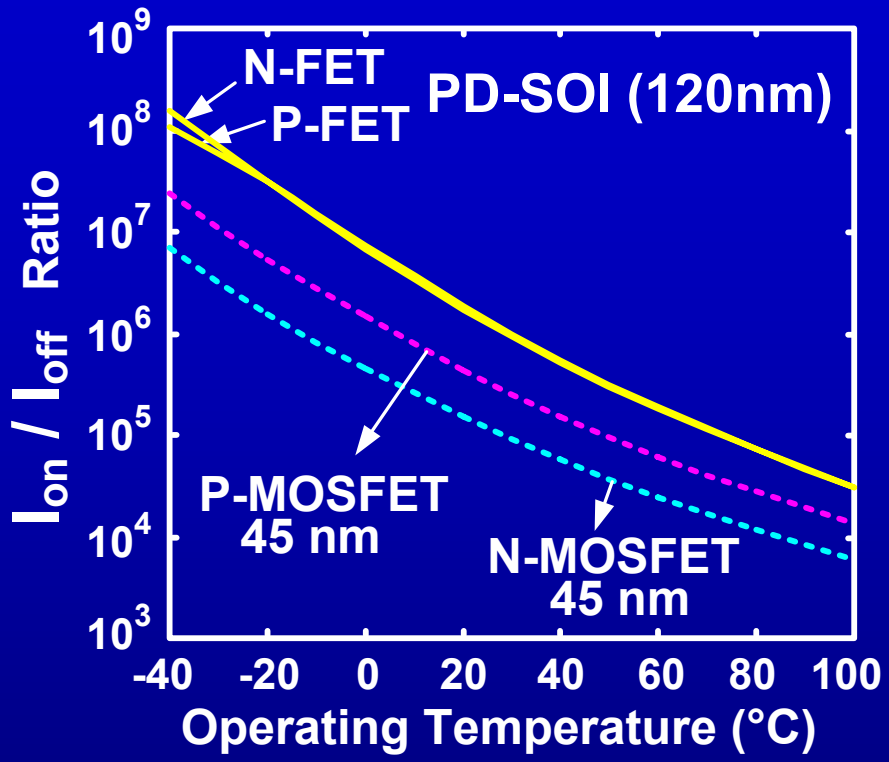


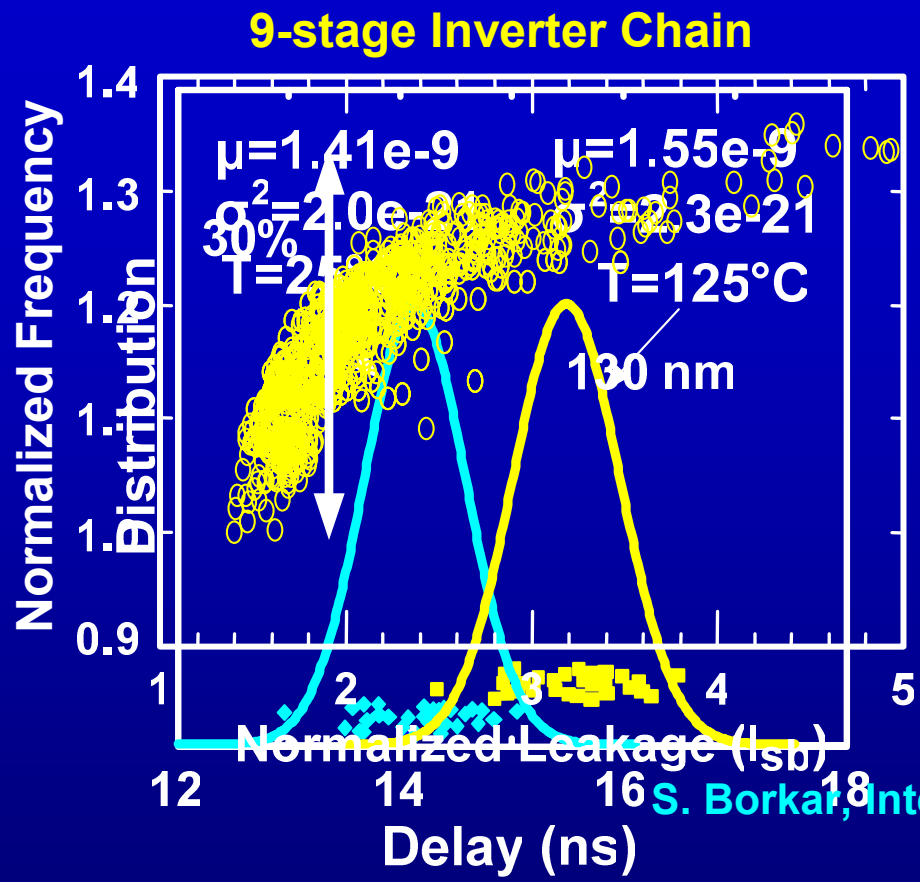
Power
Dissipation



Cooling is the Knob !

Device and Circuit Level Benefit



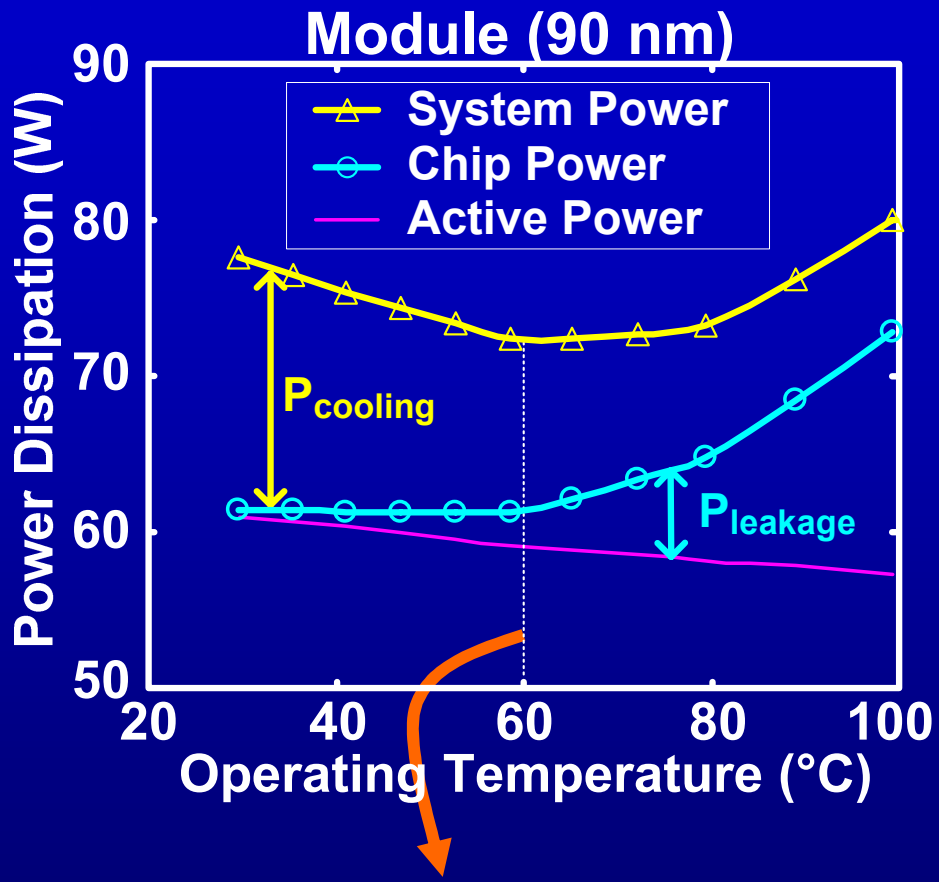


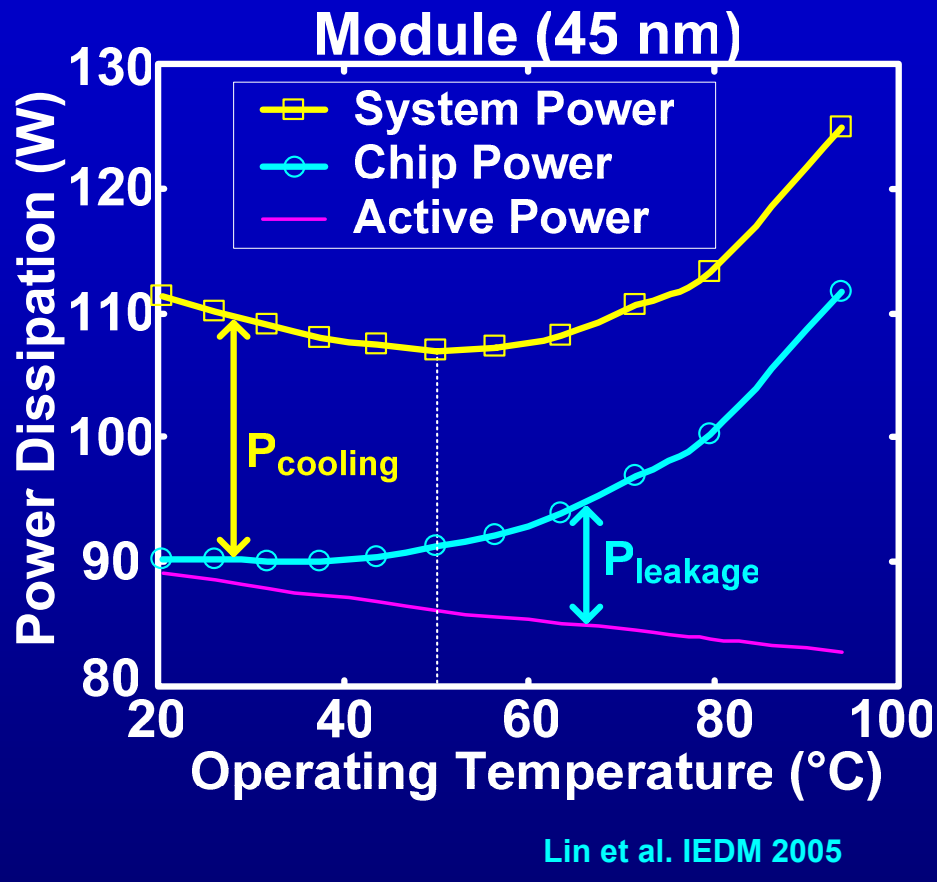
Lowering temperature

- Enhance Ion to Ioff ratio
- Reduce propagation delay and variance
- Benefit back-end performance and reliability

Lin et al. IEDM 2005

Cooling Benefit-Cost Tradeoff





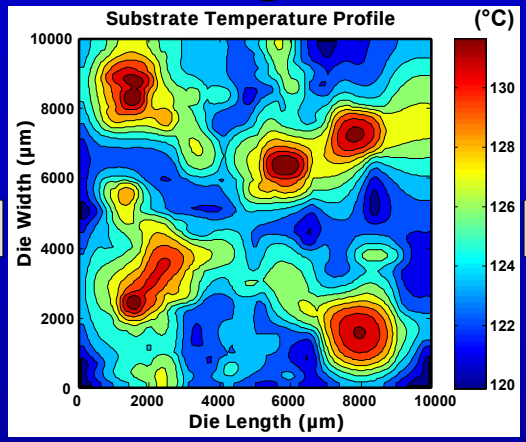
Lin et al. IEDM 2005

Beyond this point, further cooling does not lead to any power saving

The limit occurs at a lower temperature as technology scales

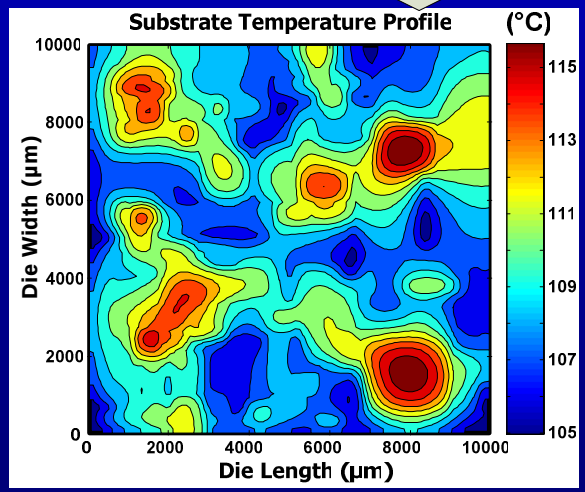
Hot-Spot Management

Global vs. localized cooling



Global cooling

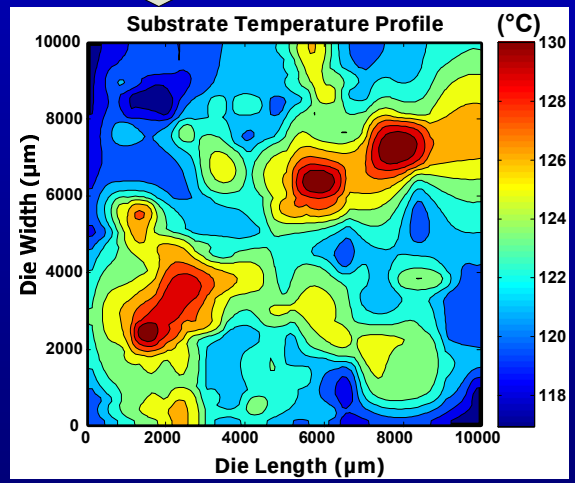
T_{MAX} decreases but hot-spots remain



(reduce θ_{ja} 20 %)

Lin et al. IEDM 2005

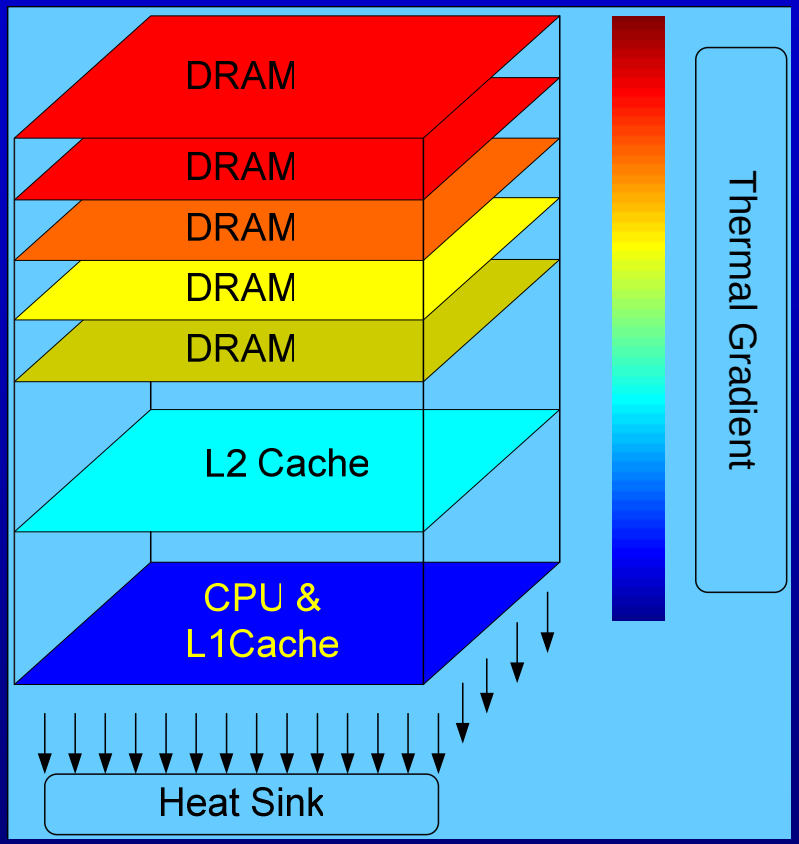
Localized cooling

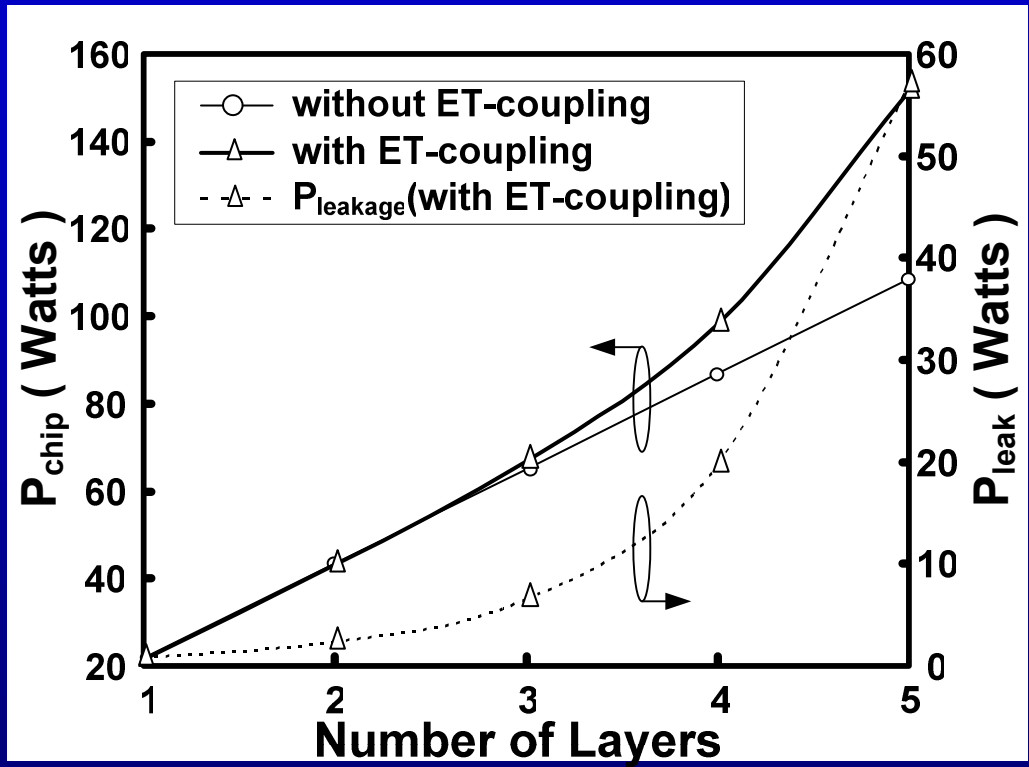


(Using thin-film TEC)
Size 0.8 mm X 0.8 mm

Localized cooling will be more effective for hot-spot management

ET Issues in 3D ICs

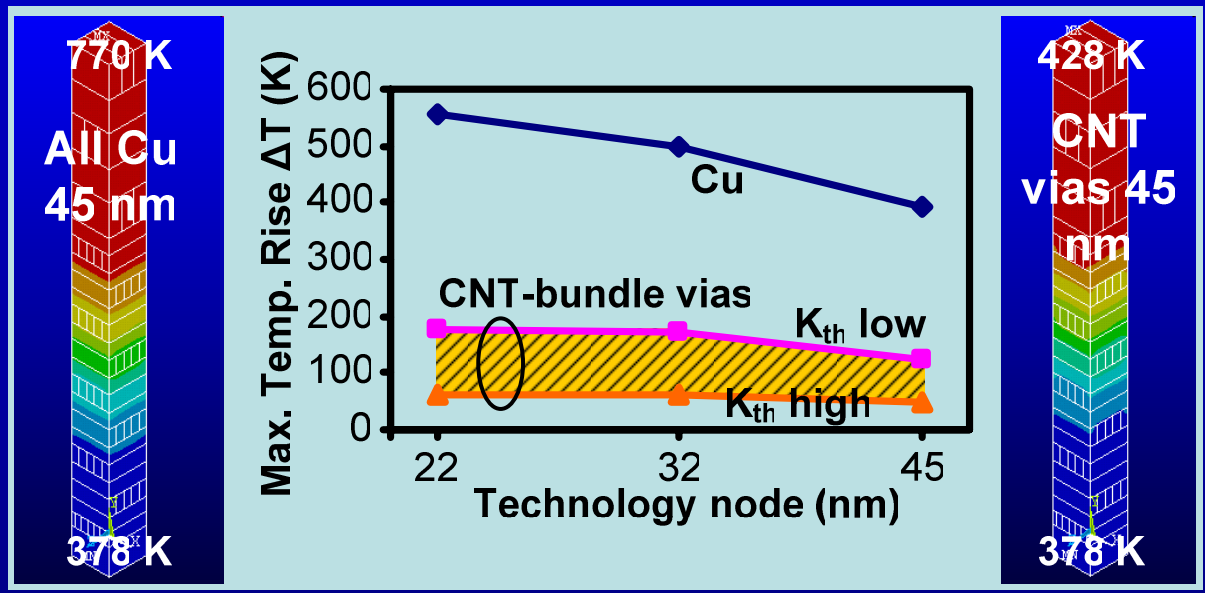




Banerjee et al. Proc. IEEE, 2001

Performance evaluation of 3D design must account for negative impact of high temperature on all active layers

Hybrid Carbon Nanotube-Cu Interconnects



Srivastava et al. IEDM 2005

For CNT bundles, the shaded region shows the range

1750 W/mK < *Kth* < 5800 W/mK

Maximum interconnect temperature rise for Cu interconnect stack with Cu vias compared to CNT bundle vias integrated with Cu interconnects

Conclusions

- **Electrothermal effects are increasing at every level *from devices and interconnects to circuits and systems* ---need careful modeling and optimization**
- **Electrothermal Engineering is a critical need…..**

  ---temperature awareness at every level to optimize performance, power and reliability

  --- understand various couplings through an integrated approach
- **Emerging technologies ---will be strongly affected**