Double Edge Triggered Feedback Flip-Flop

S. H. Rasouli, A. Amirabadi, A. S. Seyedi and A. Afzali-Kusha

Low-power High-Performance Nanosystems Lab., Elec. and Comp. Eng. Dept., University of Tehran, Tehran, Iran

a.seyedi@ece.ut.ac.ir, hrasouli@ece.ut.ac.ir, a.amirabadi@ece.ut.ac.ir ,afzali@ut.ac.ir

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Introduction

Introduction

- The power consumption of the systems is a critically important parameter in modern VLSI circuits especially for low power applications.
- One of these techniques is to use low power logic styles which should be used in design of latches and flip-flops.
- *Tclk-q* (delay from *clk* to output of FF) and *Cclk* (the load capacitance of the clock).
- In addition to the dynamic power consumption, the high leakage current in deep sub-micron regimes is a significant contributor to the power dissipation of CMOS circuits as the CMOS technology scales down.

Introduction

- Several flip-flops have been proposed in the literature for improving the speed and/or reducing the power consumption.
- Hybrid Latch Flip-Flop (HLFF).
- Semi-Dynamic Flip-Flop (SDFF).
- Conditional Capture Flip flop (CCFF).

Introduction

- The dynamic power consumption in the clock tree depends on the frequency, the voltage swing, and the load of clock tree.
- If the sampling of the input is performed in both rising and falling edge of clock (double-edge triggered), then for same applications and operational speeds, the frequency of the clock can be half of the clock frequency of the single edge triggered FF.
- Low-Swing clock Double-edge triggered Flip-Flop (LSDFF).
- Double-edge triggered Feedback Flip-Flop (DFFF) has less dynamic power consumption, static power, and delay compared to the previous flip-flops.

Flip-Flop Structures

Single-edge triggered Flip-Flops

- It is based on generating an explicit transparency window for the time that the transition is allowed.
- In each clock cycle, when the input is high, regardless of previous state of the output a glitch is generated.
- The transistors in the stack degrade the performance of the logic.
- These disadvantages make HLFF not suitable for low power applications.

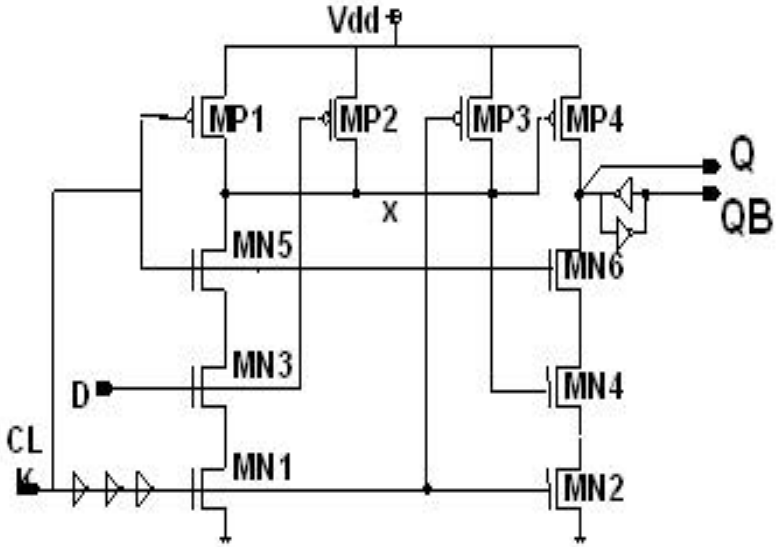


Figure 1.Circuit diagram of HLFF.

Single-edge triggered Flip-Flops

- This logic is faster than HLFF due to its lower number of transistors in the stack.
- The total number of transistors is greater than HLFF.
- Similar to HLFF unnecessary internal node transitions exist in SDFF.

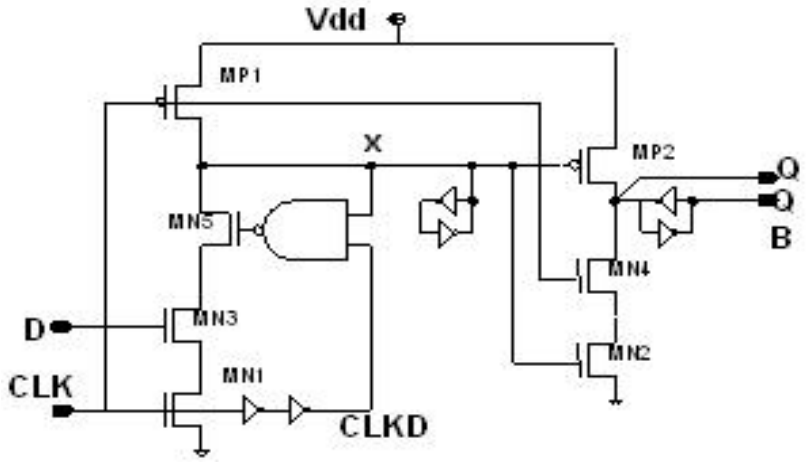


Figure 2. Circuit diagram of SDFF.

Double-edge triggered Flip-Flops

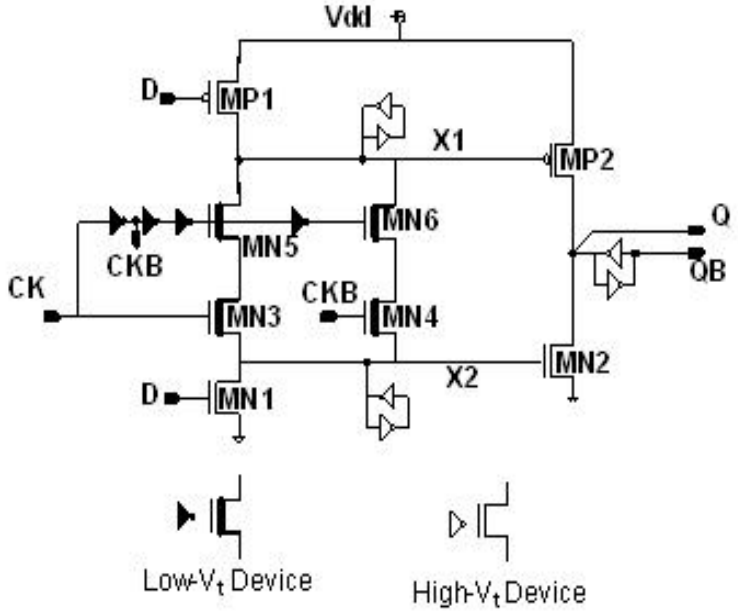


Figure 3. Circuit diagram of LSDFF.

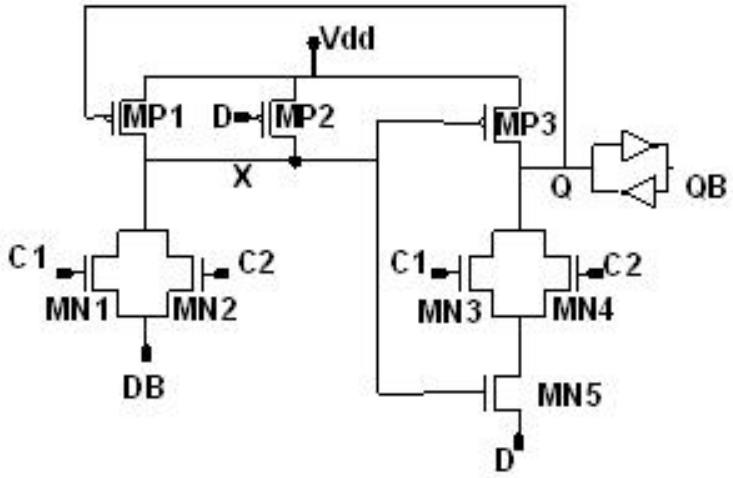
Double-edge triggered Flip-Flops

- The input of the flip-flop is transferred to the output at the rising and falling edges of the clock.
- To reduce the power consumption of the clock tree, a low swing clock is used in this logic.
- clock tree, a low swing clock is used in this logic. To have a proper functioning, some of high-Vth transistors are replaced with low-Vth transistors whose subthreshold currents are controlled by high-Vth transistors.
- For the same throughput, the frequency of the clock in LSDFF could be half of the frequency of the clock in HLFF or SDFF.

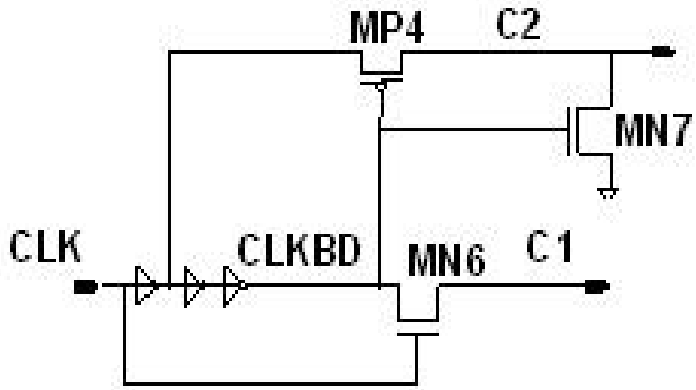
Double-edge triggered Flip-Flops

- As the swing and the frequency of the clock is lower, the power consumption of LSDFF clock tree could be lower than those of others.
- Uncontrolled subthreshold current low-*Vth* transistors in the clock tree leads to a more power consumption.
- Since the charging (discharging) the internal node X2 (X1) is done through three transistors, the speed of the circuit is reduced.

Double-edge triggered Flip-Flops



(a)



(b)

Figure 4. structure of (a) DFFF (b) clock-tree.

Double-edge triggered Flip-Flops

- The node transitions occur only when the inputs are different in two successive clocks.
- When the clock (CLK) makes a transition from low to high, CLKBD remains high for a period equal to the delay of the three inverters creating a transparency window. In this period, C1 is high turning on MN1 and MN3. In this window, if D is low and Q is high (D was high in the previous clock), MP2 becomes turning on MN2 which forces the output to low. If both D and Q are low, MP1 and MN2 are on before the beginning of the transparency window making the delay zero (similar to previous flip-flops). If D is high and Q is low, node X becomes low turning on MP3 which forces the output to high.

Double-edge triggered Flip-Flops

- As MP1 is a weak transistor, the fighting problem during the output change is alleviated.
- If D is high and Q is high, node X will not change and, therefore, redundant transitions are avoided.
- There is no delay whenever D is high in two successive clock cycles.
- The charging of the node X is done through two paths. This increases the speed of the FF compared to the previous ones.

Double-edge triggered Flip-Flops

- The node X is discharged through only one transistor (MN1 or MN2) that again leads to the reduction of the DFFF delay.
- Choosing MP1 as a small pull-up device, a weak fighting might exist during an input state change in two successive clock cycles.

Double-edge triggered Flip-Flops

- The operation of the logic at the falling edge of the clock is similar to its operation at the rising edge except that and MN2 and MN4 play the role of MN1 and MN3, respectively.

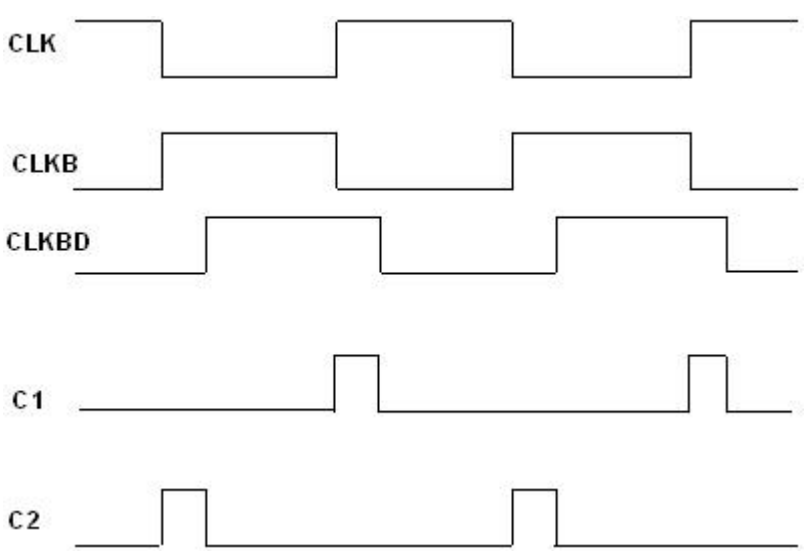


Figure 5. The timing diagram of C1 and C2 in DFFF.

Double-edge triggered Flip-Flops

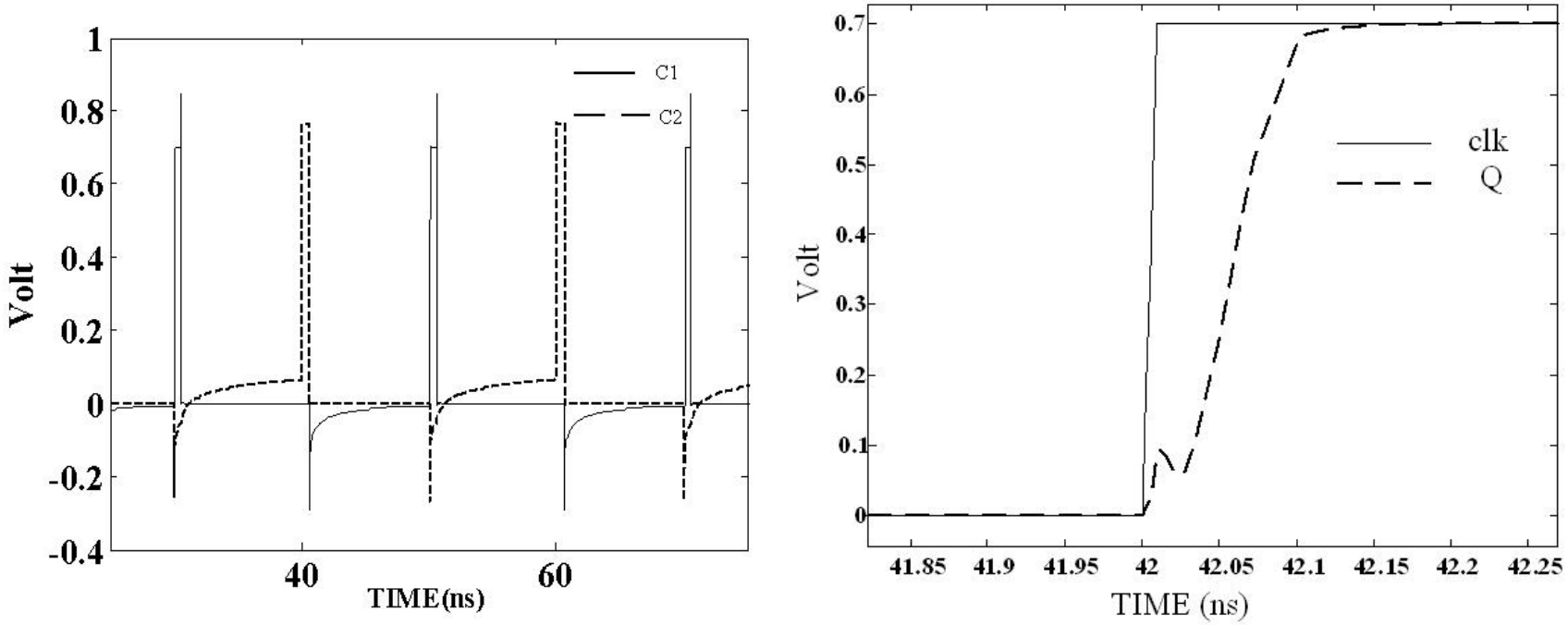


Figure 6. the waveform of (a) the controlling signal (i.e. C1 and C2)

(b) The output of DFFF.

Subthreshold Current

- Subthreshold or weak inversion conduction current between the source and drain in an MOS transistor occurs when the gate voltage is below *Vth.*

$$I_{ds} = \mu_0 C_{ox} \frac{W}{L}(m-1)(v_T)^2 \times \exp[\frac{(V_g - V_{th})}{m v_T}]$$

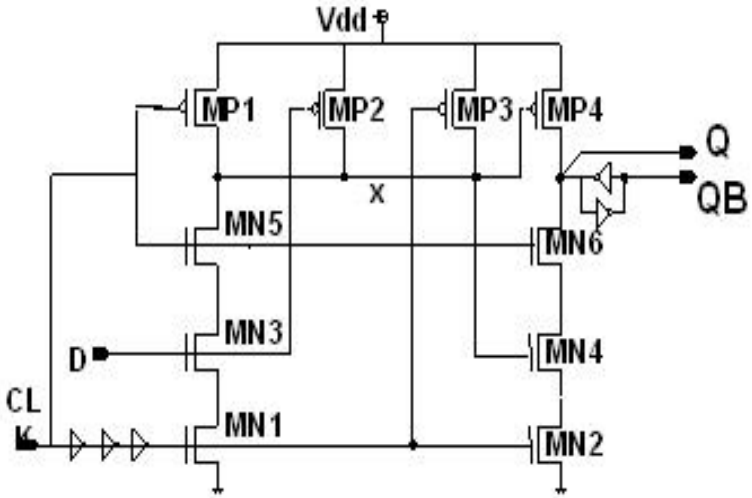
$$\times (1 - \exp[\frac{-V_{DS}}{v_T}]) \qquad (1)$$

where

$$m = 1 + \frac{3 t_{ox}}{W_{dm}}$$

Subthreshold Current

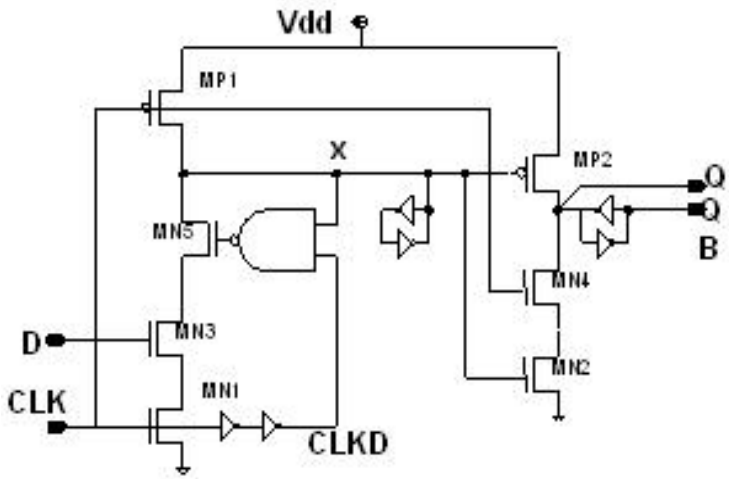
- When the node X is high, a voltage equal to *Vdd* is applied across the first branch in the pull down network (consisting of MN1, MN3 and MN5).
- When the node *X* is low then *Q* (output) will be high and output pull down tree sustains a voltage equal to *Vdd*. This high *VDS* voltage drop causes large leakage currents and hence high leakage powers.



(again) Figure 1.Circuit diagram of HLFF

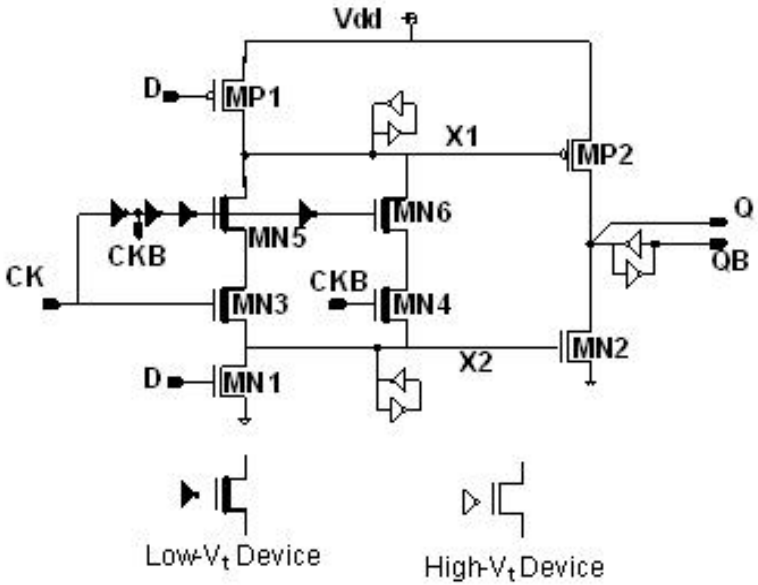
Subthreshold Current

- The situation is even worse in the case of SDFF where this voltage exists across two transistors compared to the case of HLFF where three transistors exist in the output pull down network.



(again) Figure 2. Circuit diagram of SDFF

Subthreshold Current

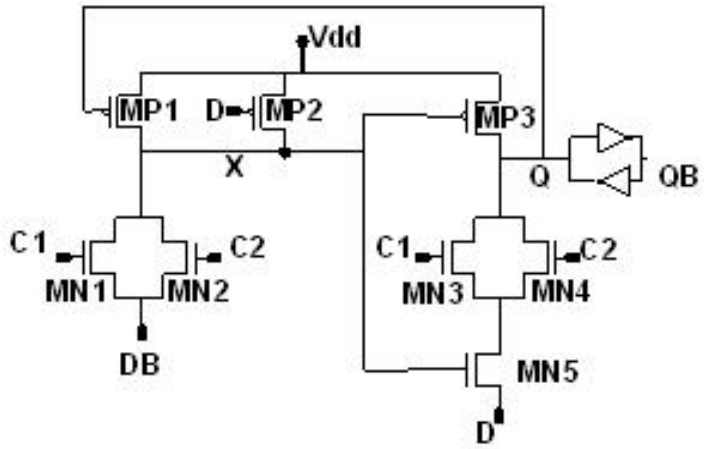


(again) Figure 3. Circuit diagram of LSDFF.

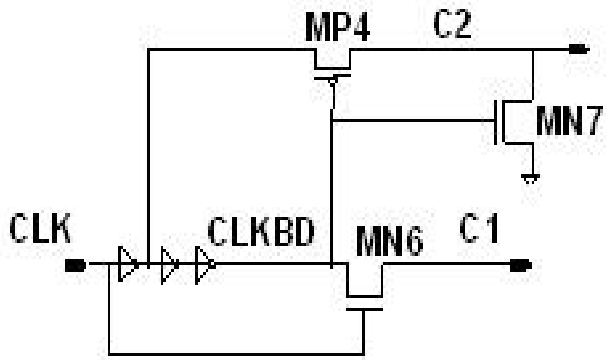
Subthreshold Current

- Now LSDFF: Suppose that D is low, and then the voltage of node X2 as well as *VDS* of MN1 is equal to *Vdd*. In the case that D is high, the *VDS* of MN2 will be equal to *Vdd* and, hence, only one transistor has a high *VDS* drop.
- The leakage current will be higher than the previous flip-flops.

Subthreshold Current



(a)



(b)

(again) Figure 4. structure of (a) DFFF (b) clock-tree

Subthreshold Current

- The *VDS* of each transistor in the pulldown network will be zero.
- Assuming D is high (DB is low), node X will be high, and, hence, both the drain and the source of MN1 and MN2 have high logic values leading to an approximately zero *VDS* for these transistors. When D as well as Q is high, the voltage drop across the output pull-down tree will be approximately zero too.
- Compared to other flip flops, subthreshold current in DFFF is very low. These very low *VDS* minimize the subthreshold leakage current of the flip flop.

Simulation Results

- All the discussed flip flops have been simulated in a 70 *nm* CMOS process.
- *Vdd* = 0.7V and the clock frequencies were 100MHz and 50 MHz for single-edge and double-edge triggered FF's. The load capacitance=10 fF.

Simulation Results

	No. of Tr.	No. of Clked Tr.	Clk-Q (ps)	Power (uW)	P.D (fj)	improvement
SDFF	23	5	124	1.9	.236	83%
HLFF	20	4	132	1.87	.247	84%
LSDFF	28	3	94	1.4	0.132	70%
DFFF	21	3	53	0.76	0.041	-

Table 1: Comparing various structures of DFF

Simulation Results

	SDFF	HLFF	LSDFF	DFFF
Leakage Power (nW)	86	49	82	27

Table 2: Comparison between LSDFF and DMHLFF structures

Summary and Conclusion

- Double edge triggered Feedback Flip-flop (DFFF) which had a better performance compared to previous logic.
- Unnecessary internal node transitions were avoided in this logic.
- This logic may work with a lower clock frequency.
- These two reduced the power consumption of the flip-flop compared to other flip-flops.
- Reducing the number of transistors in the stack for both the internal and the output nodes and increasing the number of charging and discharging paths decreased the delay of the logic.

Summary and Conclusion

- The simulation results indicate that the improvement in the performance of DFFF is approximately between 70% and 84% compared to previous works.

Thank You!