Delay Defect Screening for a 2.16GHz SPARC64 Microprocessor

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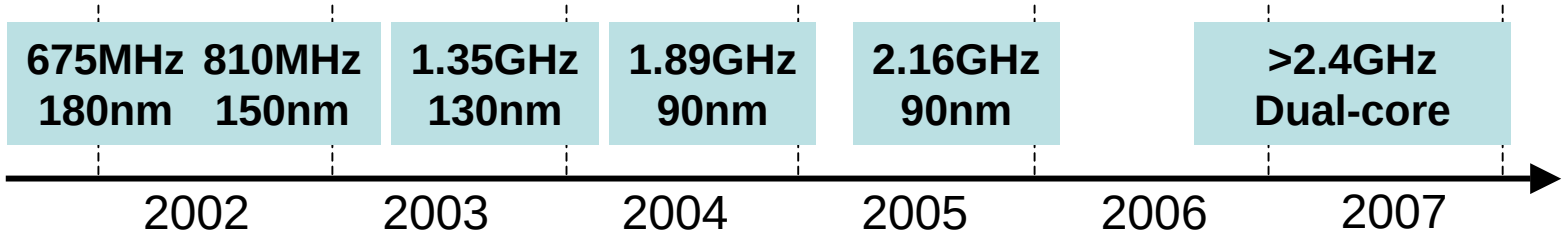
Outline

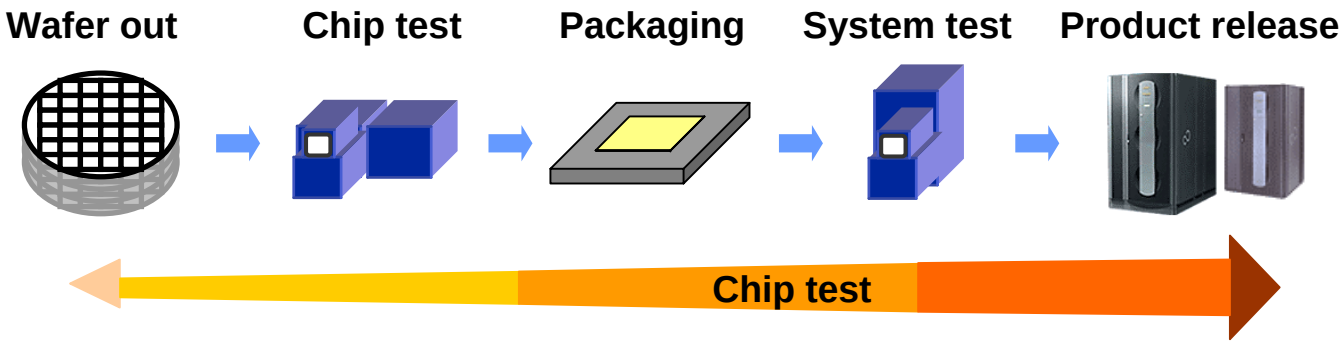
- Motivation
- Delay test economics
- Detection of multiple delay faults
- Screening results
- Coverage analysis
- Conclusions

Motivation

- The importance of screening delay defects increases with smaller feature sizes and higher frequency.

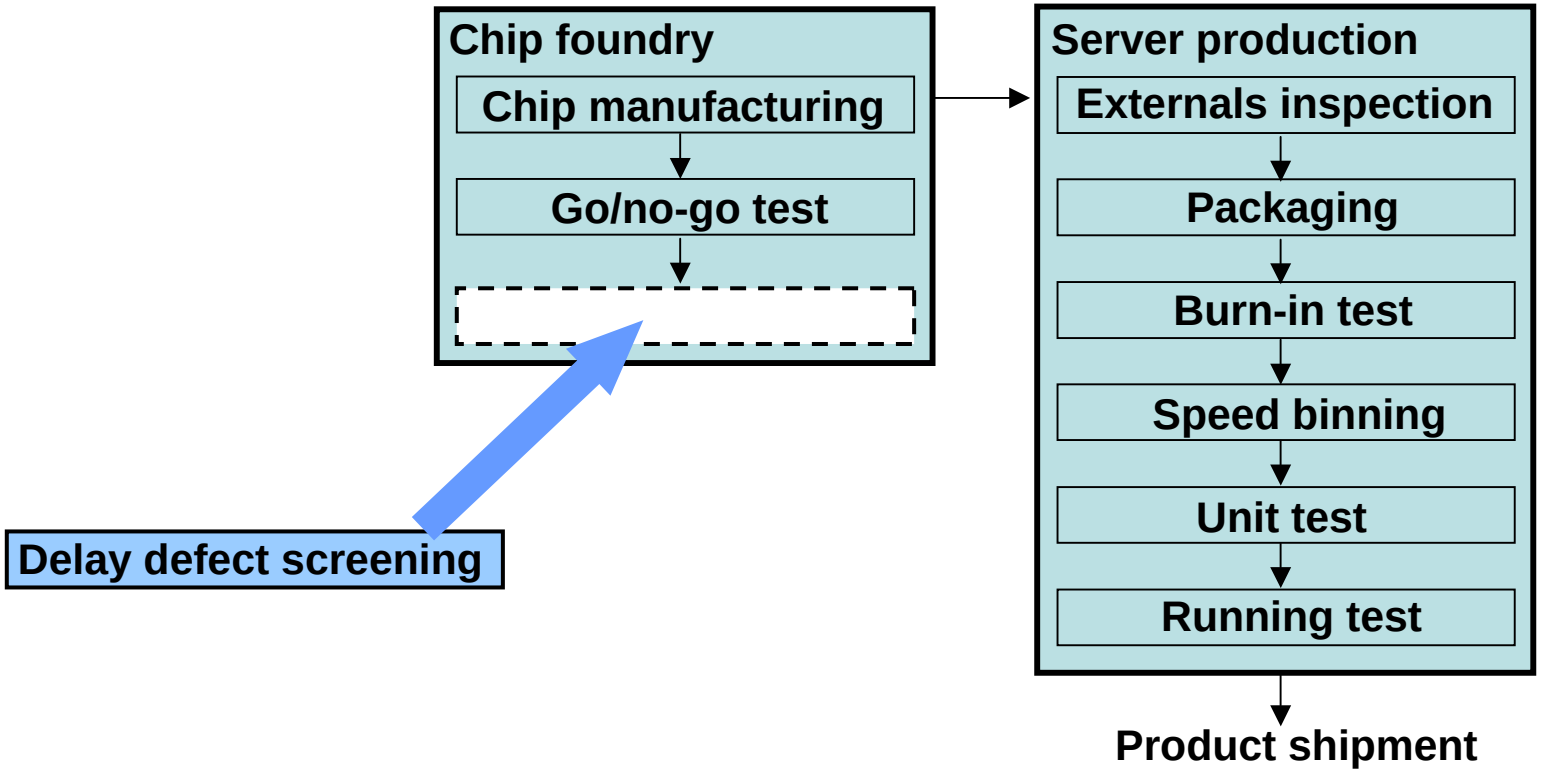


- The later a delay defect is found, the larger the manufacturing cost is.



Motivation (cont'd)

- We must reduce delay defects found in the server production phase by screening based on a delay test at wafer-level.



Delay test economics

- Results of delay test and system test are categorized as follows:

		Delay test	
		Pass	Fail
System test after packaging	Pass	**Case A:** Real pass No loss	**Case C:** **Over-kill** Loss
	Fail	**Case B:** **Under-kill** Loss	**Case D:** Real fail No loss

  - Under-kill is due to the low coverage achieved for critical paths and the low frequency of the clock applied for the delay test.
  - Over-kill is due to the excessive usage of test vectors that test functionally untestable path. – i.e. a path not activated by any combination of instructions in a microprocessor.

- Over-kill and under-kill should be reduced as much as possible when a delay test is applied.

Delay test economics (cont'd)

- When the case a delay test is not applied is compared with the case it is applied, the loss of the manufacturing cost is expressed as:

$$\Delta LMC = \underbrace{N_D \cdot (PC + STC)}_{\text{waste of chips after packaging}} - \underbrace{(N_C \cdot UP}_{\text{waste of good chips}} + \underbrace{\sum_{i=A,B,C,D} N_i \cdot DTC)}_{\text{delay test cost}}$$

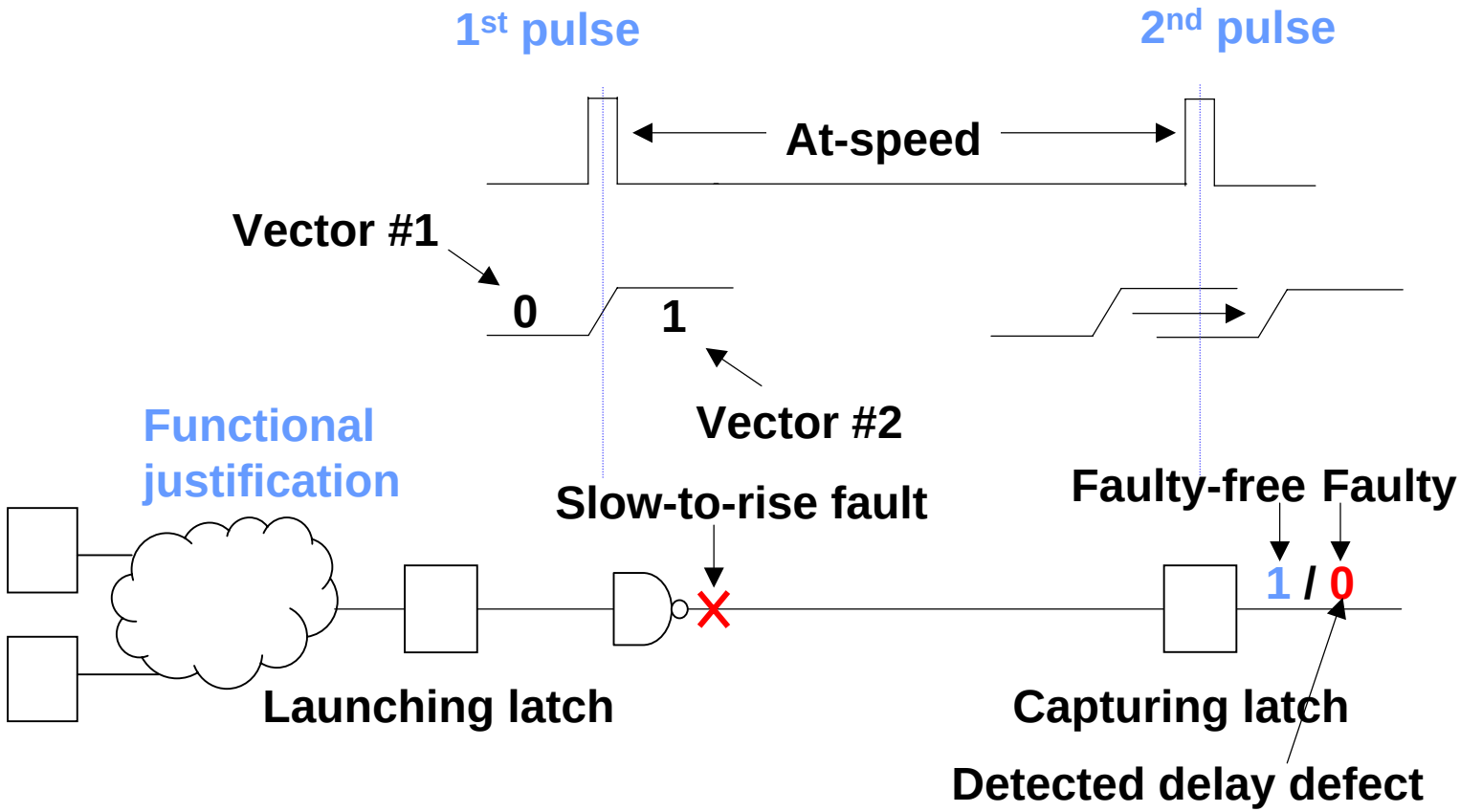
N_i : the number of chips categorized into case i
PC : Packaging cost
STC : System test cost
UP : Unit price
DTC : Delay test Cost

		Delay test	
		Pass	Fail
System test after packaging	Pass	**Case A:** Real pass	**Case C:** Over-kill
	Fail	**Case B:** Under-kill	**Case D:** Real fail

- Applying the delay test is beneficial only if ΔLMC is positive.

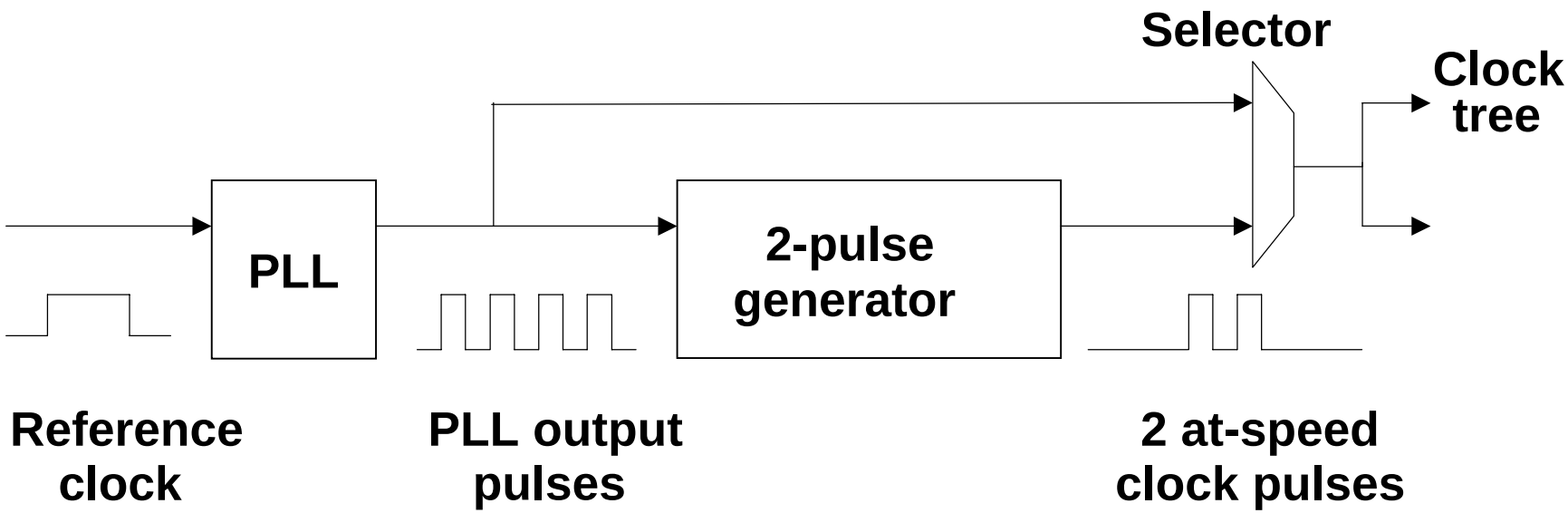
How is delay test performed?

- A delay Test is performed by two at-speed clock pulses.
- The second vector is set by functional justification.



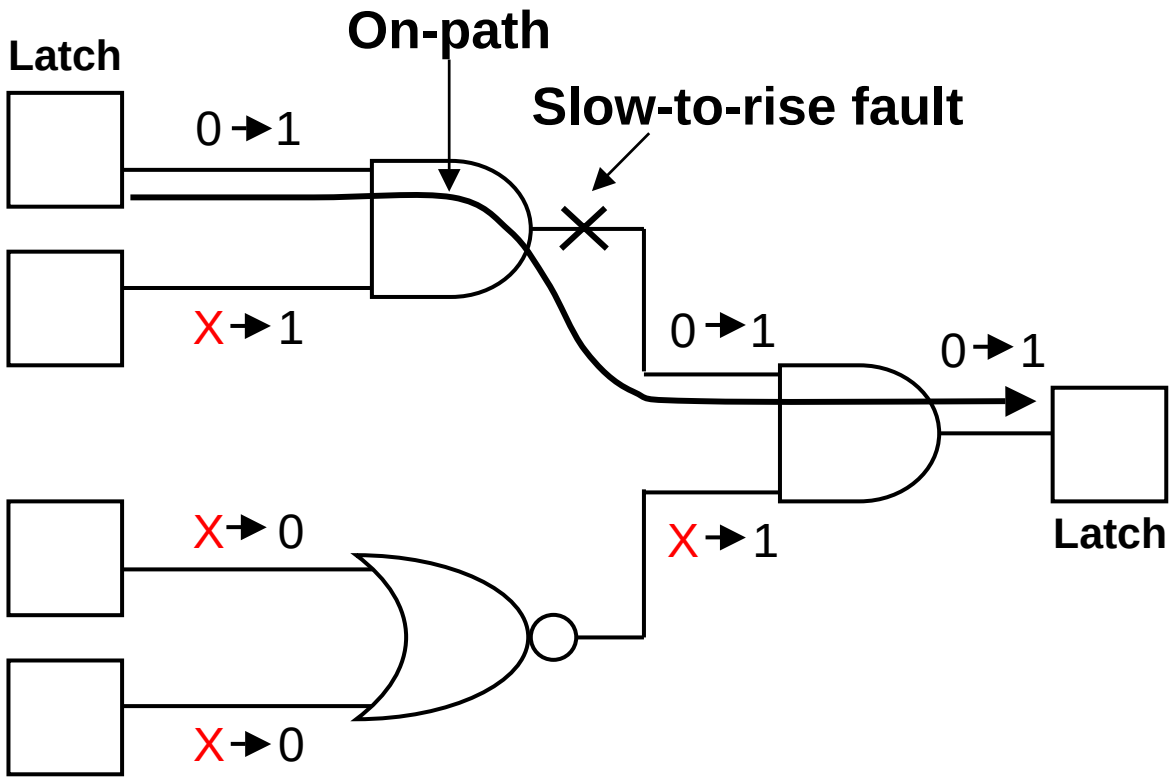
2-pulse generator

- The 2-pulse extractor extracts two consecutive pulses from the PLL output.
- The selector selects the PLL output or the 2-pulse extractor output.



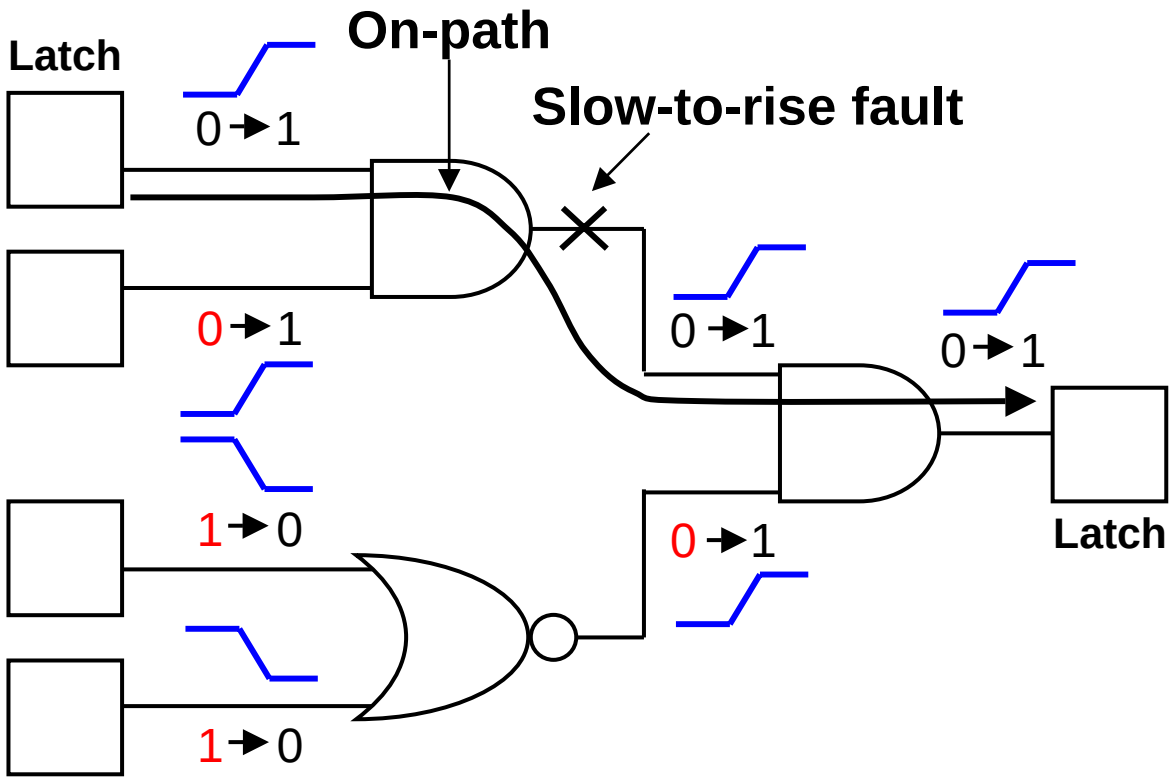
Detection of multiple delay faults

- A non-robust delay test is enough for screening.
- In a non-robust test, a state of off-paths before launching a transition is don't care.



Detection of multiple delay faults (cont'd)

- As many transitions as possible are generated at latches on off-paths.
- Dynamic compaction is used to implement this.



Detection of multiple delay faults (cont'd)

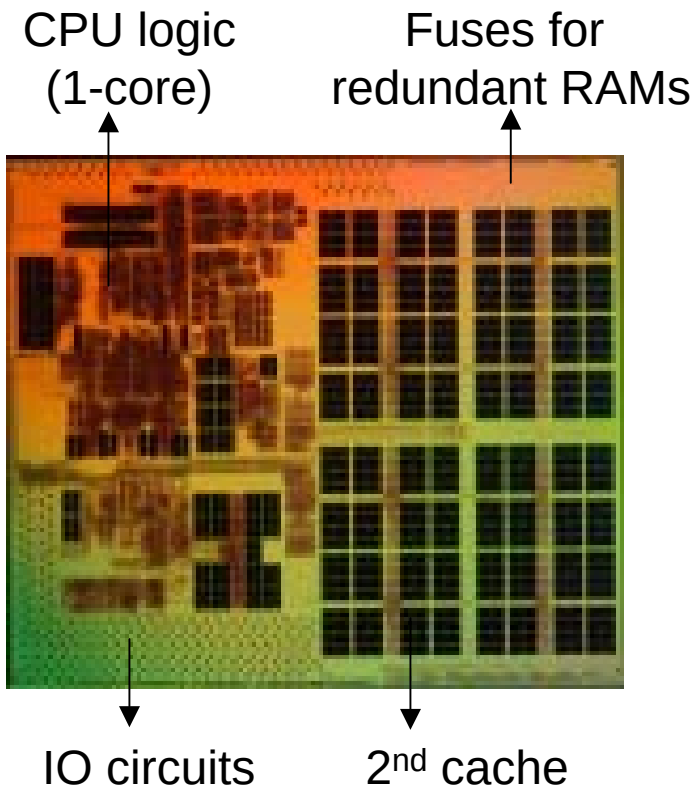
- By dynamic compaction technique, value 0 or 1 is assigned to off-path inputs at time t-1 to generate as many transitions as possible.

	On-path		Off-path					
			Our Method		Non-Robust		Robust	
Time frame	t-1	t	t-1	t	t-1	t	t-1	t
AND/NAND	0	1	A0	1	X	1	1	1
	1	0	X	1	X	1	1	1
OR/NOR	0	1	X	0	X	0	0	0
	1	0	A1	0	X	0	0	0

A0 (A1) means the value 0 (1) is selected if possible.

2.16GHz SPARC64 Microprocessor overview

- Chip die image



- Microprocessor profile

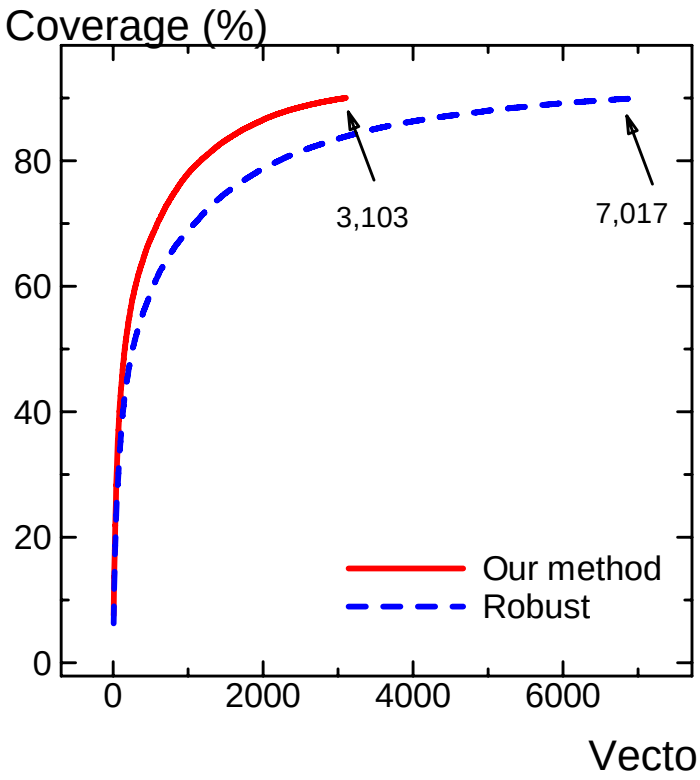
Process: 90nm, Cu metallization,
10 metal layers
Frequency: 2.16GHz
Die size: 18.46mm x 15.94mm
Transistor count: 400M
Level 2 on-chip cache: 4MB
I/O signals count: 279
Power dissipation: less than 65W

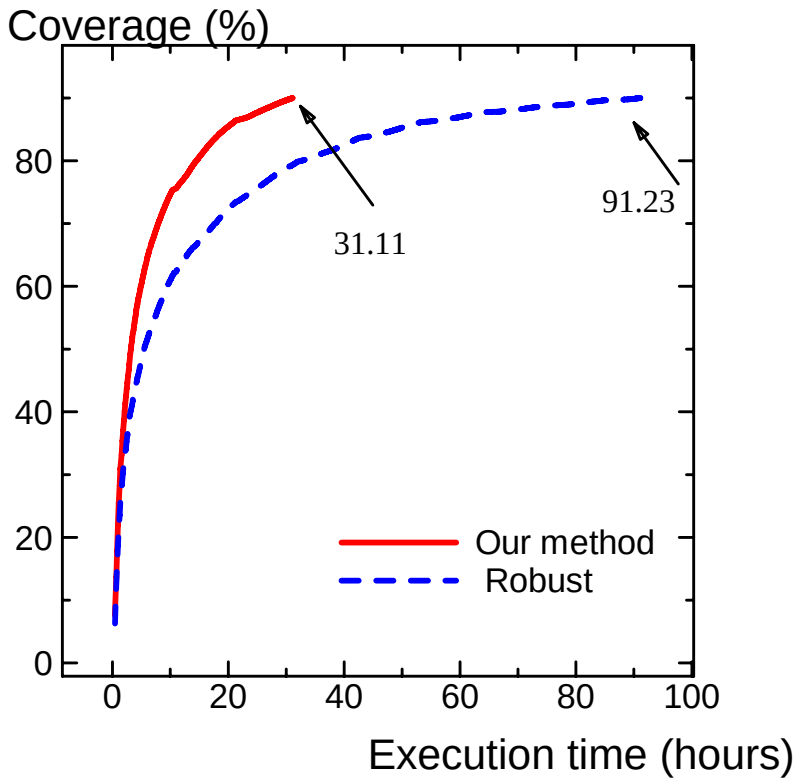
- DFT circuits

Scan clock: 2-phased clocks
Scan chain count: 16
Scan latch count: 238,620
Additional circuits: TPCM, 2-pulse generator, RBIST

Delay test coverage

- A robust test requires twice the number of test vectors and three times longer to reach the same coverage.





- A robust test is not practical for screening delay defects.

Screening results

- The screening ratio for the total actual defective chips is 5.0% when a delay test is applied as follows:
  - Speed: 1.5GHz (70% of the target chip frequency)
  - Voltage: the normal operating voltage
  - # of tested chips: about 4,000
- For the above good chips, we applied a delay test at a lower voltage. Then, regardless of the result, the system test is performed.

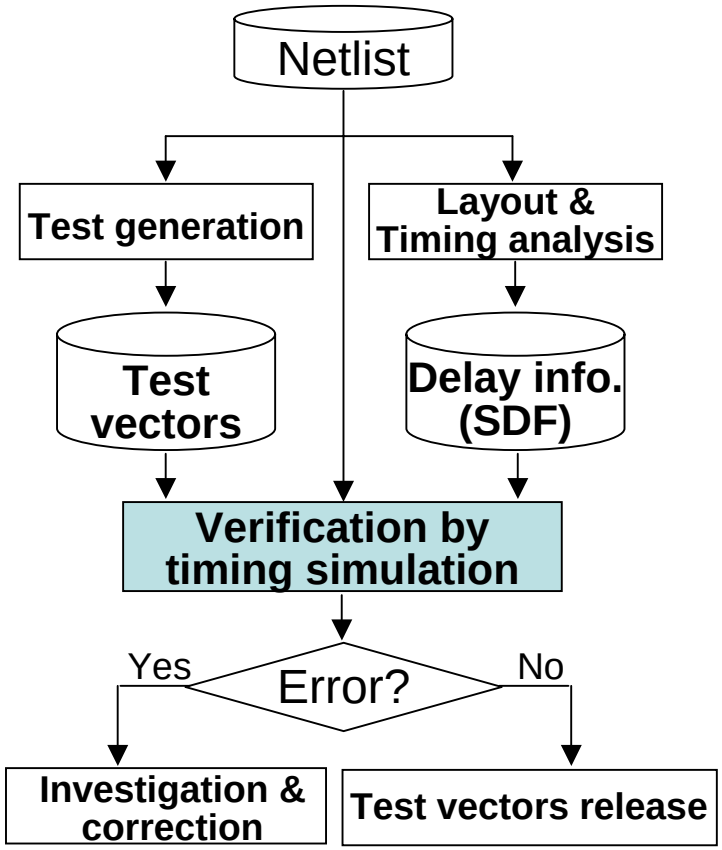
Under-kill Over-kill

		Delay test		Total
		Pass	Fail	
System test after packaging	Pass	98.3%	1.7%	100%
	Fail	53.3%	46.7%	100%

About half of fails in system test can be detected by a delay test in advance!

Paths covered by a delay test

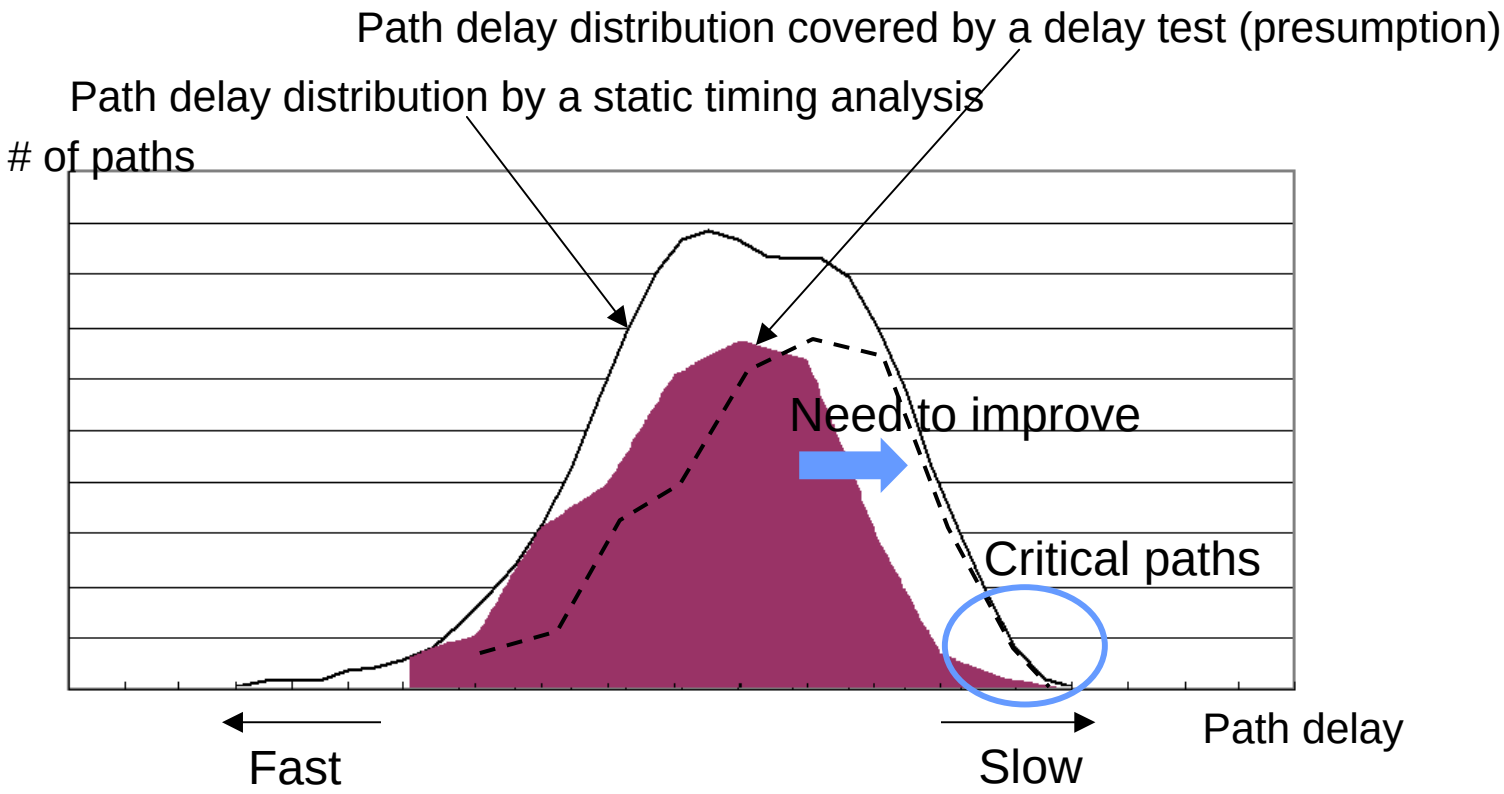
- Test vector verification flow



- Verification by varying a strobe time
  - If the simulated values of latches are different than the expected values, the applied vector tests a path slower than the frequency corresponding to the strobe time.
  - We performed the verification several times using different values for the strobe times; we used frequencies both lower and higher than the target frequency.

Paths covered by a delay test (cont'd)

- Our delay test covers paths in each frequency to some extent.
- The coverage of critical paths should be improved.



Statistics of test generation and verification of tests

- It took about 2 weeks to generate test vectors and to verify them including a delay test.
  - Generation (1 CPU is used in 1.3GHz UNIX server)

Test	# Faults	# Vectors	Coverage	Time (Hours)
SCAN	9,059,216	14	99.9%	0.22
FUNCTION	21,803,669	2,014		14.15
RBIST	N/A	N/A	N/A	0.12
DELAY	9,750,387	3,103	90.0%	31.11

  - Verification (12 CPUs are used in 2.4GHz IA server)

Test	Verification (Hours)	Relative Verification Time
SCAN	101.02	2.9%
FUNCTION	16.80	0.5%
RBIST	3,346.04	96.1%
DELAY	16.24	0.5%

Conclusions

- Conclusions
  - Our delay defect is successfully applied to 2.16GHz SPARC64 microprocessor for screening out delay defects.
    - The screening ratio for the total actual defective chips is 5.0% now.
    - About half of fails in system test will be detected by a delay test in advance if it is applied at a lower voltage.
- Future work
  - To increase the coverage of critical paths, we are enhancing our delay test to cover more critical paths combined with path-base test.