THETA EDA

Delay Variation Tolerance for Domino Circuits

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Outline

- The delay variation problem in domino circuits
- Duplex system
- Re-synthesis for delay variation tolerance
- Experimental results & conclusion

Delay Variation Problem

- Circuit delay is increasingly sensitive to
  - process variation
  - delay defect
  - noise effects (crosstalk and IR drop)

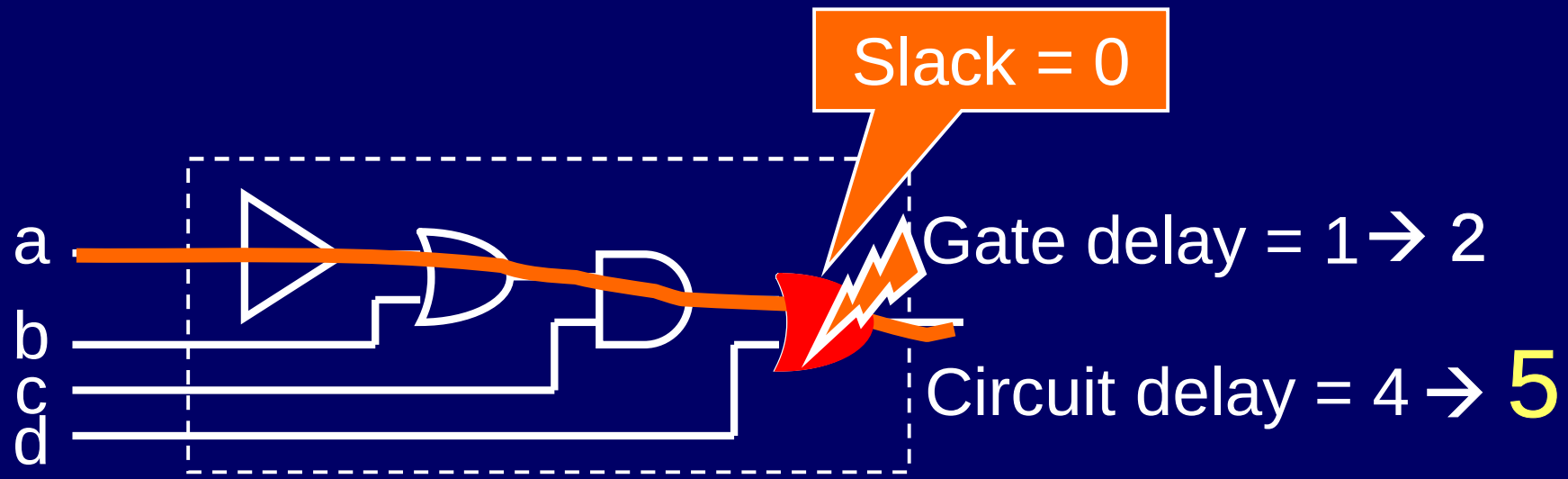
- Cause a circuit's delay to fluctuate, and in the worst case, to violate timing requirement.

Delay Tolerance for Domino Circuits

- High performance designs are normally susceptible to delay variation.
- Domino circuits are usually adopted to implement high performance designs.
- Important to develop delay variation tolerance for domino circuits.

Delay Variation Tolerance

- Slack has strong correlation with delay variation tolerance.

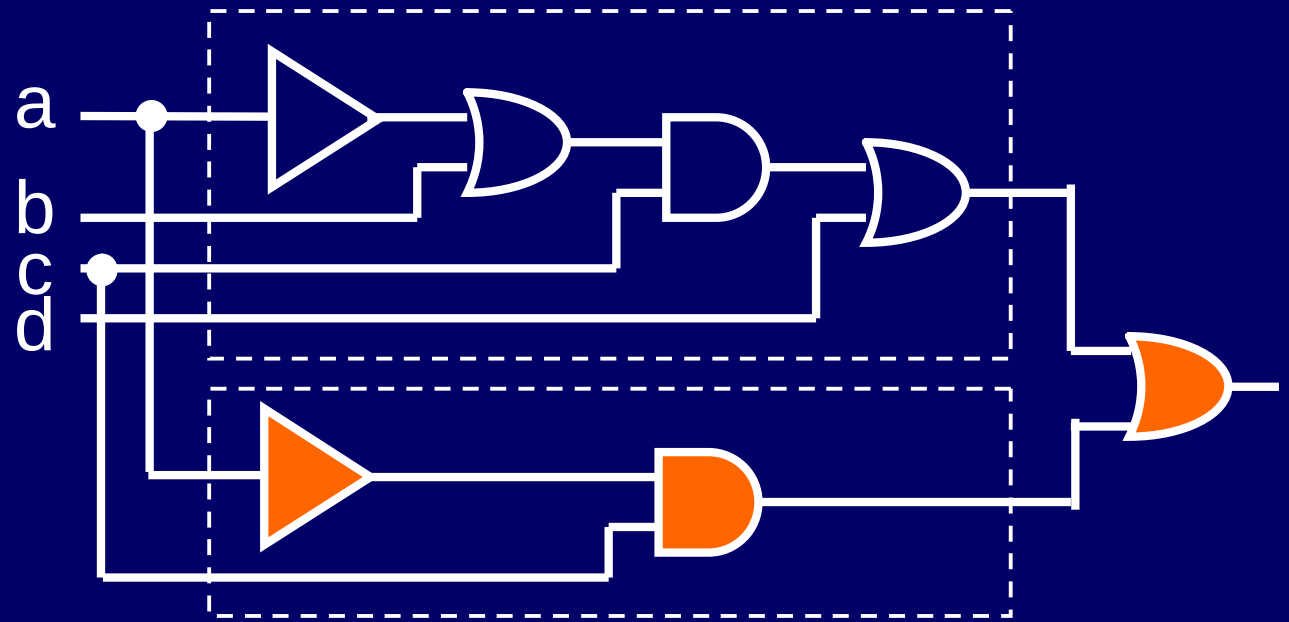


Objectives

- Slacks are normally used for area and power minimization ➔ no slacks available.
- Objectives:
  - NOT timing optimization to increase slacks. Assume a circuit is well optimized for timing.
  - Add redundancy to increase slacks with very minor impact in timing.

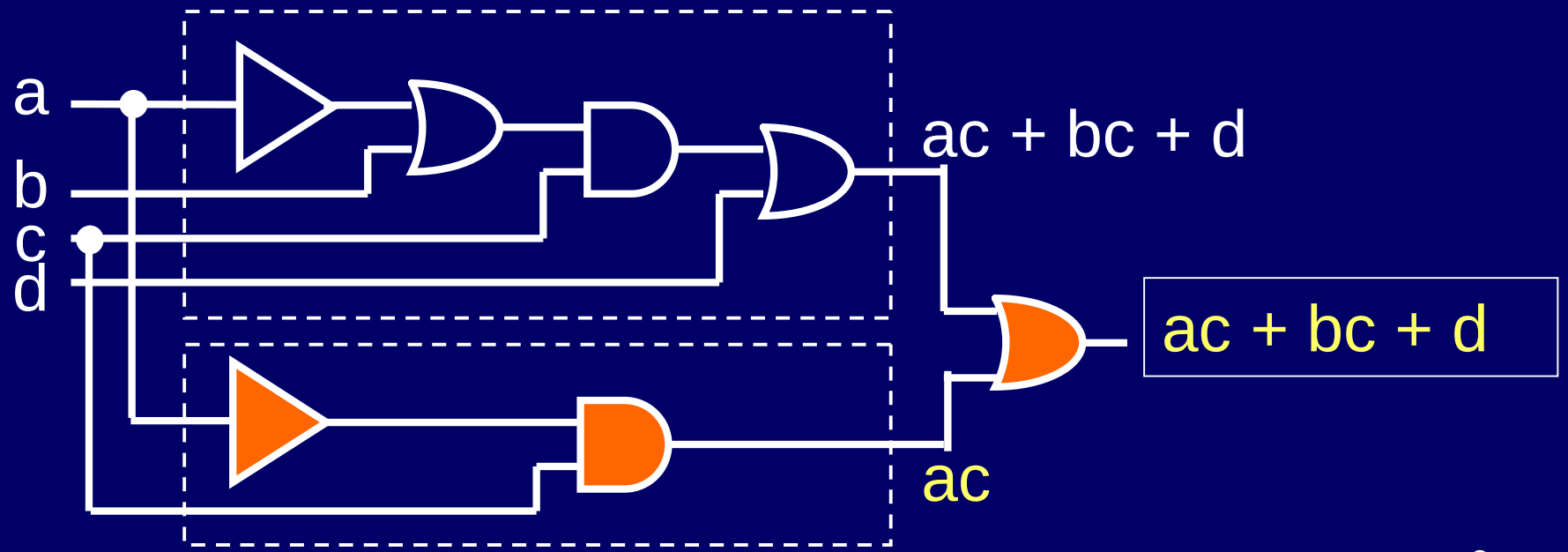
Basic Idea

- Add redundancy.



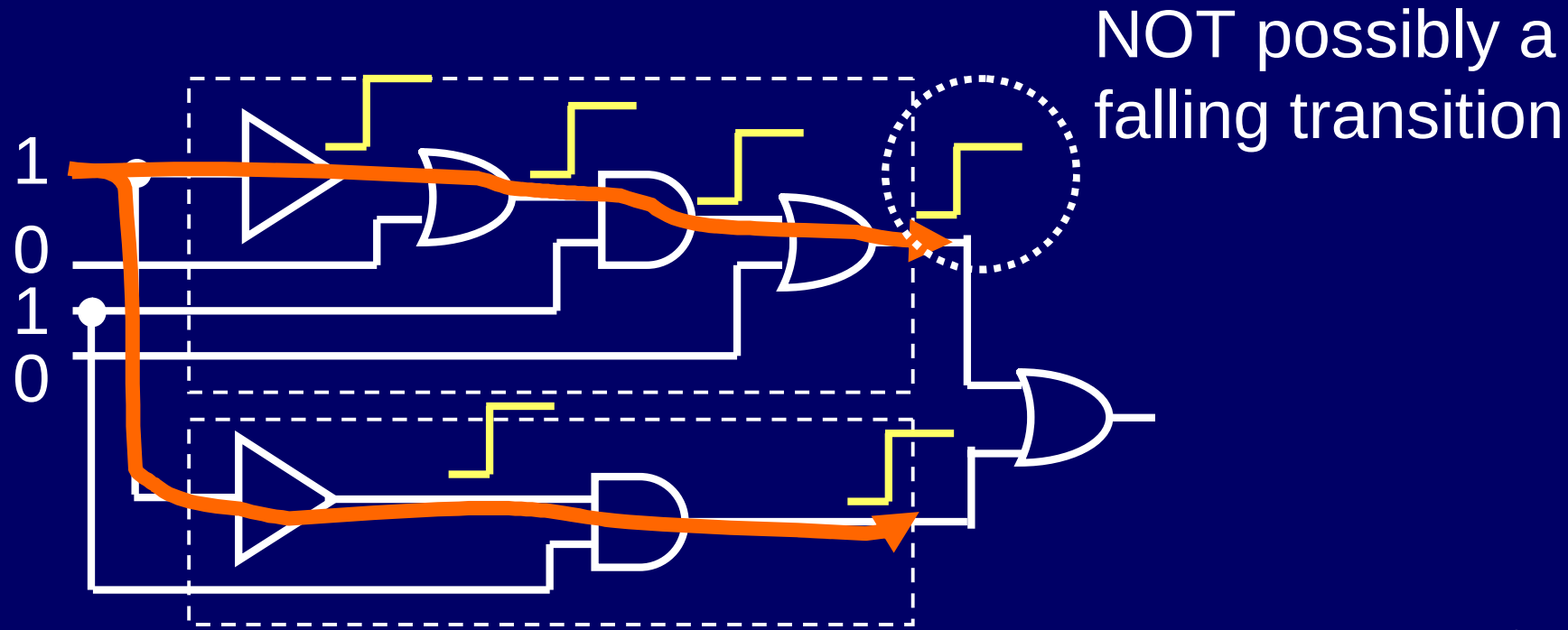
Function Not Changed

- The on-set of the appended function is covered by that of the original function.



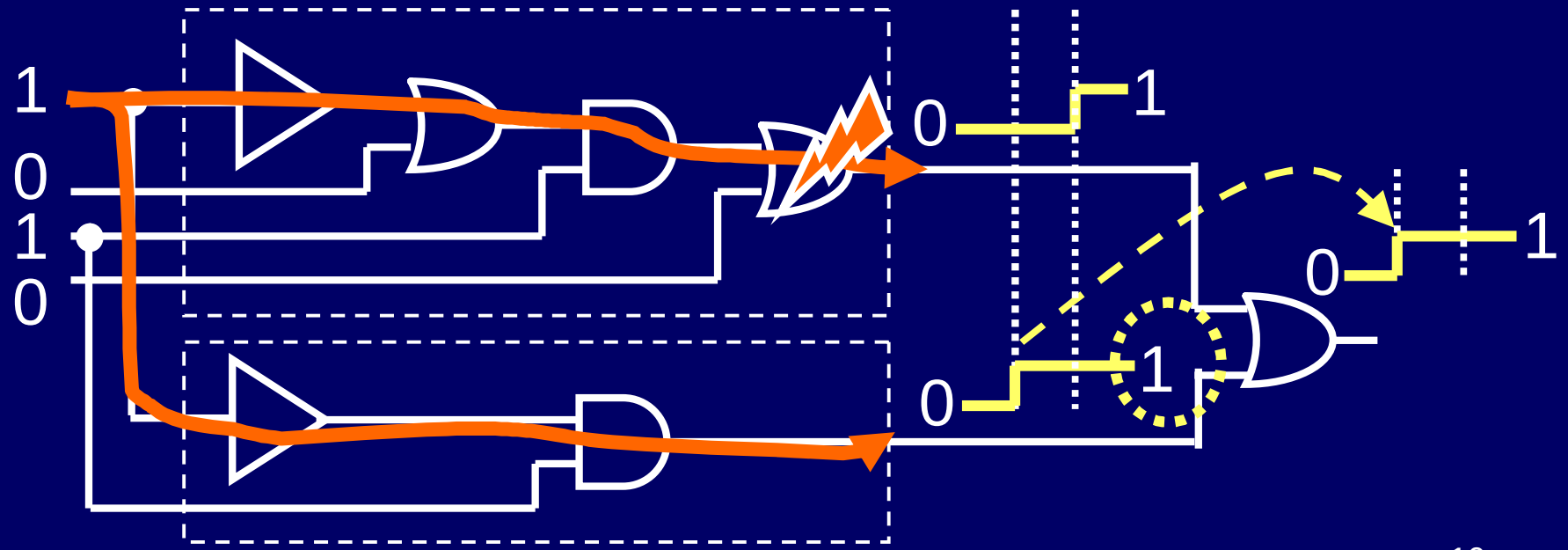
Slacks Increased (1/2)

- When the critical path is activated, both the two circuits produce a rising transition.



Slacks Increased (2/2)

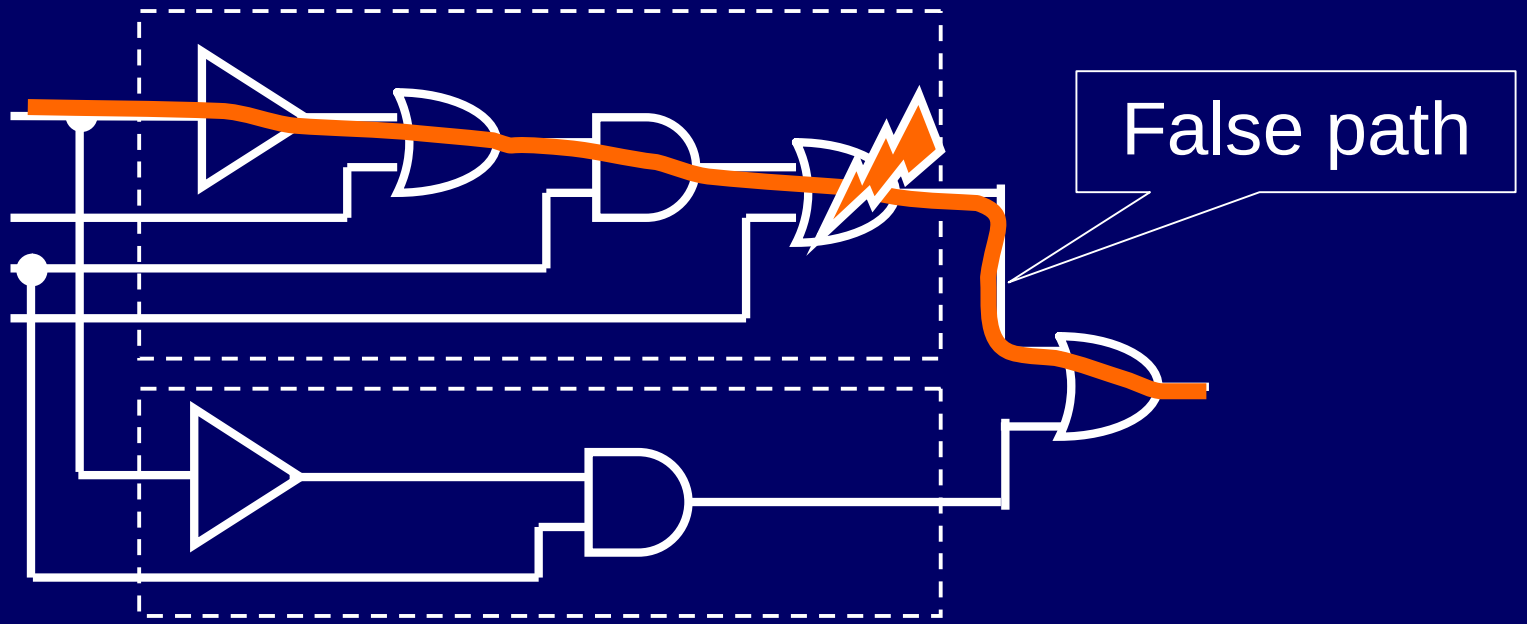
- The early transition must determine the circuit delay.
- The late transition does not affect the delay.



Slacks Increased (2/2)

- For all input vectors activating the critical path, the appended circuit produces a 1.

  ➔ Slacks are increased.



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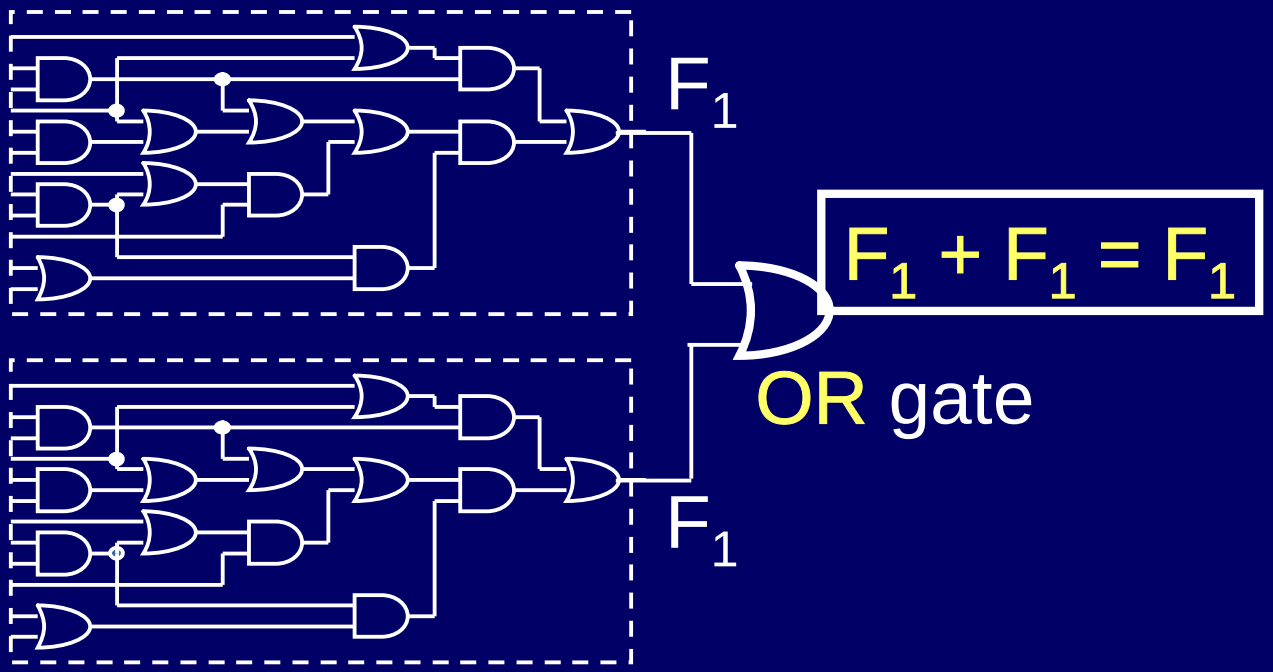
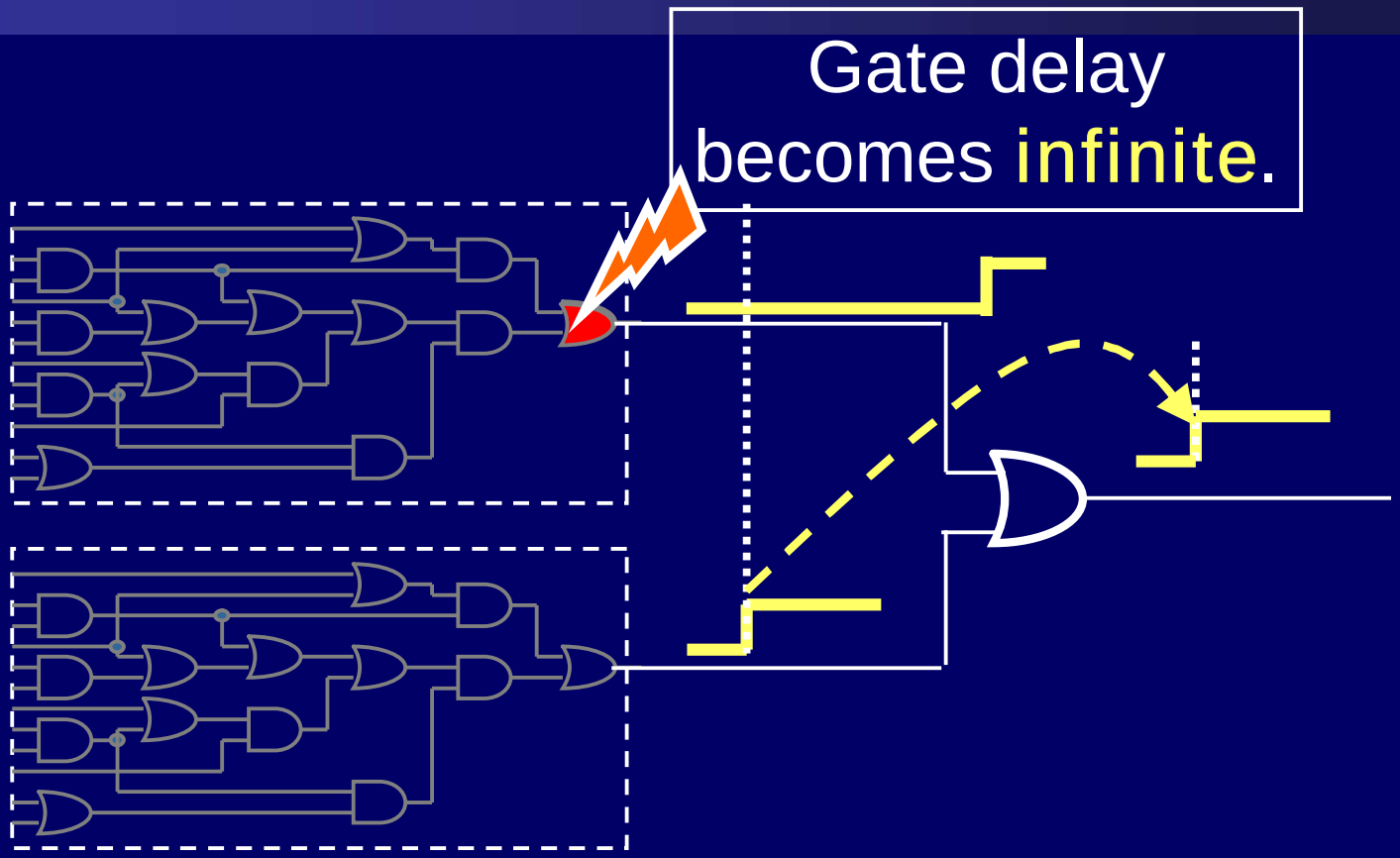
A Duplex System



- Has the same function.
- Has larger delay variation tolerance.

Infinite Slack



- All gates in the two blocks have infinite slacks.

Duplex System Impractical

- In a duplex system, the slack is infinite.
  - Over-protective for delay variation
    - Delay variation is 10%~20% of the original circuit delay.
  - About 100% area overhead.

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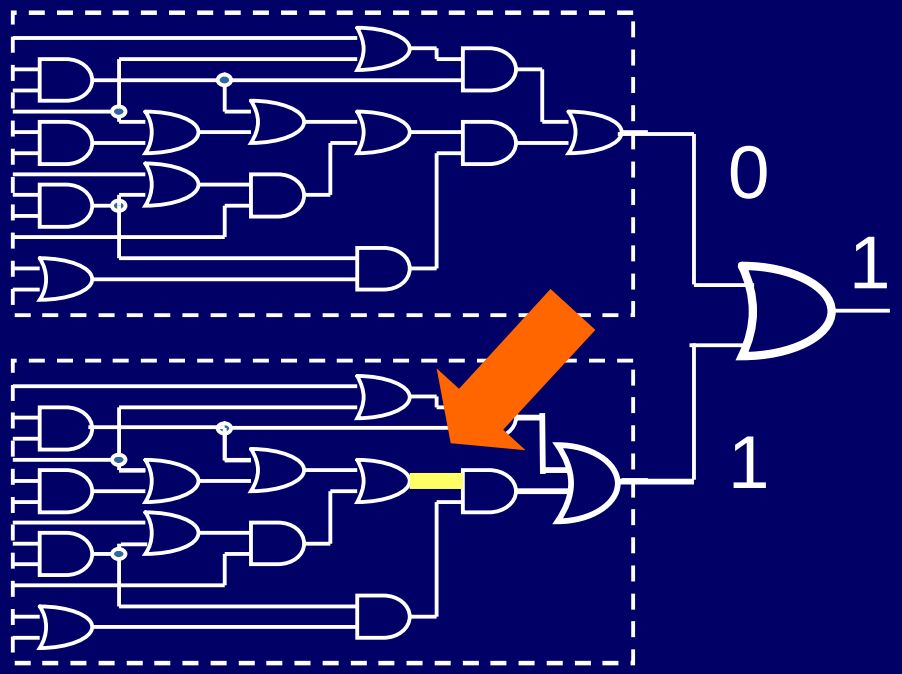
Wire Removal

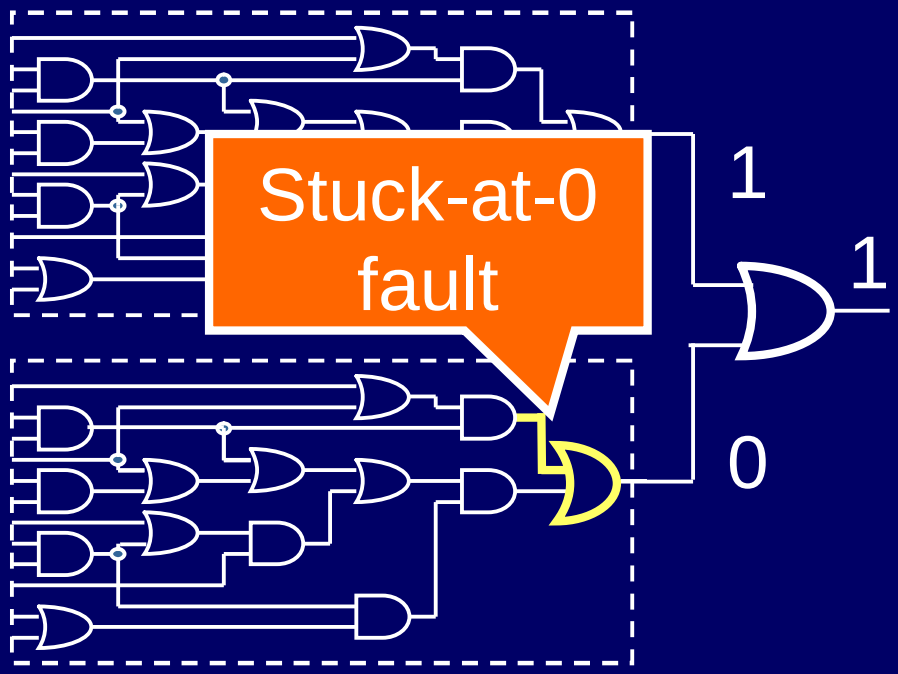
- Remove redundant wires to reduce area overhead.
- Some wires are not redundant.



Redundant Wires

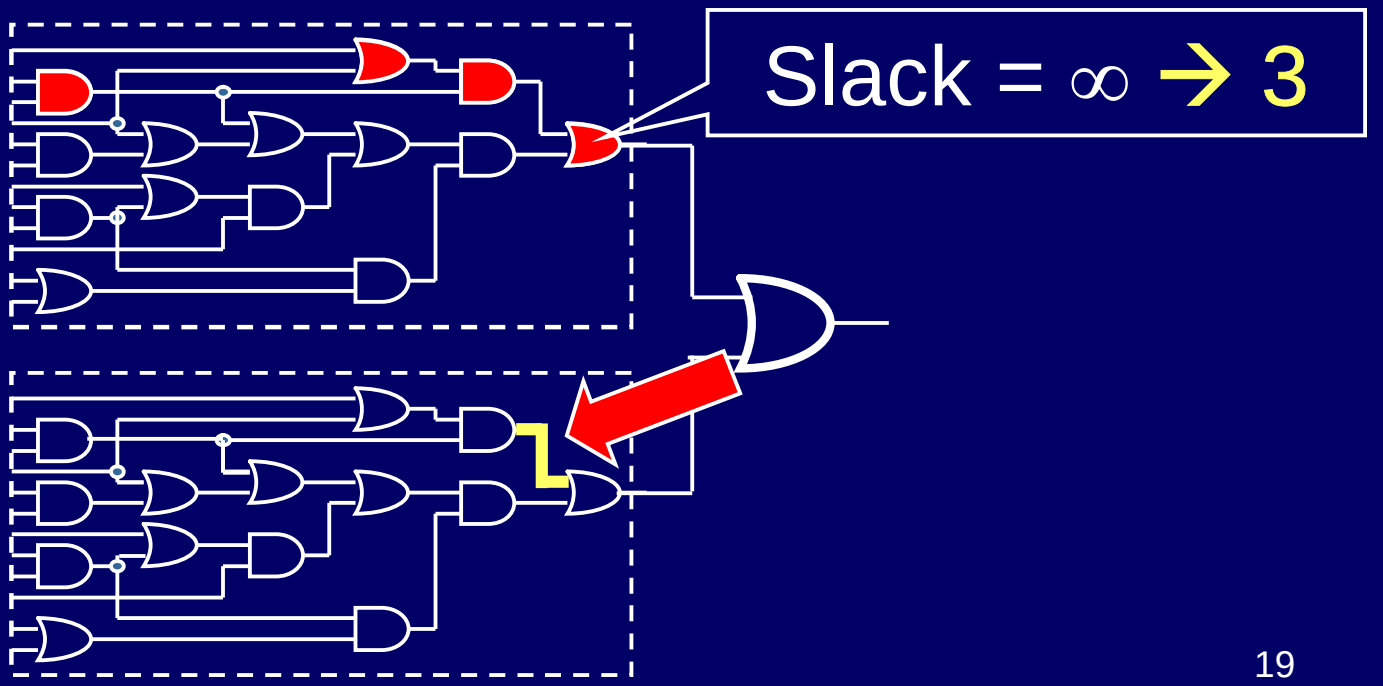
- Lemma:

  Input wires to OR gates in the appended circuit are redundant and can be removed simultaneously.



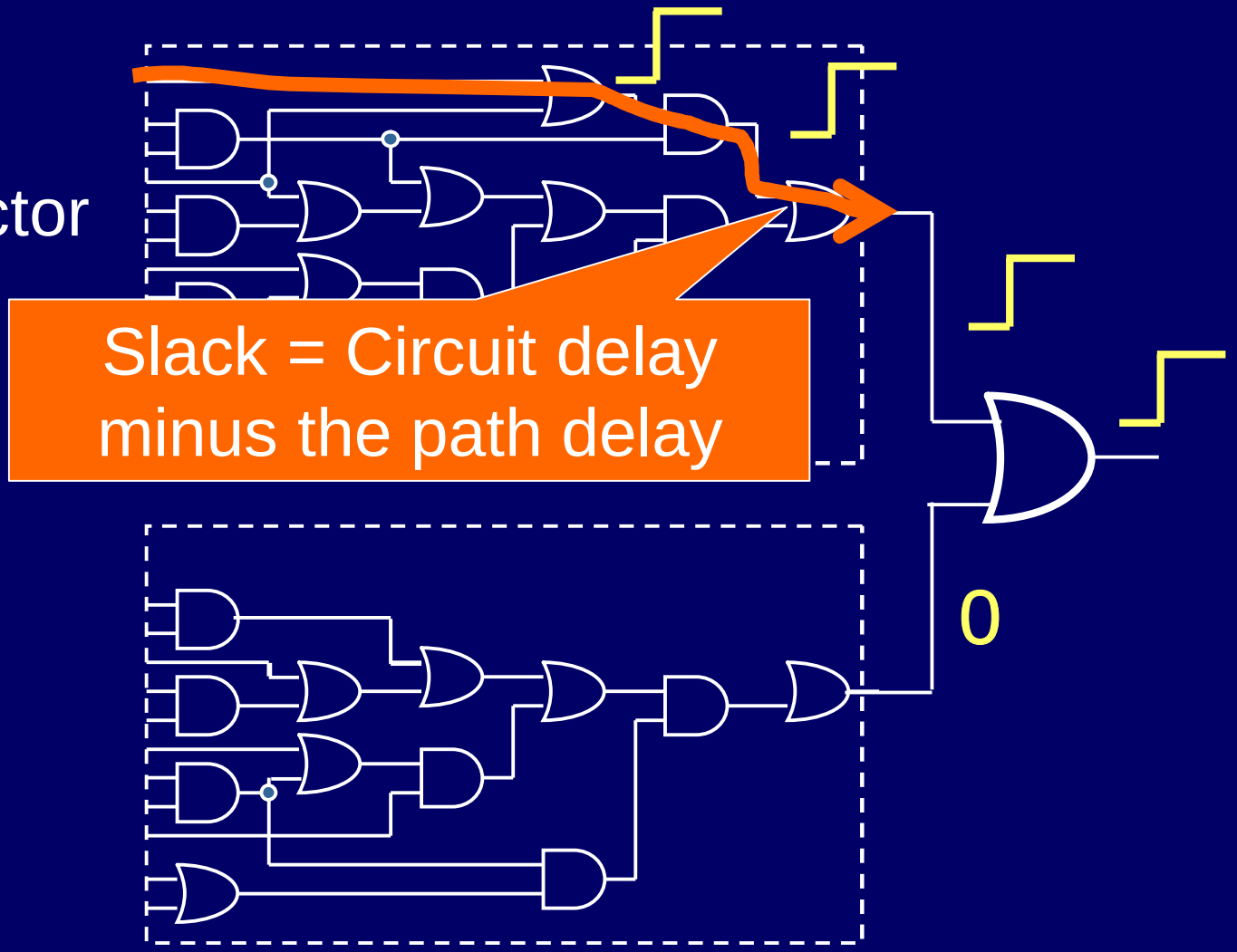
Slacks Decreased (1/2)

- After removing redundant wires, some slacks may decrease.



Slacks Decreased (2/2)

Exist an input vector



Problem Formulation

- Let the slacks of all gates at least a certain level.

- Given a d_t value, we remove redundant wires keeping the slacks at least d_t.

Wire Removal Theorem

- Theorem

  For a domino circuit, a wire in the duplication circuit can be removed if its corresponding wire in the original circuit is

  1. a d_t-side input wire,
  2. connected to an OR gate, and
  3. free from AND converging nodes in its transitive fanouts.

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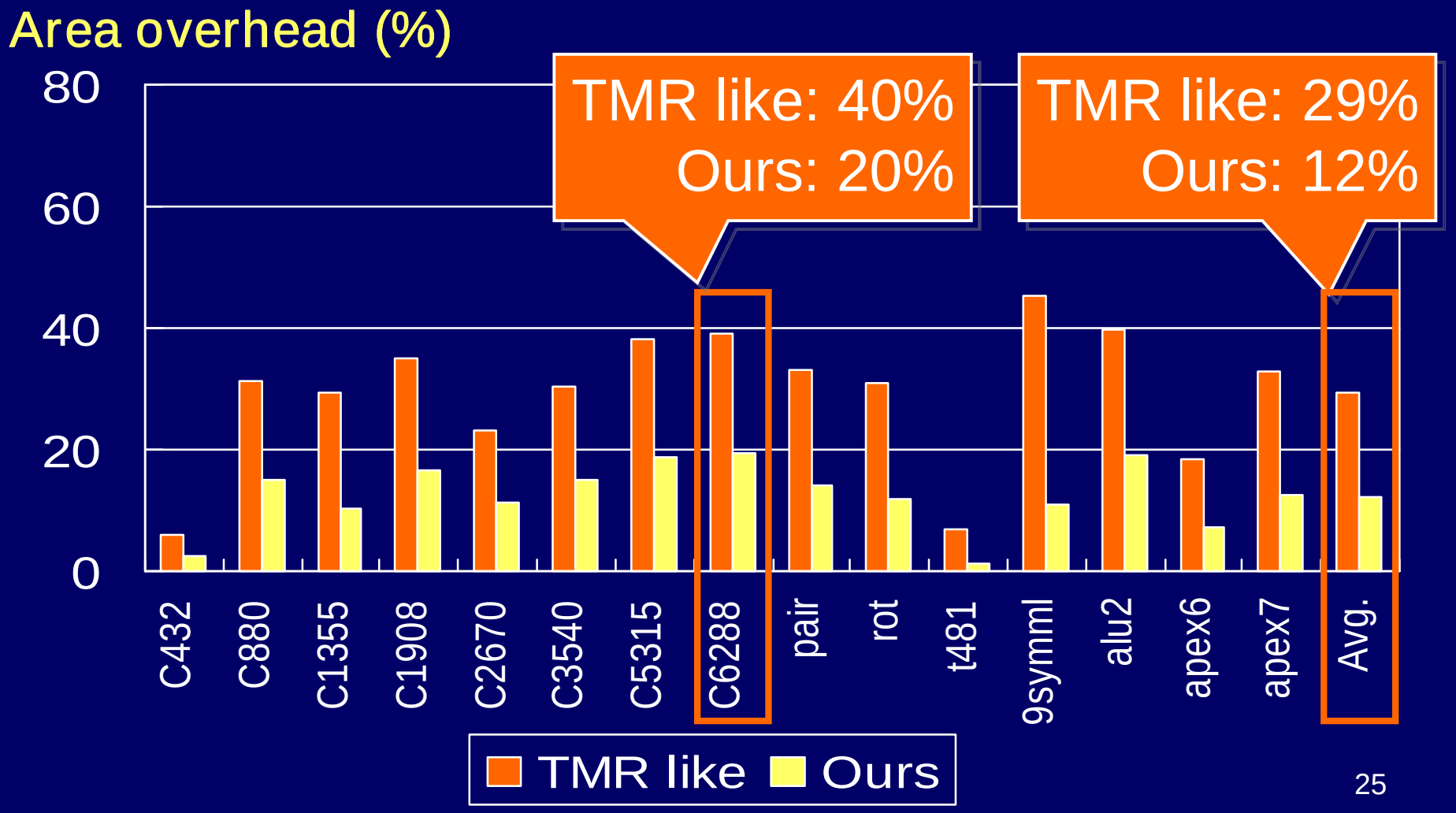
Experimental Flow

- Optimize benchmarks by script.delay in SIS.
- Re-synthesize circuits using
  - TMR like structure [S.C. Chang, et al. DAC'04]
  - Our duplex like structure
- Set the slacks at least 10% * the circuit delay.

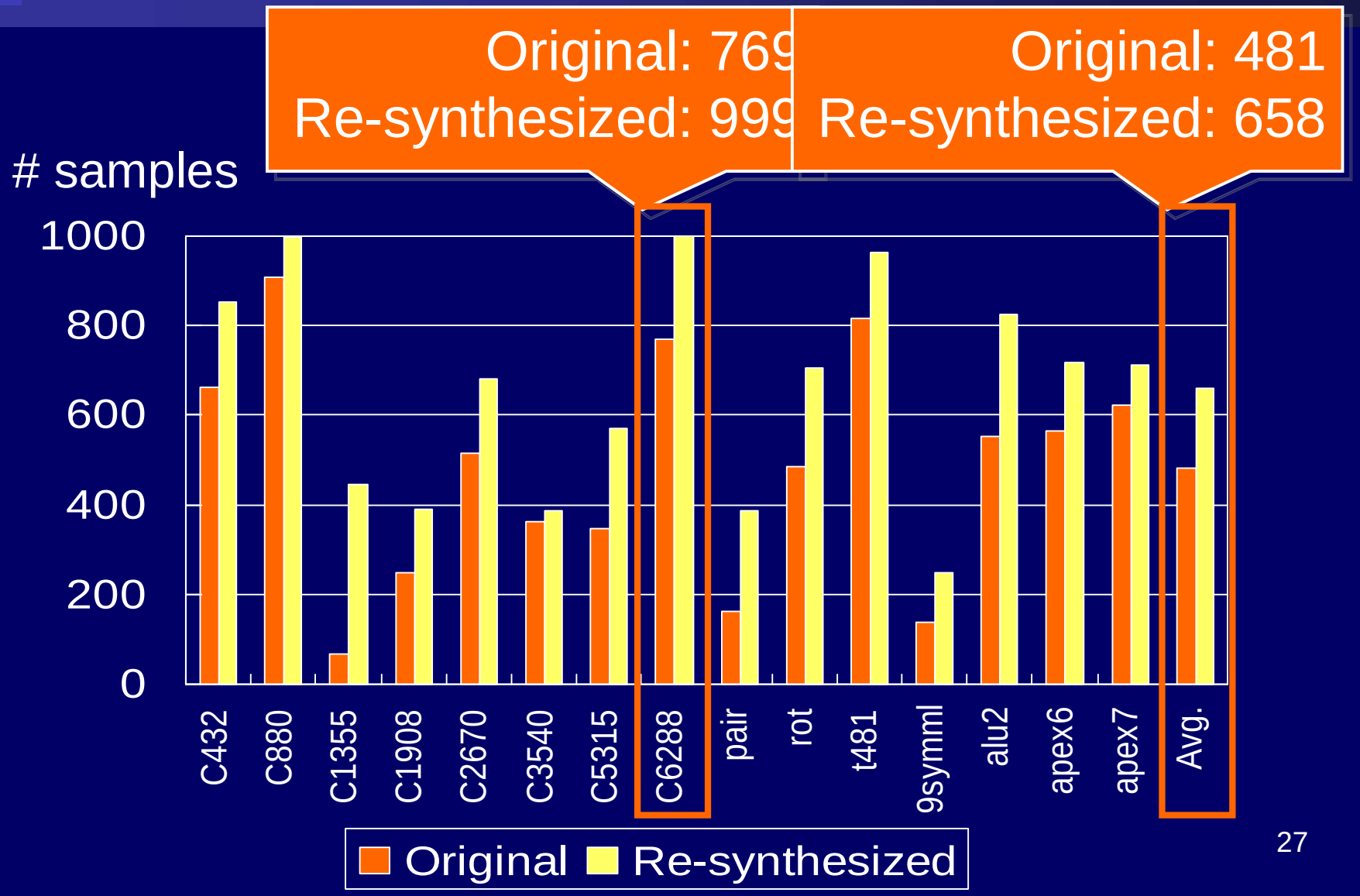
Experimental Results (d_t=10%)



Statistical Analysis

- Monte-Carlo experiments to demonstrate the effect of delay tolerance.
- Assume gate delay is a probability density function as described in [Liou DAC'02].
- Run Monte-Carlo to generate 1000 samples for both a circuit and its re-synthesized circuit.
- Count the number of samples whose delay satisfies a pre-defined delay requirement.

Statistical Analysis



Conclusion

- Re-synthesize a given domino circuit for d_t delay tolerance.
- 12% area overhead for 10% delay tolerance.

Thank you!