Efficient Identification of Multi-Cycle False Path

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Abstract

- Address the timing analysis problem by considering both single-cycle and multi-cycle operations
- Provide the precise definition of multi-cycle false paths and the necessary conditions for multi-cycle sensitizable paths
- Propose a segment-based algorithm to identify multi-cycle false paths
- Propose an iterative method to compute valid clock period
- Demonstrate the improvement in clock frequency by taking multi-cycle false paths into account

Outline

- Motivation
- Previous Work
- Multi-Cycle Path
- Necessary Conditions for Path Sensitization
- Identification of Multi-Cycle False Paths
- Valid Clock Period
- Experimental Result
- Conclusion

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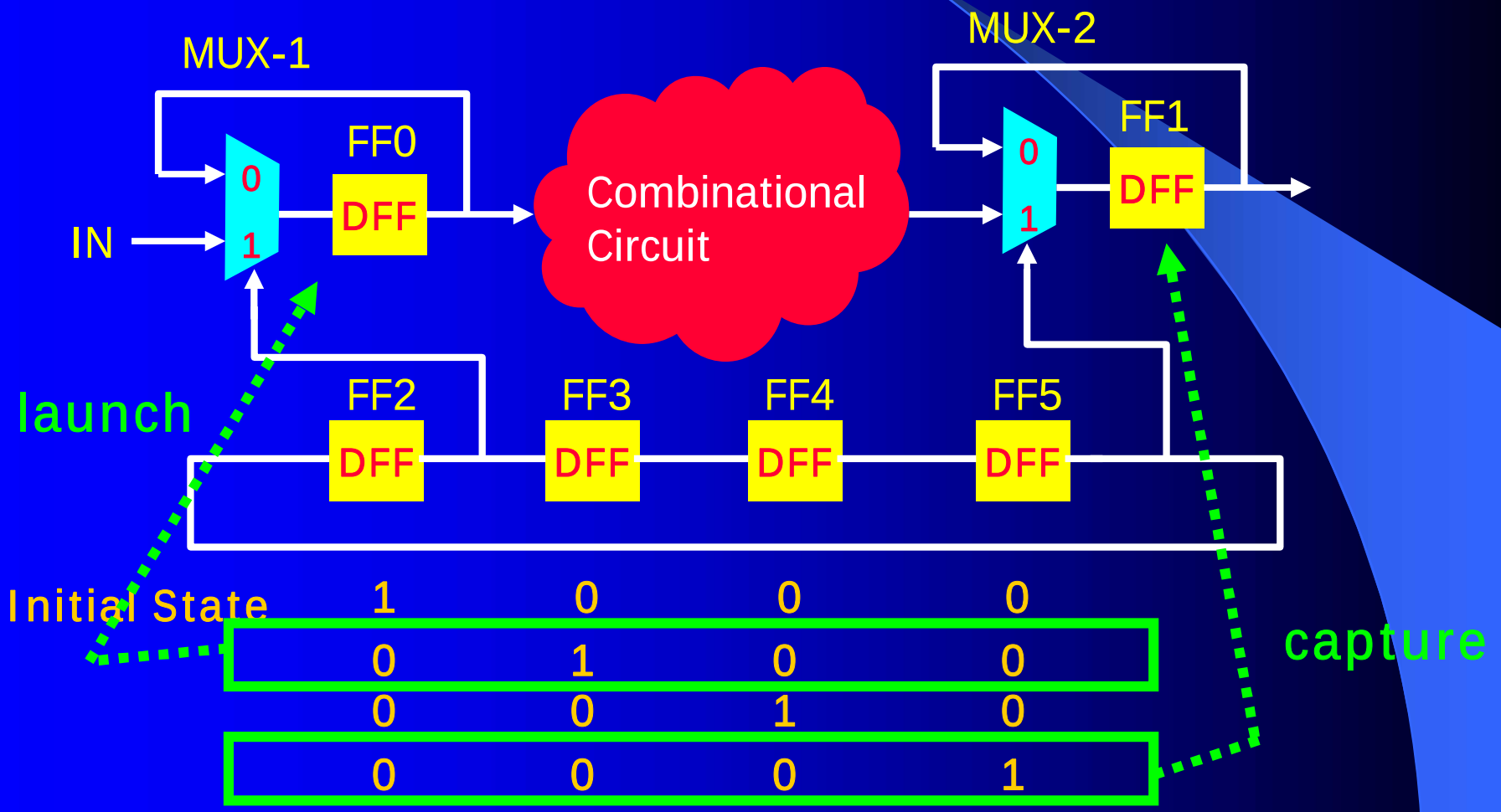
Motivation

- Clock period is determined by the delay of the longest path in the circuit
- Utilizing only topological delay to determine the clock period could be too conservative
  - False path
  - Multi-cycle path
- A multiple-cycle path in a sequential circuit is a combinational path which does not have to complete the propagation of the signals along the path within one clock cycle

Motivation (cont.)

- 3-cycle multi-cycle operation



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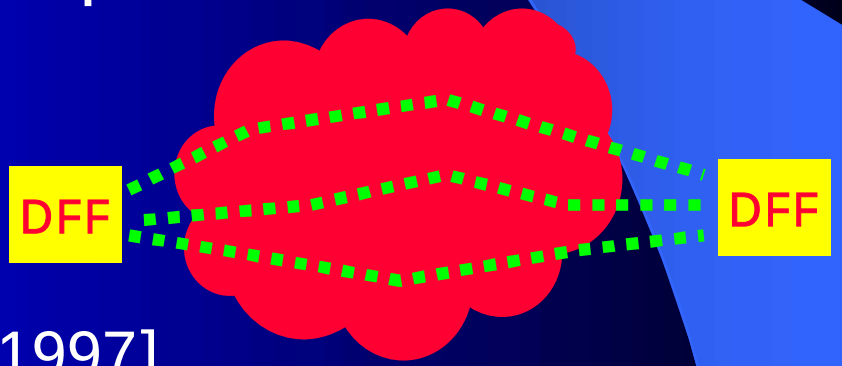
Previous Work

- Define: multi-cycle flip-flop pair

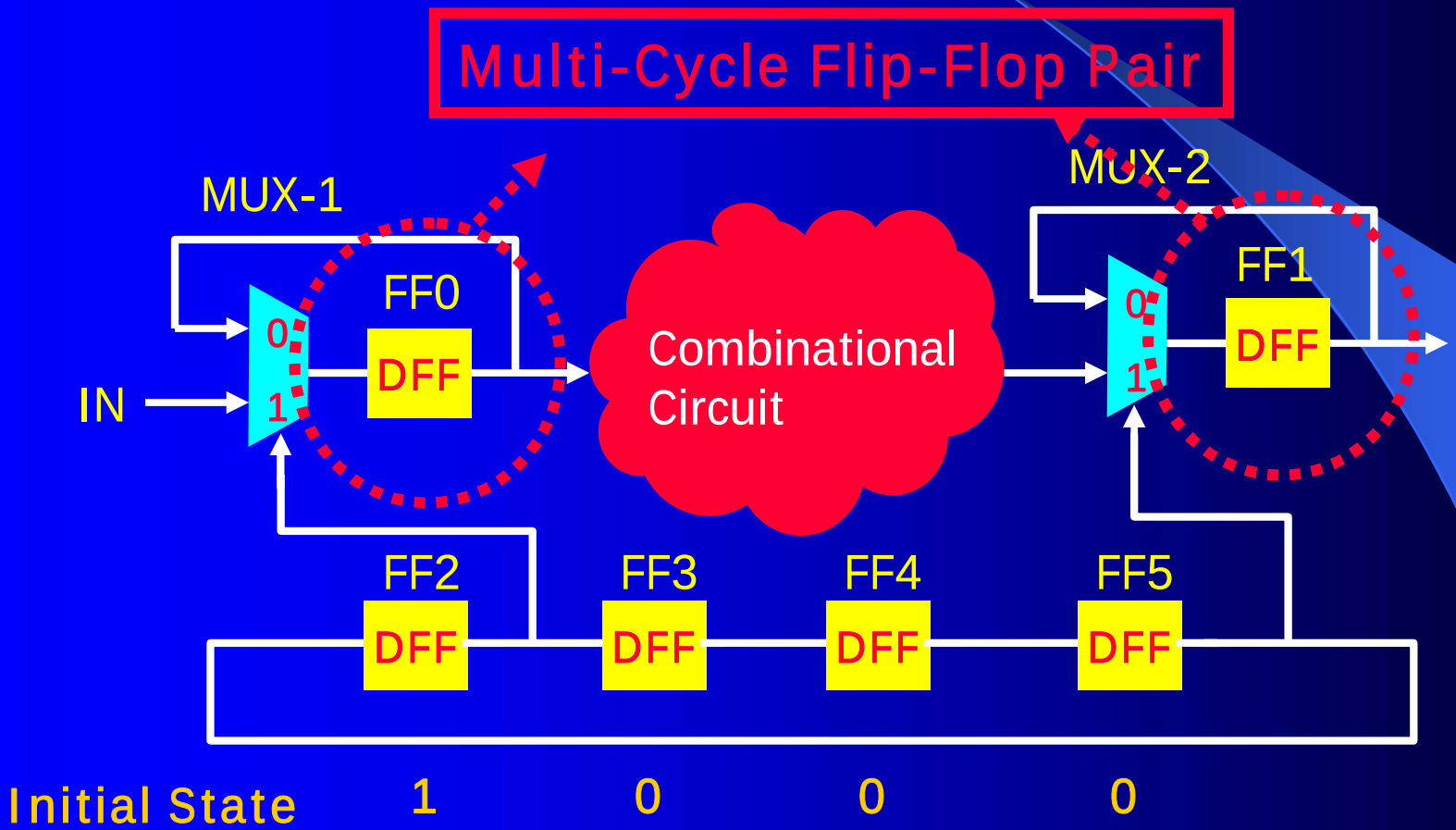
$$FF_i(t) \neq FF_i(t+1) \Rightarrow FF_j(t+1) = FF_j(t+2)$$

- All paths between multi-cycle flip-flop pairs are then declared as multi-cycle paths



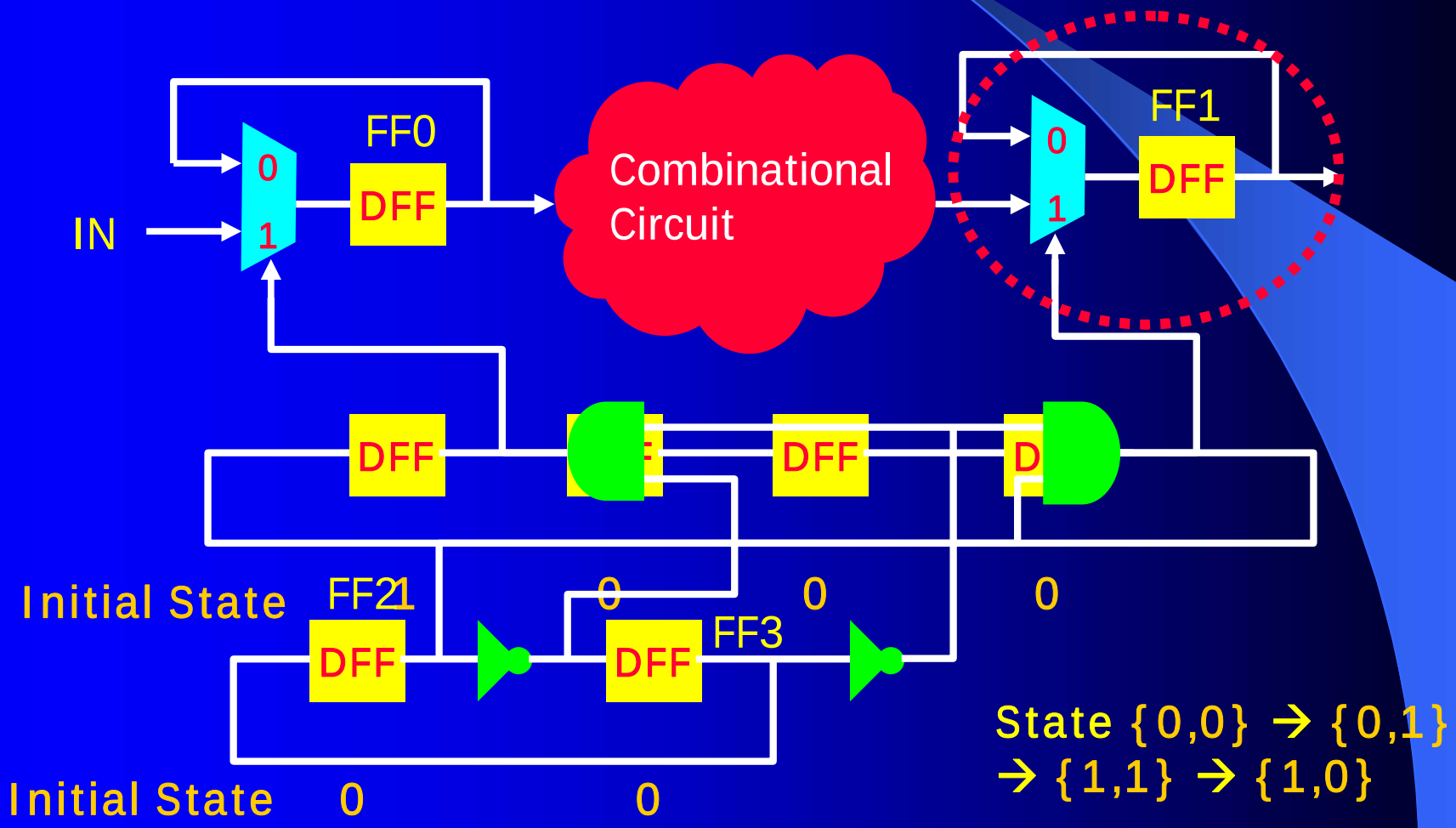
- Stable state checking
  - BDD [K. Nakamura, ICCAD-1997]
  - SAT [K. Nakamura, IEICE-2000]
  - ATPG [H. Higuchi, DAC-2002]

Multi-Cycle Flip-Flop Pair Example

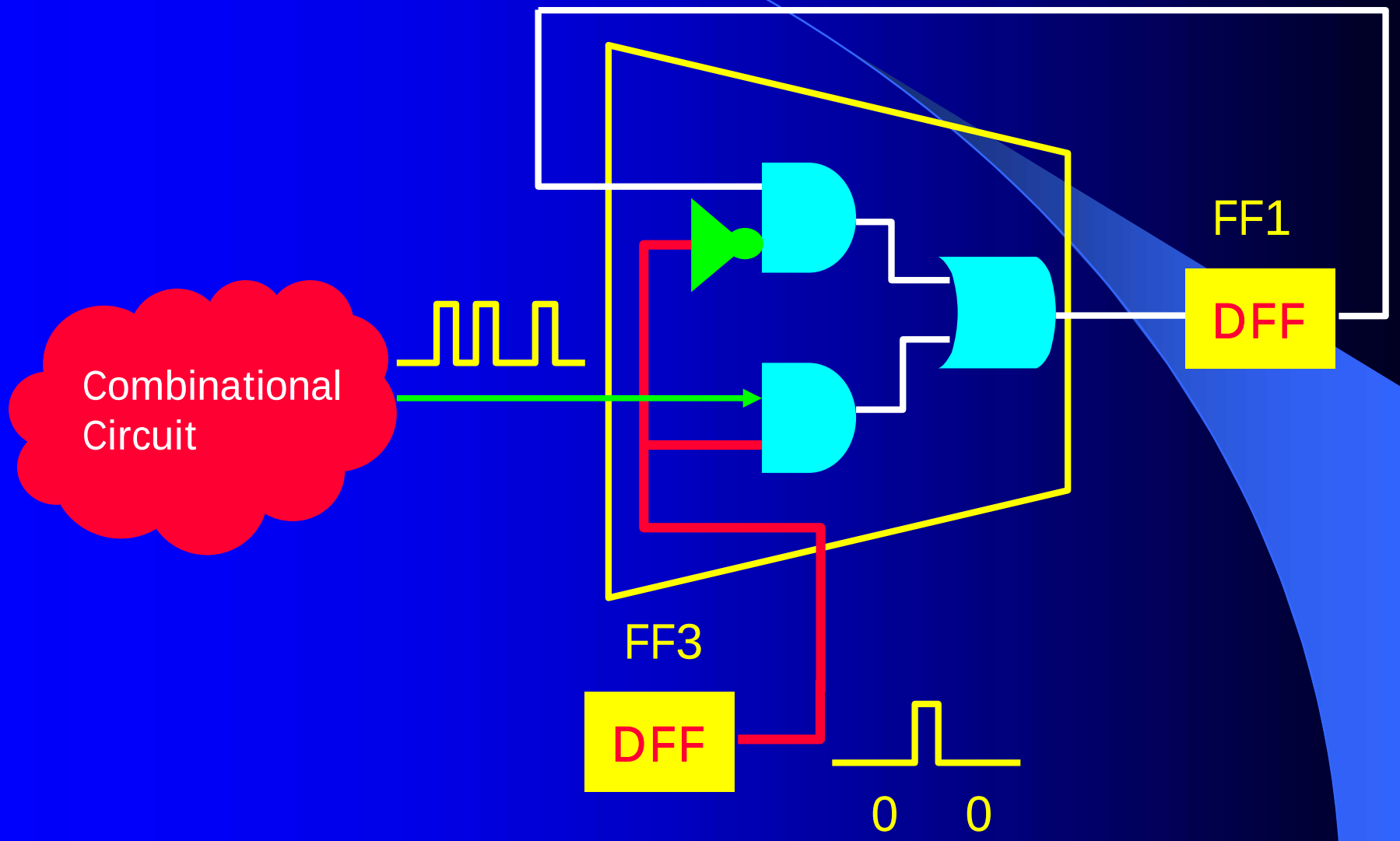


Invalid Clock Calculation

- Stable state checking might not result in correct classification of multi-cycle flip-flop pairs due the presence of static-hazard [H. Higuchi 2002]



Static-Hazards Problem



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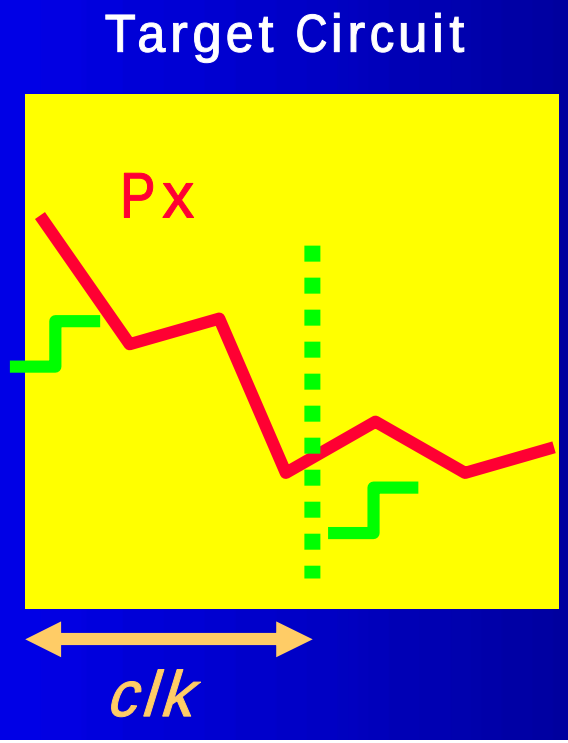
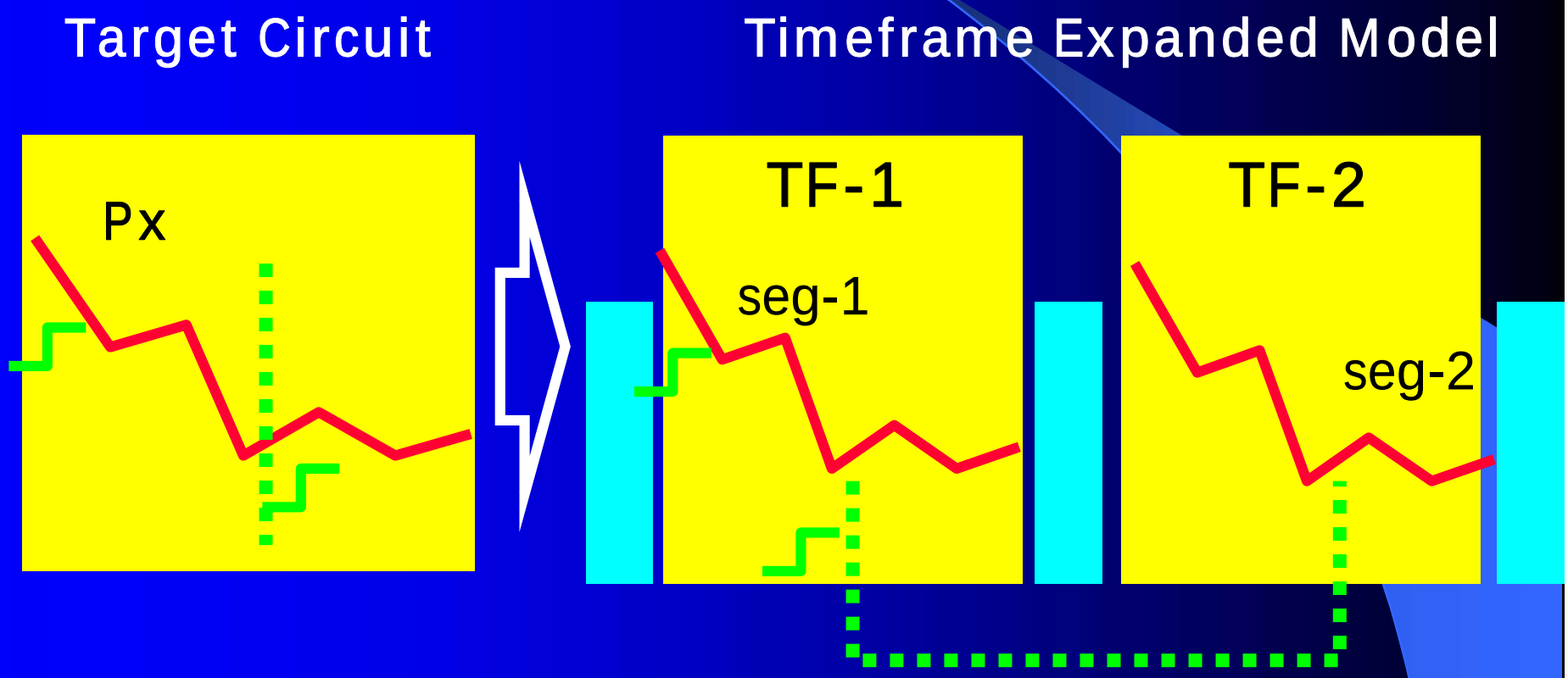
Multi-Cycle Path

- Definition: A k-cycle path *Px* could complete the propagation of the signal transition from the source to the destination in *k* cycles
- Clock period could be shorter than the delay of *Px*



Model for Illustration and Analysis



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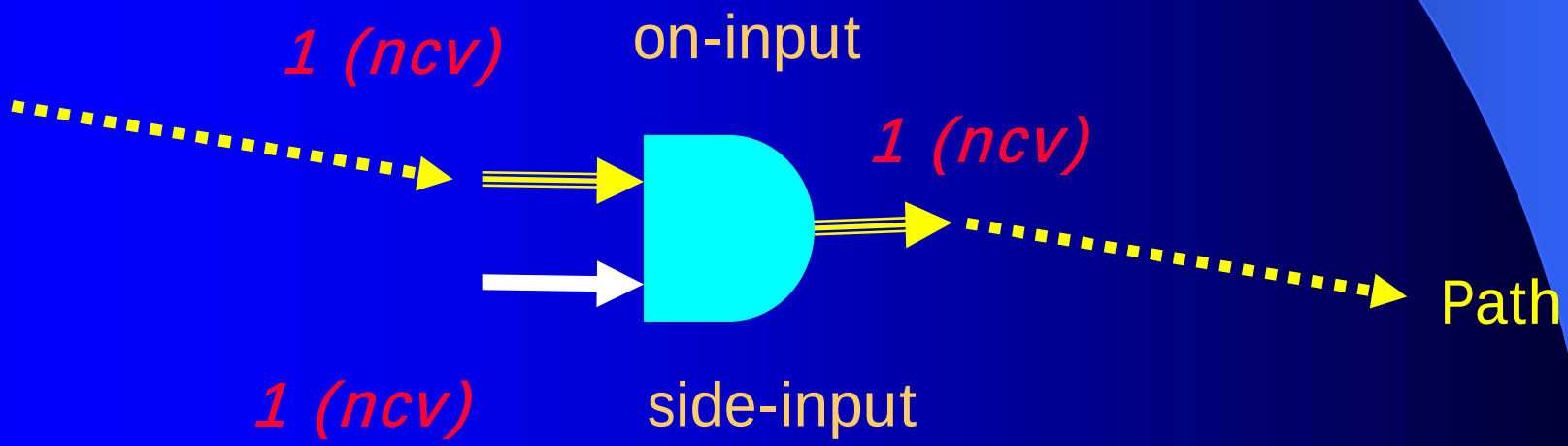
Necessary Conditions for Single-Cycle Sensitizable Path

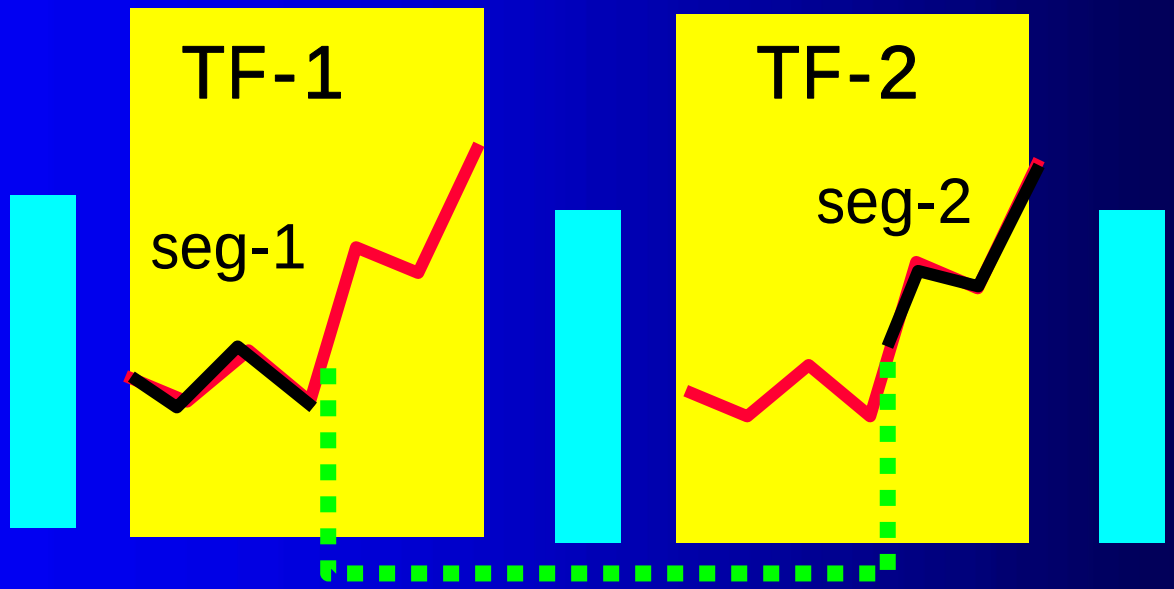
- Functional sensitization criterion [Cheng]
  - A path is sensitizable if there exists an input vector such that all the side-inputs along the path are non-controlling values when the corresponding on-input propagates a non-controlling value



Necessary Conditions for Multi-Cycle Sensitizable Path

- Each segment of a multi-cycle sensitizable path must satisfy the functional sensitization criterion in its corresponding timeframe. Otherwise, it is false.

Timeframe Expanded Model



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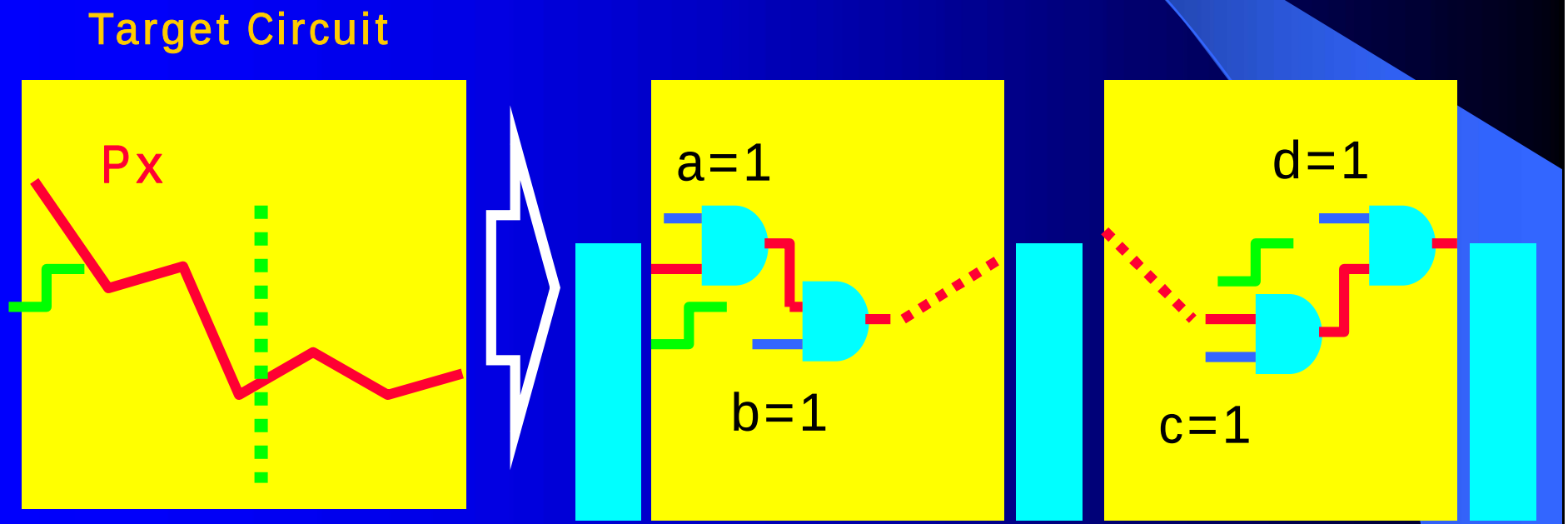
Identification of Multi-Cycle False Paths

- Segment-based checking algorithm to identify multi-cycle false paths
- Check the necessary condition under the timeframe expanded model

- Input
  - A path *Px*
  - The multiplicity *k*
  - The clock period *clk*
- Output
  - The sensitizability of path *Px*

Segment-Based Checking Algorithm

- Check the sensitizability of each segment of the multi-cycle path at each timeframe



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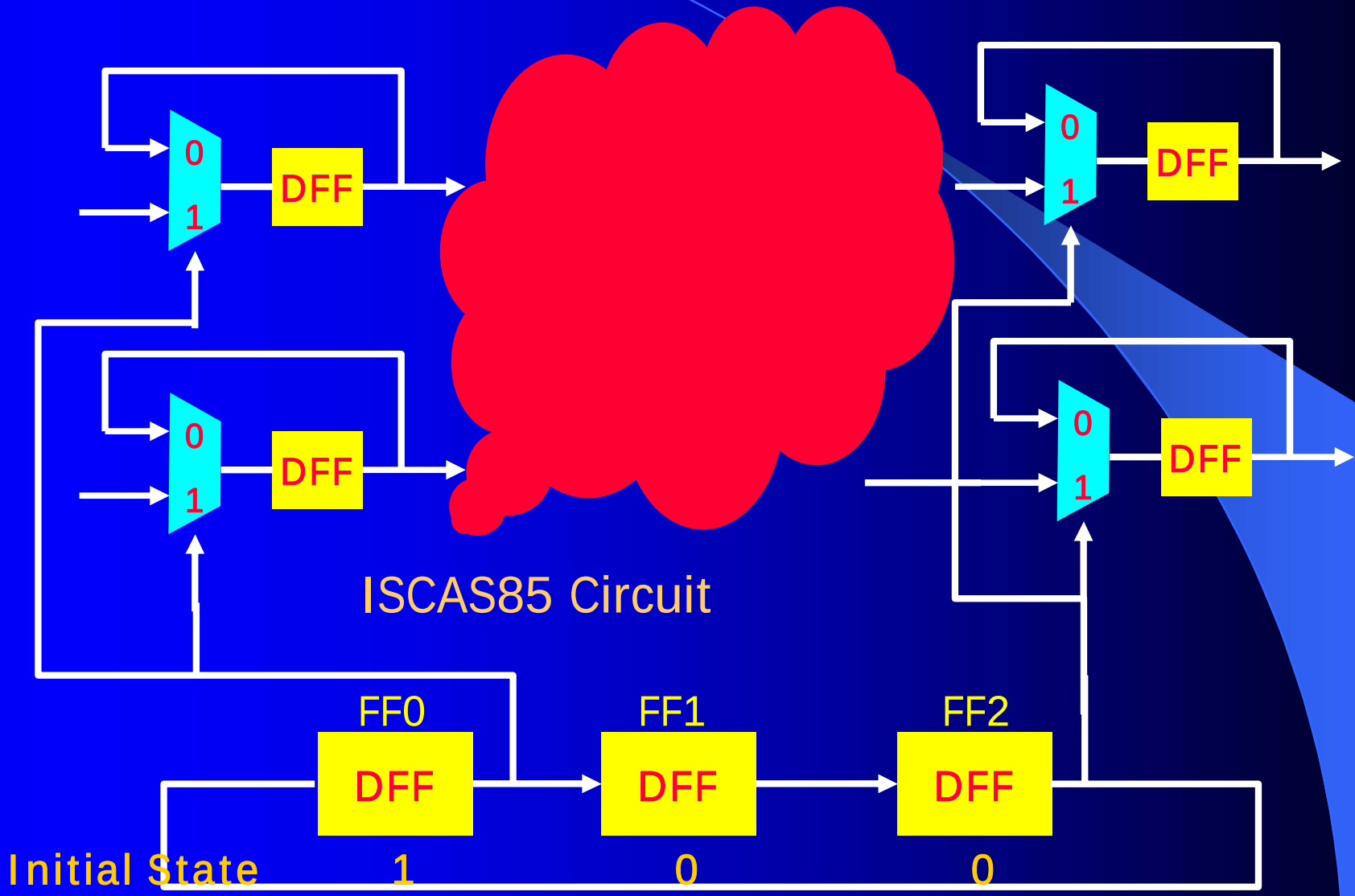
Valid Clock Period

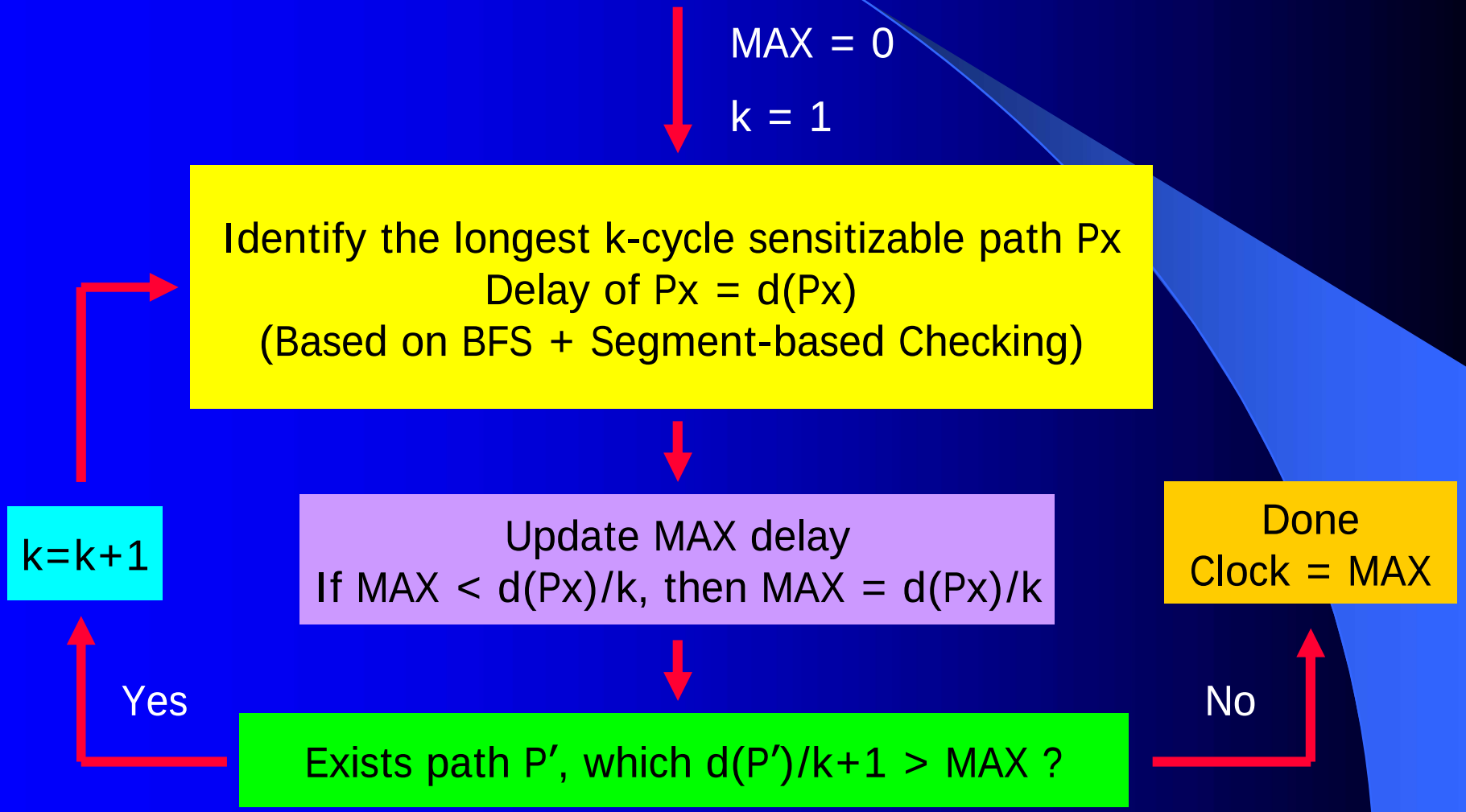
- Traditionally, the valid clock period is determined by the delay of the longest single-cycle sensitizable path
- With multi-cycle operation, the clock period is determined by the delay of the longest k-cycle sensitizable path divided by *k*

$$clk \geq (\max(d(P))/m, \forall P \in m-cycle-true-path, 1 \leq m \leq k$$

Calculating a Valid Clock Period



Iterative Method for Calculating Valid Clock Period



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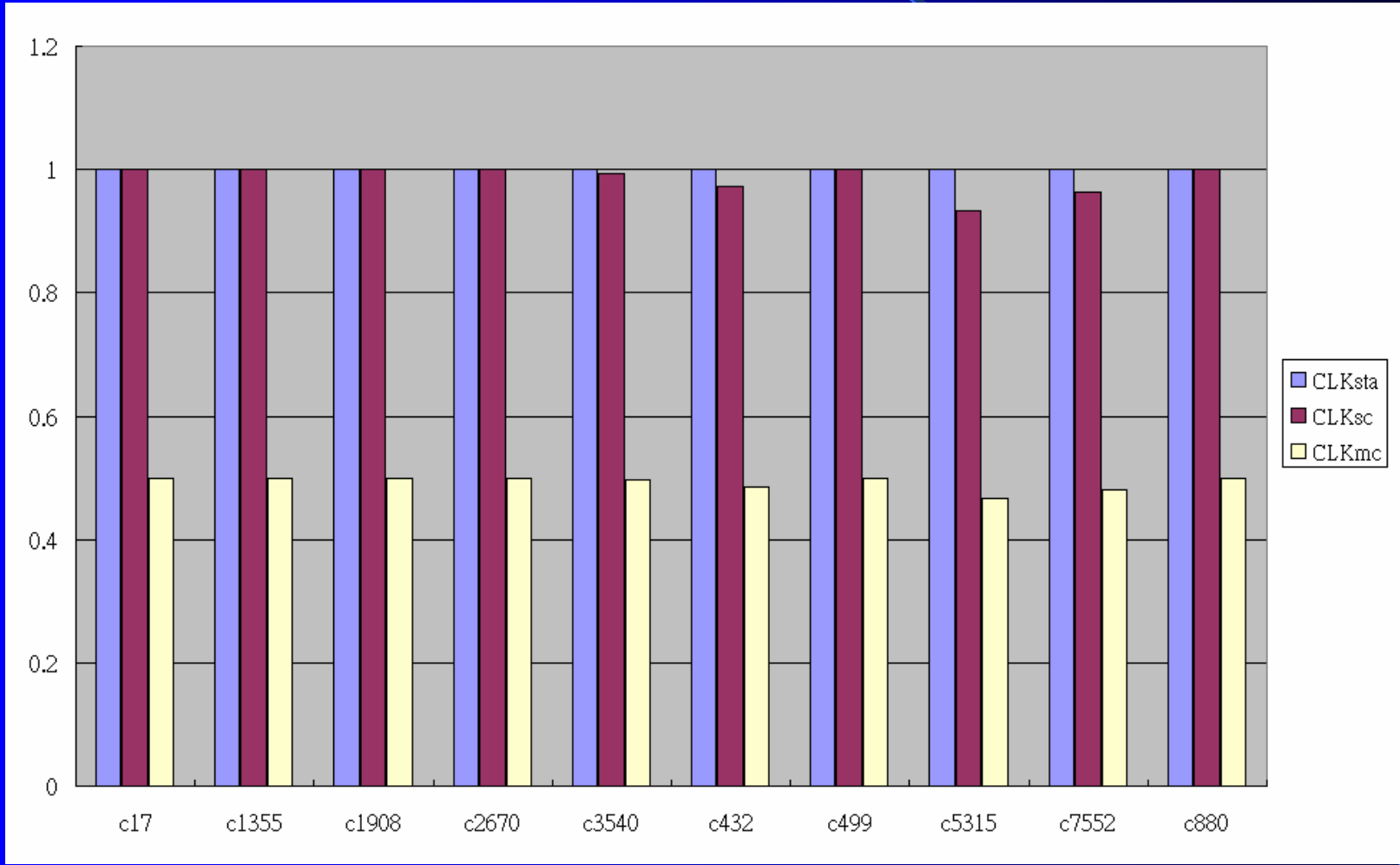
Experimental Result

Reported Clock Period for exemplar circuit



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Conclusion

- Define the multi-cycle false path and the multi-cycle sensitizable path
- Provide necessary conditions for multi-cycle sensitizable paths
- Algorithm to compute the valid clock period
- Demonstrate the improvement the clock frequency by considering multi-cycle false paths