IEEE Standard 1500 Based Interconnect Diagnosis for Delay and Crosstalk Faults

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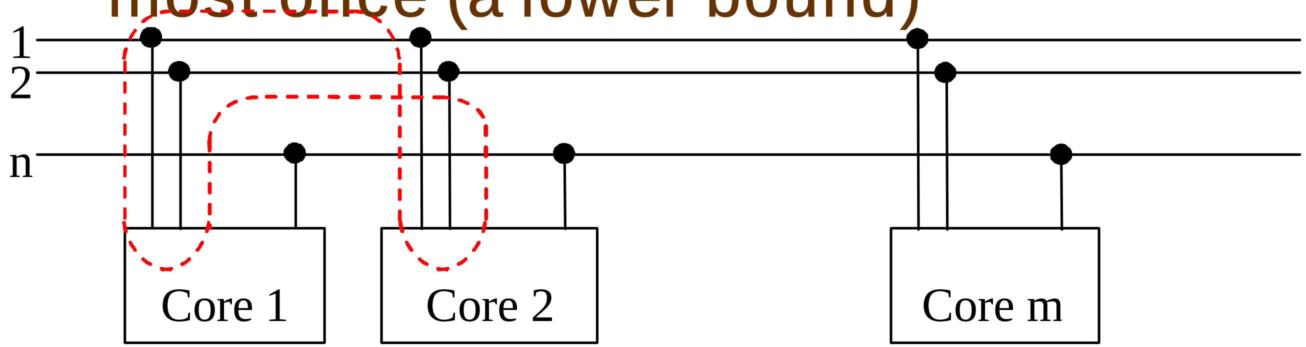
Outline

- Introduction
- Oscillation Ring Test Scheme for Interconnect Detection and Diagnosis
- Interconnect Diagnosis Algorithm
- Optimization Techniques for Interconnect Diagnosis
- Experimental Results
- Conclusion

C_i^n

Why Interconnect Testing and Diagnosis are Difficult?

- Complexity issue
  - Too many rings
  - Consider a bus-connected system
    - m cores, n bus lines
    - Assuming each core passed by a ring at most once (a lower bound)



rings of length l from n buses (connecting i cores): C_i^n

all rings: $\sum_{i=2}^{\min(m,n)} C_i^m C_i^n$ → Exponential !

Introduction (Cont'd)

- Interconnect dominates performance
  - Interconnect Diagnosis
- SoC Design Methodology
  - IEEE Std.1500 Based Interconnect Diagnosis
- Other Applications: PCB, MCM, SiP
- Interconnect Test
  - Goal
    - Interconnect Detection Problem=>Pass/Fail
    - Interconnect Diagnosis Problem=>Fault Location
  - Target Fault Models
    - Delay Fault
    - Crosstalk Glitch Fault
    - Traditional Stuck-at Fault, Open Fault
  - Oscillation Ring (OR) Based Test Scheme

Contribution of this Work

- Apply a heuristic algorithm to generate test rings quickly (R_t)
  - Previous Work on Oscillation Ring (OR) Based Interconnect Test Scheme for SOC
    - ASPDAC 2005
- Provide a fast diagnosability check algorithm
  - Similar to fast fault simulation
- Provide a heuristic algorithm to generate extra diagnosis rings
  - Similar to IORD test pattern generation
- Present two optimization testing process
  - Concurrent OR
  - Adaptive OR

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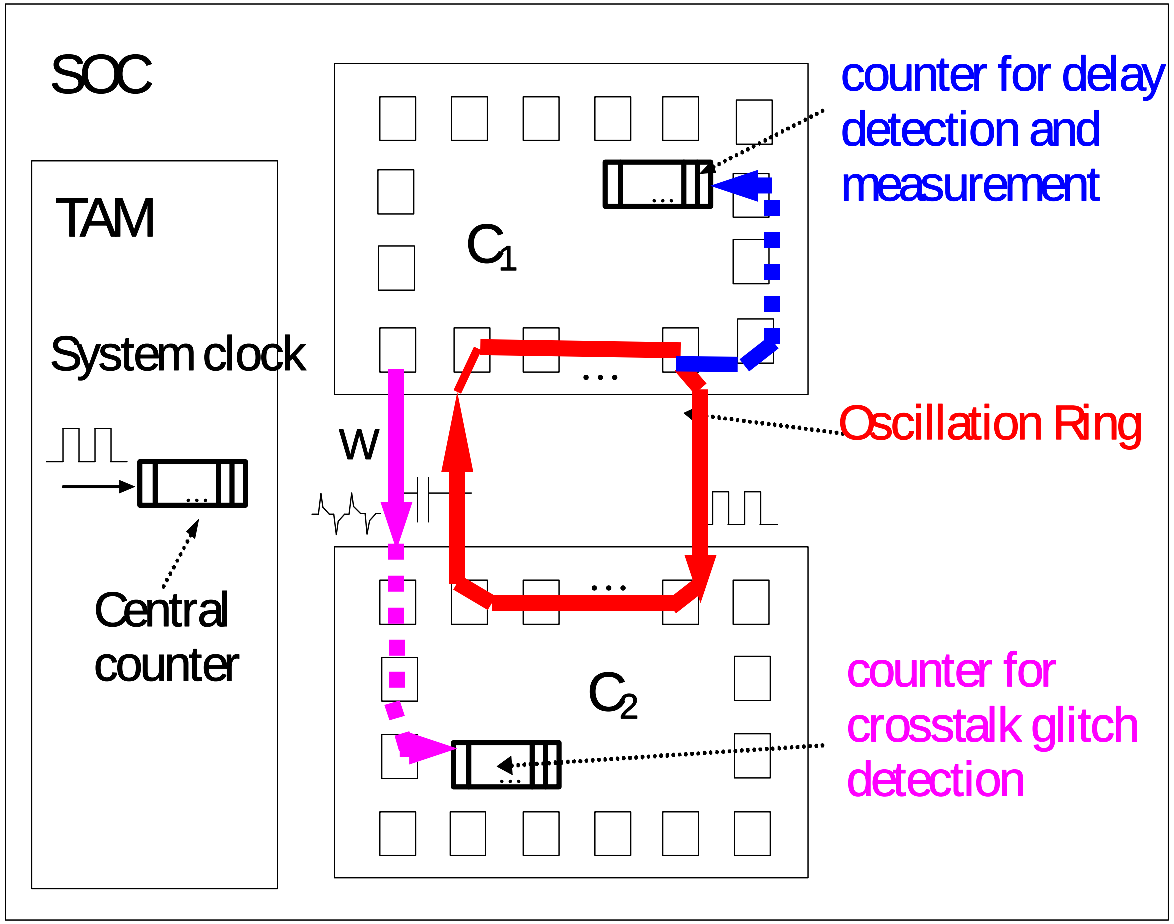
Oscillation Ring Test Scheme for Interconnect Detection and Diagnosis

- Oscillation Ring Test Scheme
  - Test Architecture
  - Enhanced IEEE Std.1500-Compliant Wrapper Cell Design
  - Effectiveness
    - Delay Fault: longest & shortest ring in HP circuit (f_{min} vs. f_{max})
    - Crosstalk Glitch Fault: SoC simulation results
- Oscillation Ring Test Scheme for
  - Interconnect Detection Problem (IORT)
  - Interconnect Diagnosis Problem (IORD)

Test Architecture for Delay and Crosstalk Detection and Delay Measurement



Oscillation Ring Test Scheme for Interconnect Detection and Diagnosis

- Oscillation Ring Test Scheme
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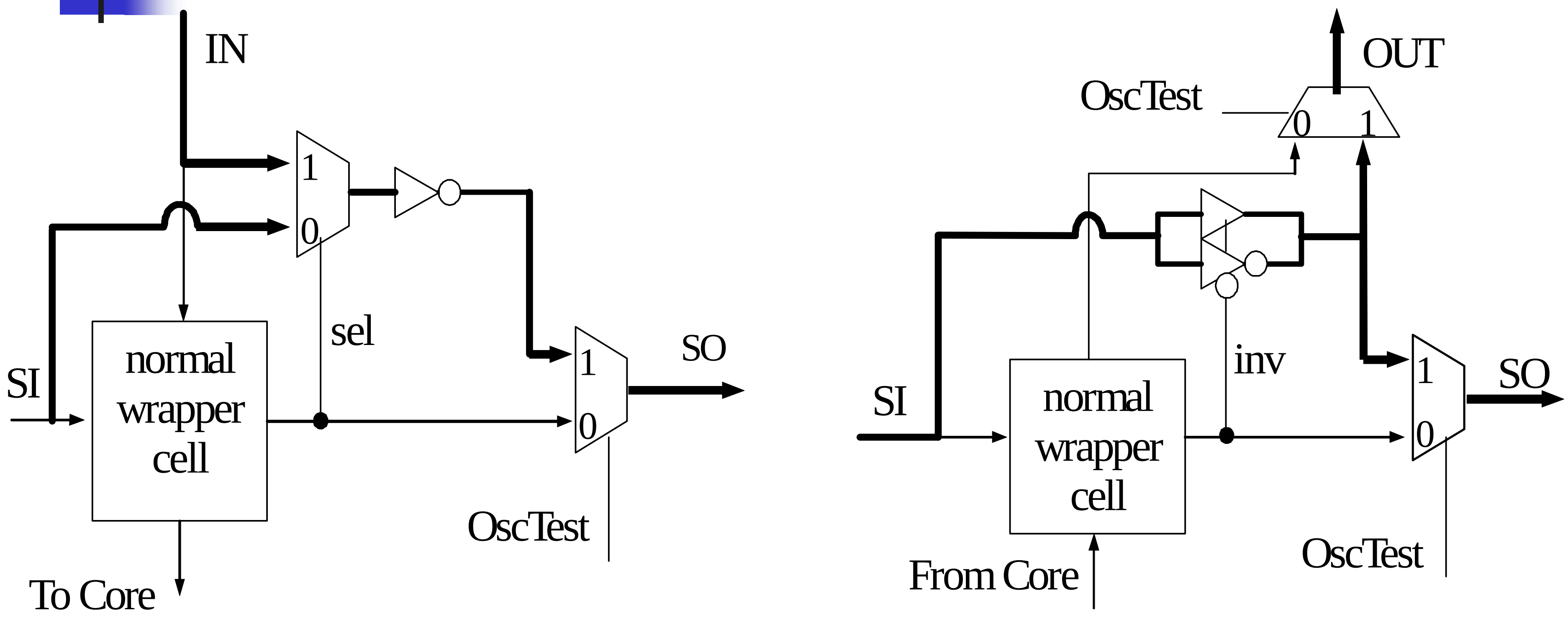
    - Crosstalk Glitch Fault:
- Oscillation Ring Test Scheme for
  - Interconnect Detection Problem (ORT)
  - Interconnect Diagnosis Problem (ORD)

IEEE Std.1500 Wrapper Cell Design



(a) Input

(b) Output

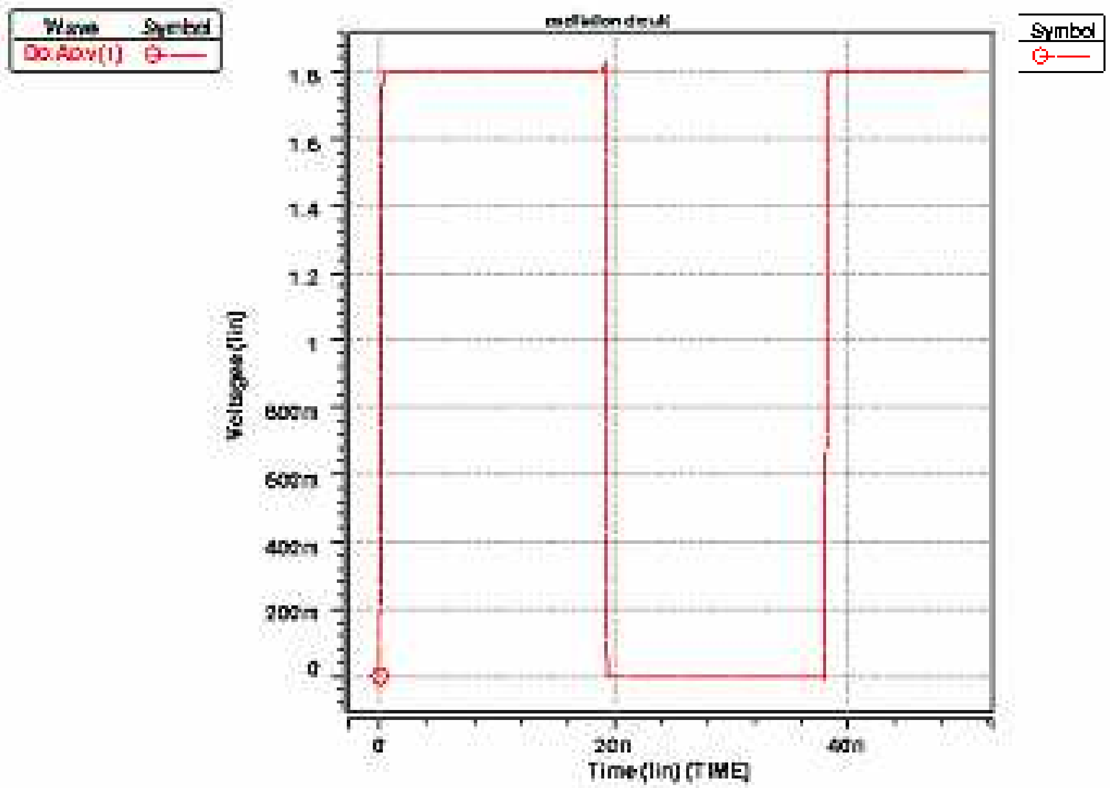
Modified with force Inversion

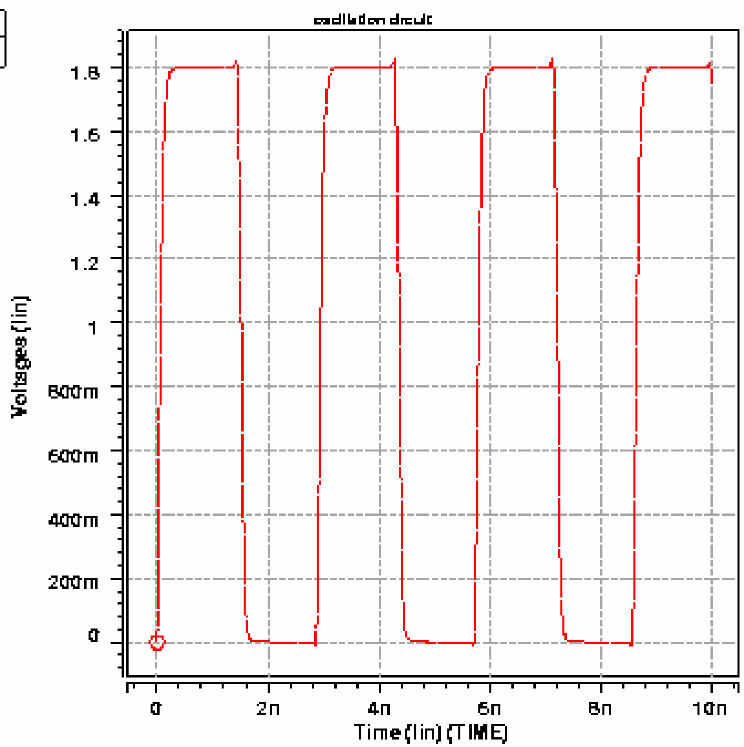
Oscillation Ring Test Scheme for Interconnect Detection and Diagnosis

- Oscillation Ring Test Scheme
  - Test Architecture
  - Enhanced IEEE Std.1500-Compliant Wrapper Cell Design
  - Effectiveness
    - Delay Fault:
      - longest & shortest ring in HP circuit (f_{min} vs. f_{max})
      - Delay Measurement
    - Crosstalk Glitch Fault:

Longest Test Ring in HP circuit

Simulated Waveforms of Longest and Shortest Test Rings of HP Circuit





Longest Ring of 38 ns

f_{min}= 21.316 MHz

Shortest Ring of 2.8 ns

f_{max}= 357.143 MHz

Oscillation Ring Test Scheme for Interconnect Detection and Diagnosis

- Oscillation Ring Test Scheme
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    - Delay Fault:
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      - Delay Measurement
    - Crosstalk Glitch Fault:

Delay Measurement

$$f_i = f \times \frac{n_i}{n}$$

Let f_i be 4 MHz to 400 MHz
(f_{min} = 4MHz, f_{max} = 400MHz)

$$\varepsilon = \frac{1}{f_{min} \times T_0} \leq \zeta$$

ξ be at least is 0.001

=>$n_{min} \geq 1000$

=>$T_0 \geq 250\mu s$

=> $T_0 = 250\mu s$ (OscTest Spec.)

Oscillation Ring Test Scheme for Interconnect Detection and Diagnosis

- Oscillation Ring Test Scheme
  - Test Architecture
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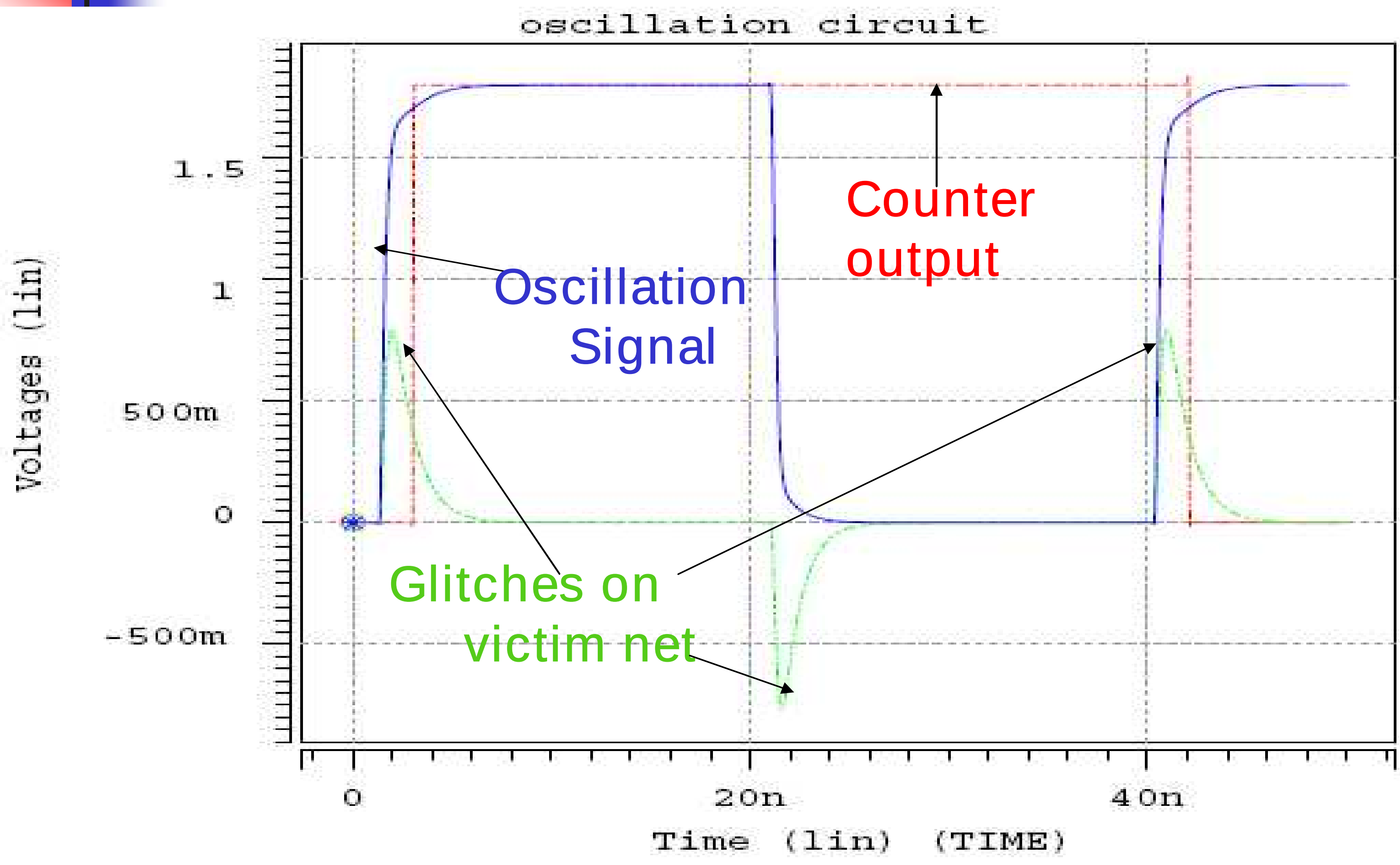
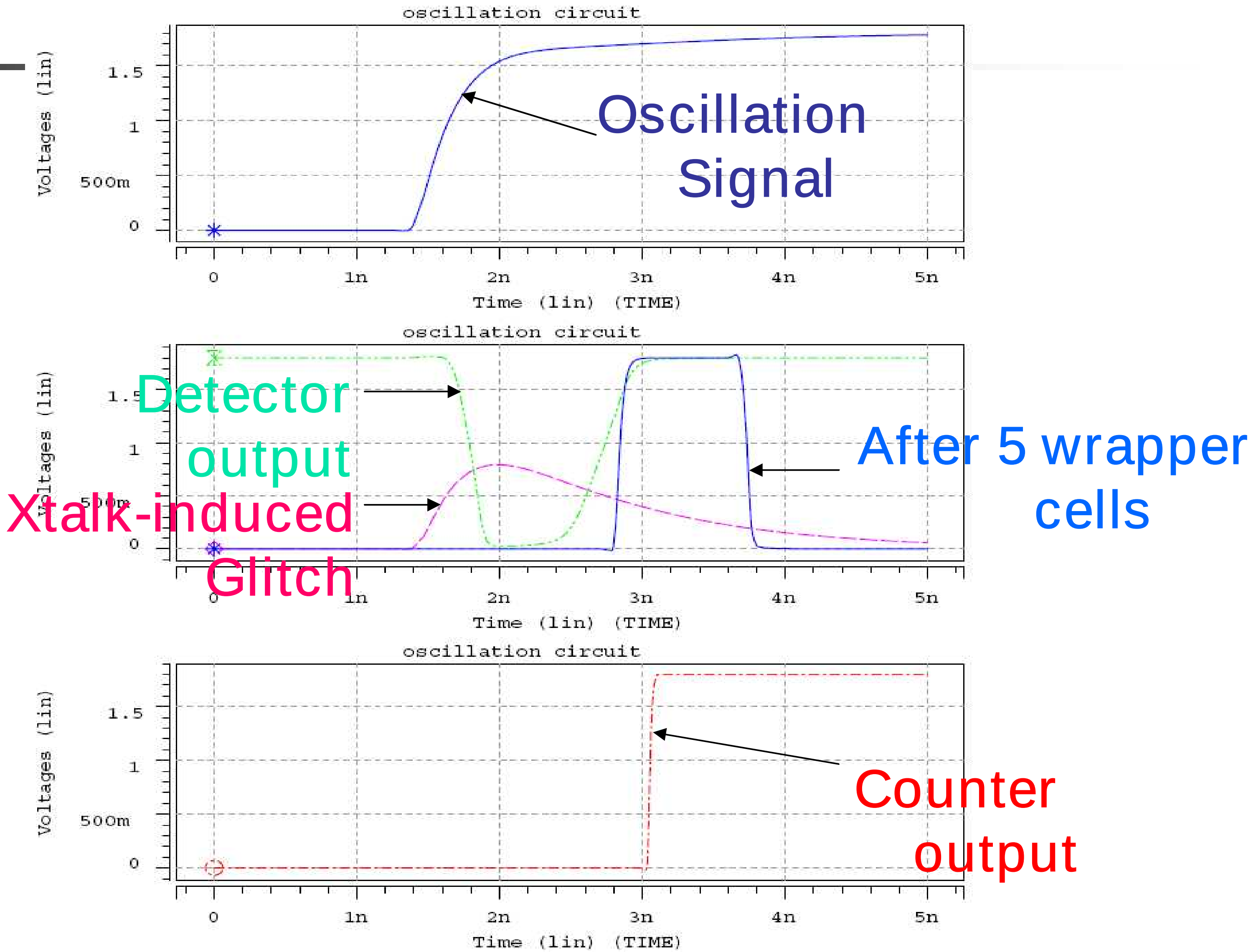
  - Effectiveness
    - Delay Fault:
      - longest & shortest ring in HP circuit (f_{min} vs. f_{max})
      - Delay Measurement
    - Crosstalk Glitch Fault:
      - longest ring in HP circuit with 5 wrapper cells

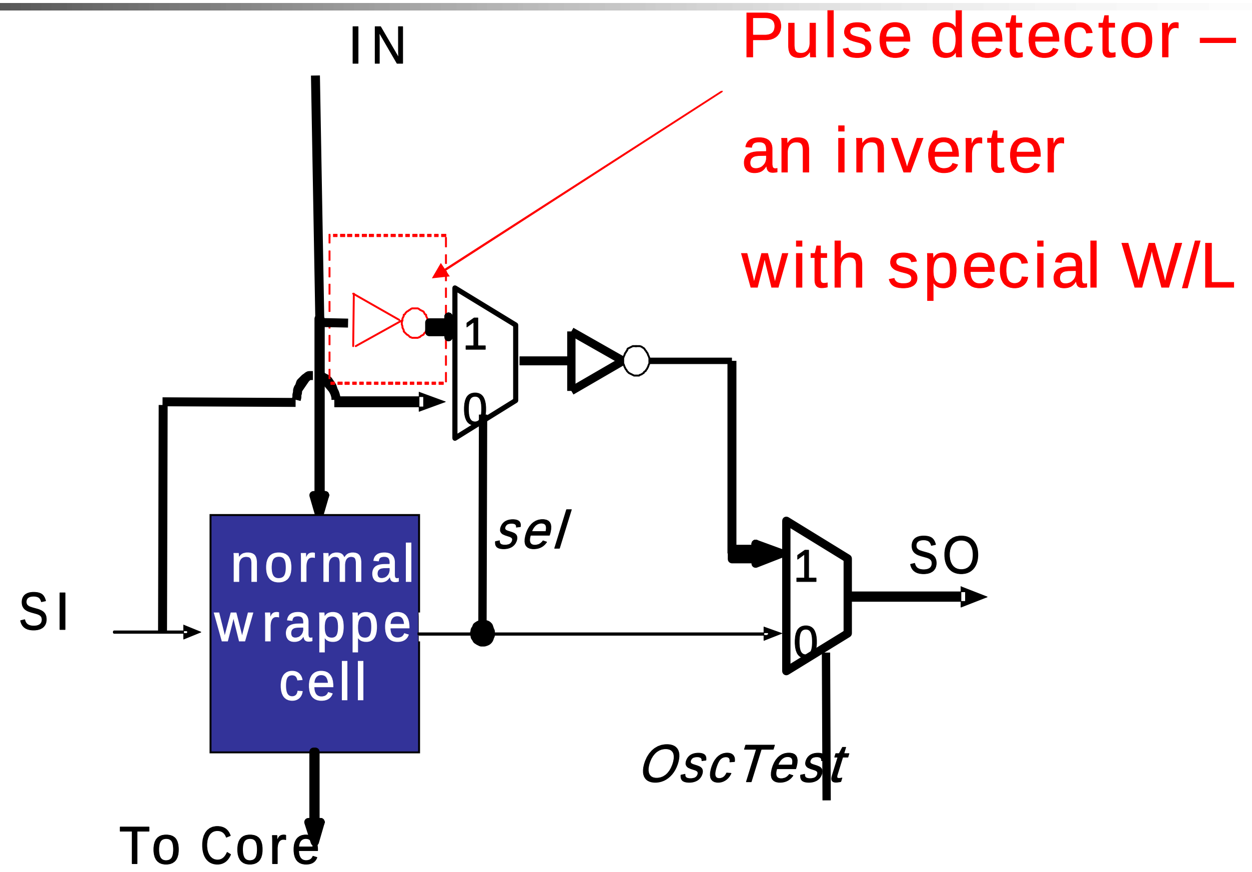
Crosstalk Glitch Fault Detection – longest ring in HP with 5 wrapper cells



Crosstalk Glitch Detection (cont'd)



Modified Input Wrapper Cell for Crosstalk Glitch Faults



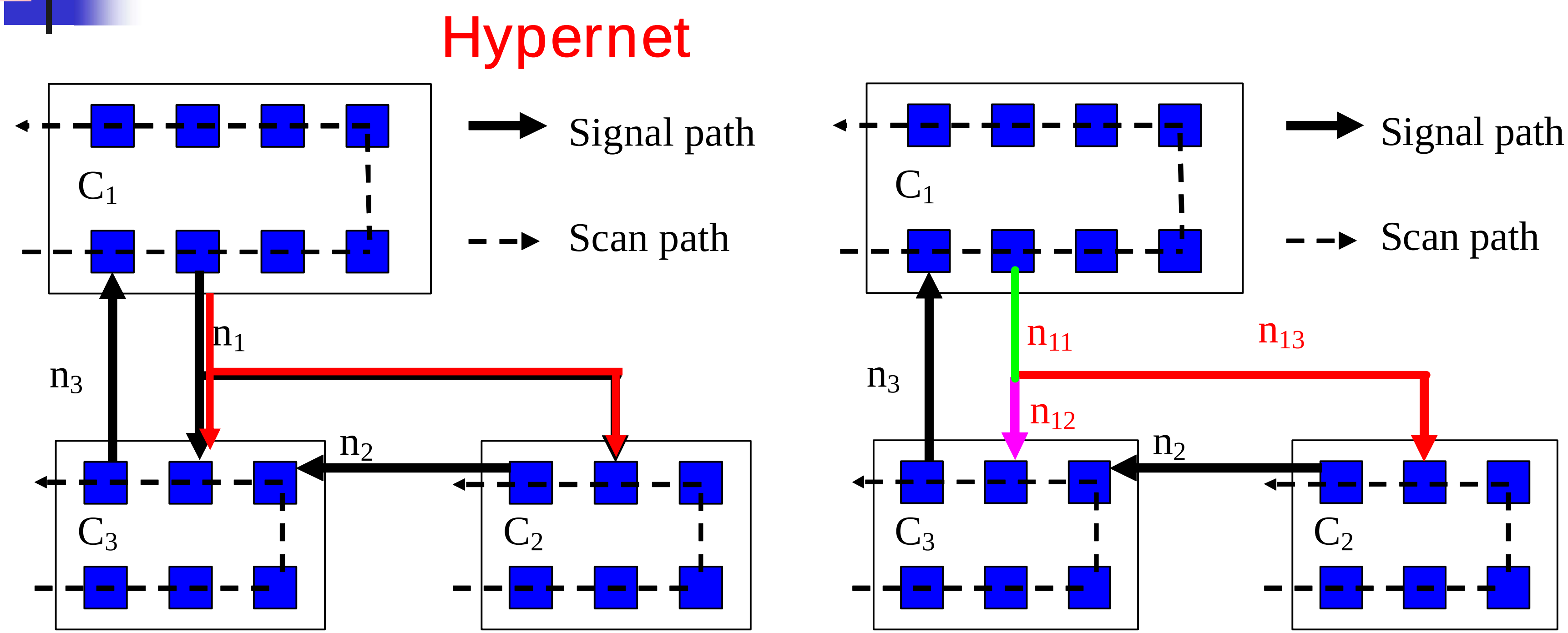
Oscillation Ring Test Scheme for Interconnect Detection and Diagnosis

- Oscillation Ring Test Scheme
  - Test Architecture
  - Effectiveness
    - Delay Fault: longest & shortest ring in HP circuit (f_{min} vs. f_{max})
    - Crosstalk Glitch Fault:
- Oscillation Ring Test Scheme for
  - Interconnect Detection Problem (IORT)
  - Interconnect Diagnosis Problem (IORD)

Oscillation Ring Test Scheme

- Single-Fault Assumption
- Interconnect Detection Problem (IORT)
  - Pass or Fail=>Edge-Covering Problem
  - Goal: Fault Detection on Test Rings
  - Interconnect Detection Model
- Interconnect Diagnosis Problem (IORD)
  - Fault Diagnosis=>Fault Location Problem
  - Goal: Optimal Resolution to Net Segment
  - Interconnect Diagnosis Model

An Example SOC Circuit for Interconnect Test



(a) Hypergraph of SoC Circuit with multiple-terminal nets

(b) Interconnect Test Modeling

Oscillation Ring Test Scheme

- Single-Fault Assumption
- Interconnect Detection Problem (IORT)
  - Pass or Fail=>Edge-Covering Problem
  - Goal: Faults on Test Rings
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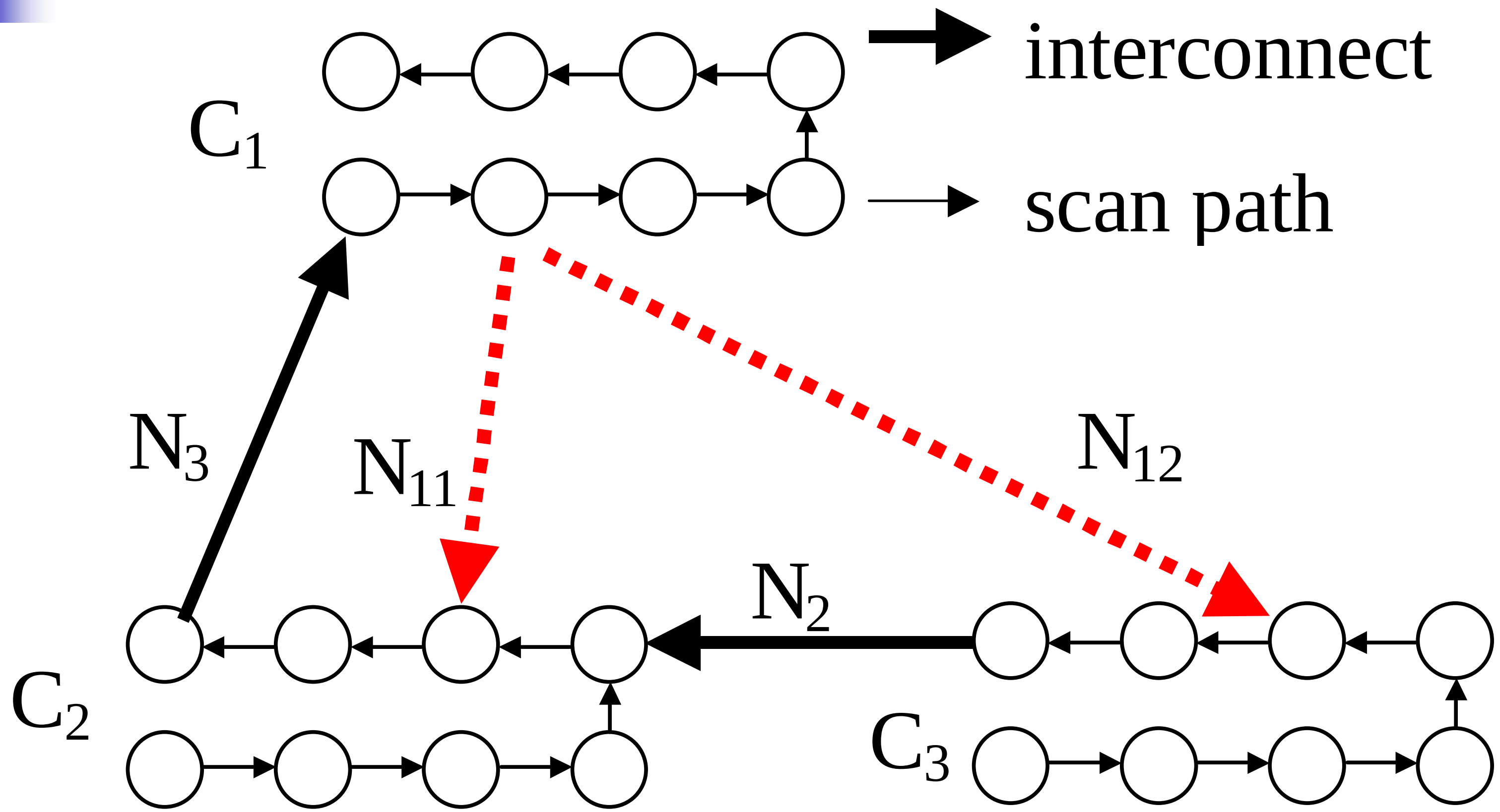
Interconnect Detection Model

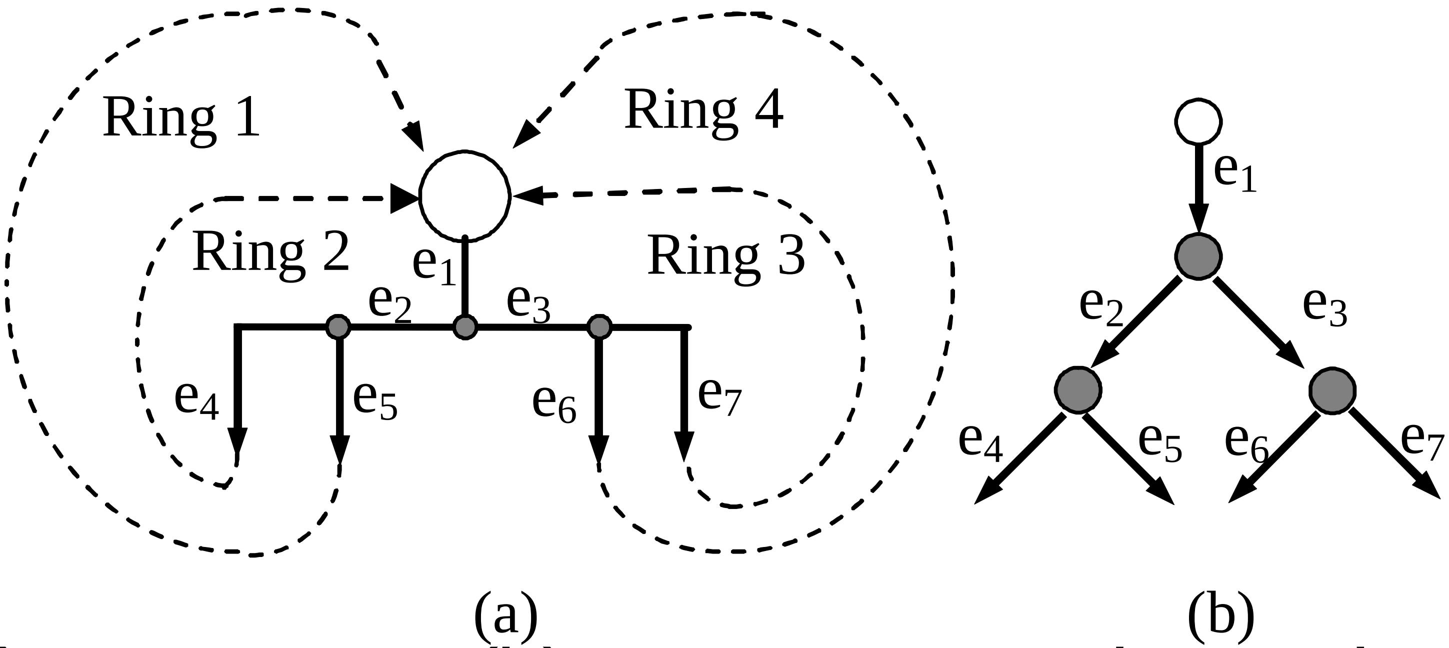


2-pin nets ($N_{11}=n_{11}+n_{12}$, $N_{12}=n_{11}+n_{13}$)

Oscillation Ring Test Scheme

- Single-Fault Assumption
- Interconnect Detection Problem (ORT)
  - Pass or Fail=>Edge-Covering Problem
  - Goal: Faults on Test Rings
  - Interconnect Detection Model
- Interconnect Diagnosis Problem (ORD)
  - Fault Diagnosis=>Fault Location Problem
  - Goal: Optimal Resolution to Net Segment
  - Interconnect Diagnosis Model

Interconnect Diagnosis Model



(a) Hypernet (b) Interconnect Diagnosis Model

For Diagnosis: Every Edge Influences Different Rings=>Optimal Diagnosis Resolution is Edge

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- Concluding Remarks

Interconnect Diagnosis Algorithm

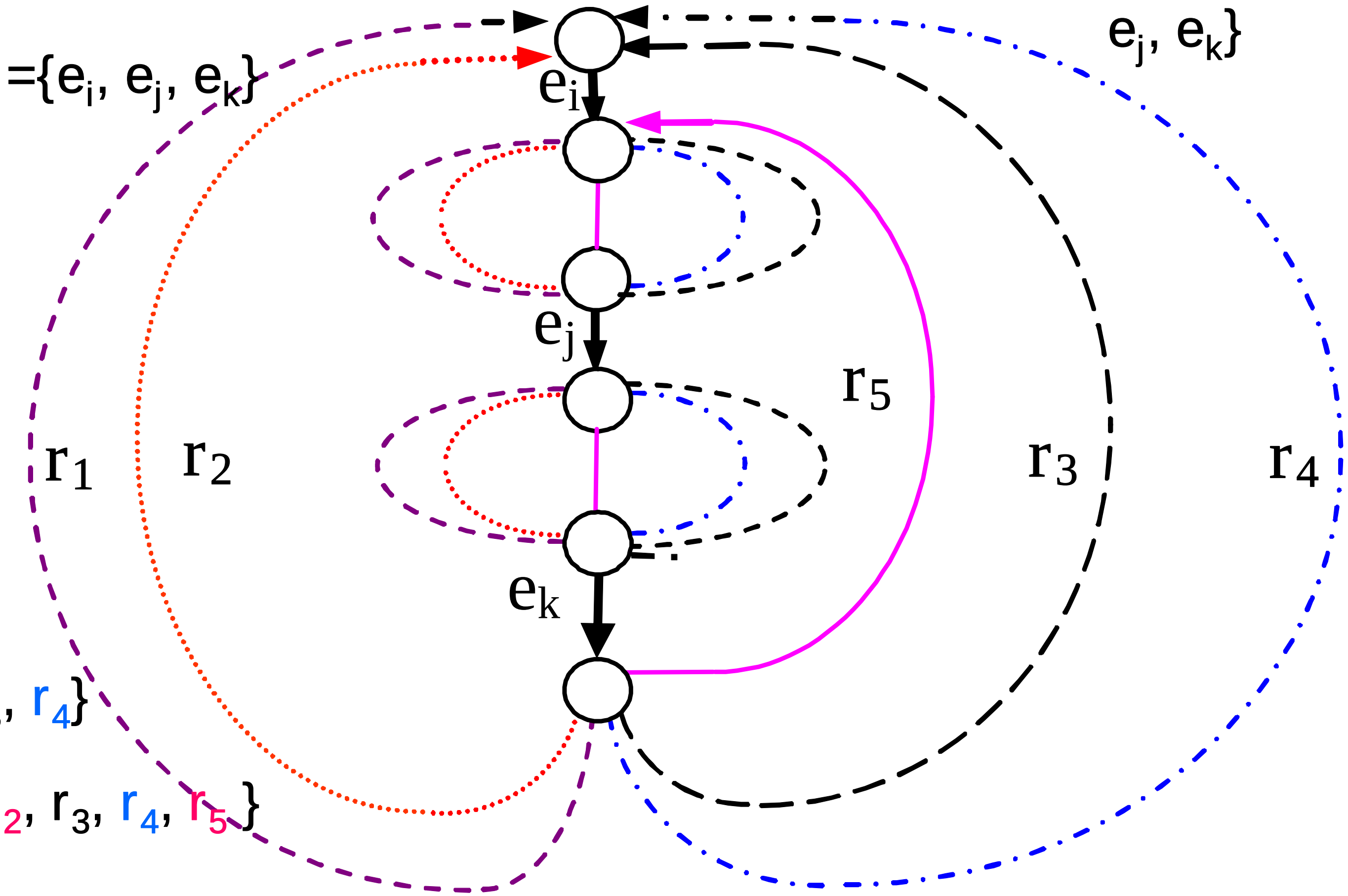
- Diagosability Conditions
- Heuristic Diagnosability Check
- Number of Tests
- Interconnect Diagnosis Algorithm
  - IORT (Interconnect Oscillation Ring Test)
  - IORD (Interconnect Oscillation Ring Diagnosis)

An Interconnect Diagnosis Graph Example to Show Diagosability Conditions

$E_i = r_1 \cap r_2 \cap r_3 \cap r_4 = \{e_i, e_j, e_k\}$

$r_1 = r_2 = r_3 = r_4 = \{e_i, e_j, e_k\}$

$r_5 = \{e_j, e_k\}$



$R_i = \{r_1, r_2, r_3, r_4\}$

$R_j = R_k = \{r_1, r_2, r_3, r_4, r_5\}$

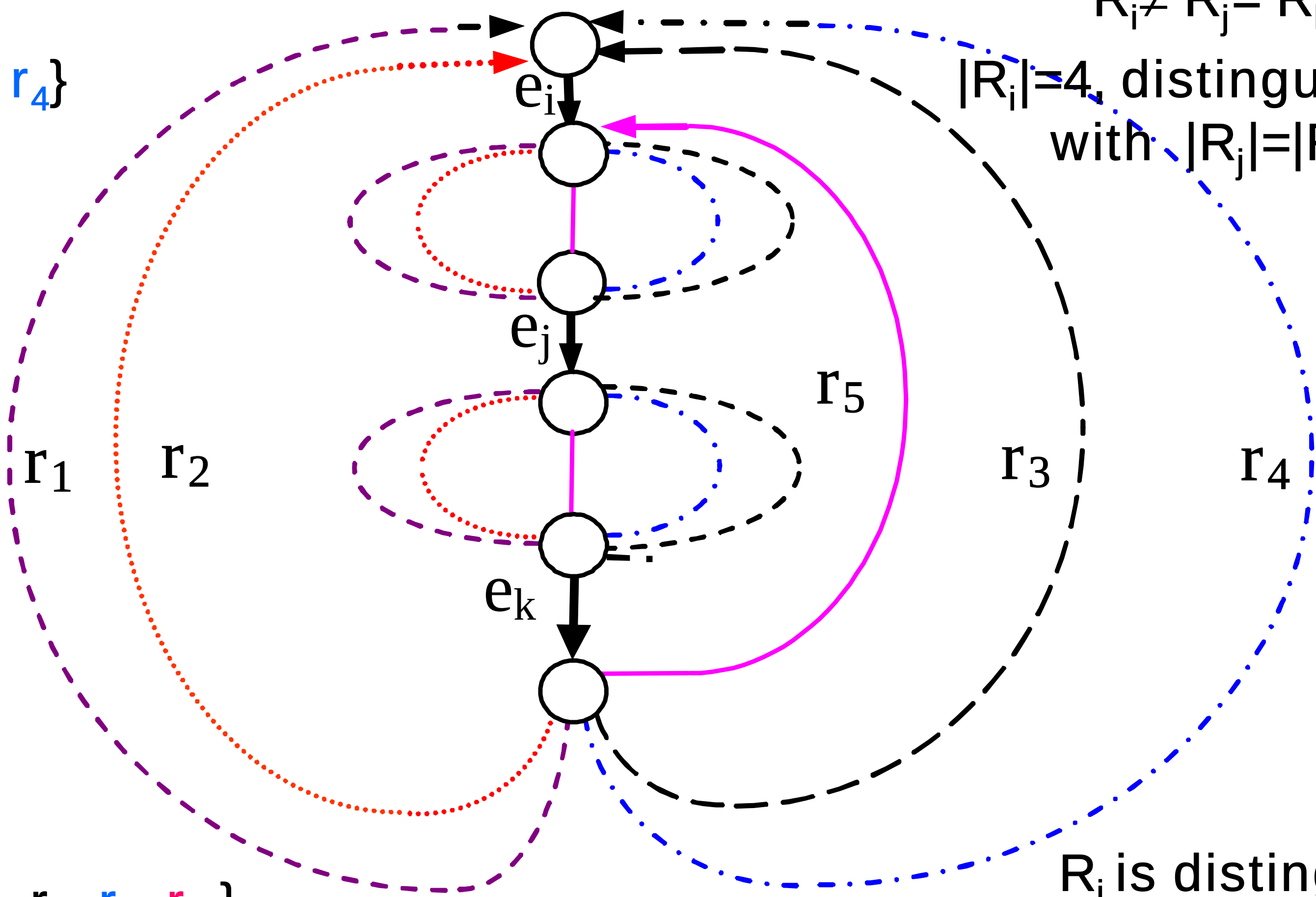
$E_j = E_k = r_1 \cap r_2 \cap r_3 \cap r_4 \cap r5 = \{e_j, e_k\} \Rightarrow Ei \neq E_j = E_k$

An Interconnect Diagnosis Graph Example

$R_i \neq R_j = R_k$

$|R_i|=4$, distinguishable with $|R_j|=|R_k|=5$

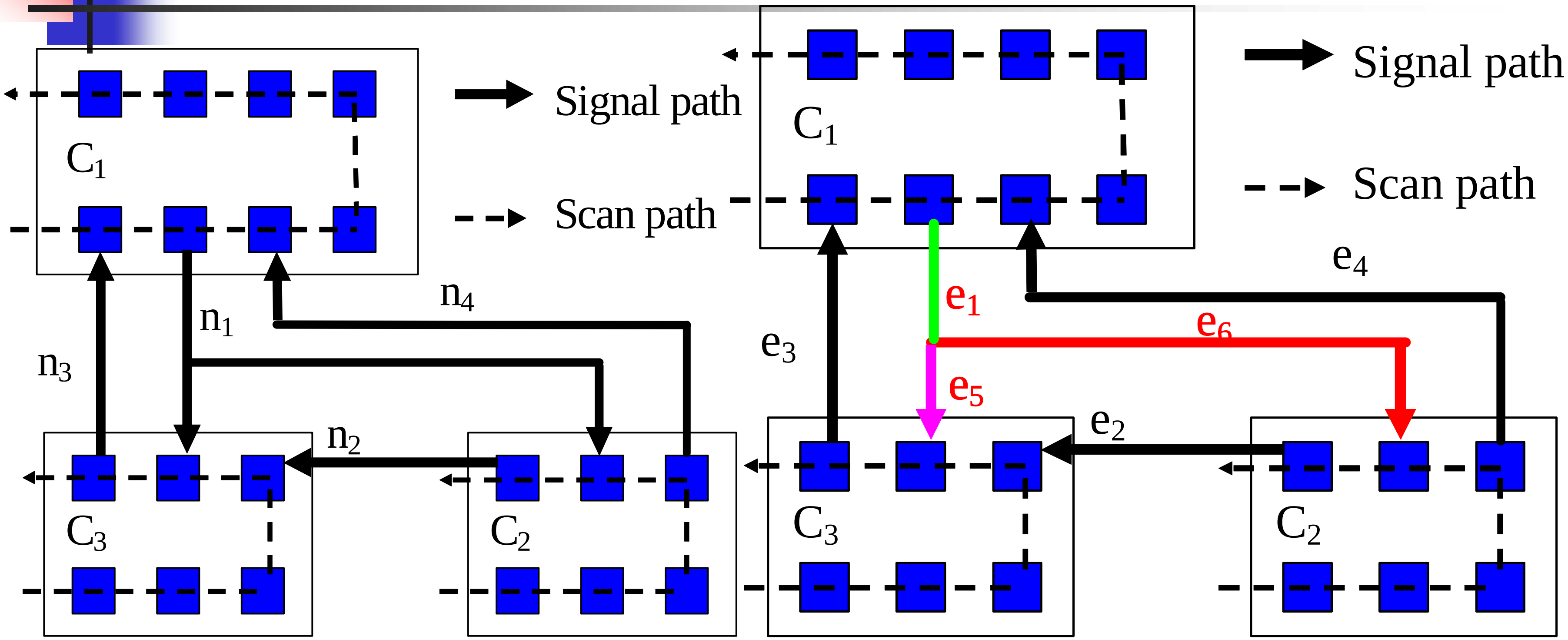
$R_i=\{r_1, r_2, r_3, r_4\}$



$R_j= R_k=\{r_1, r_2, r_3, r_4, r_5\}$

R_i is distinguishable with R_j and R_k

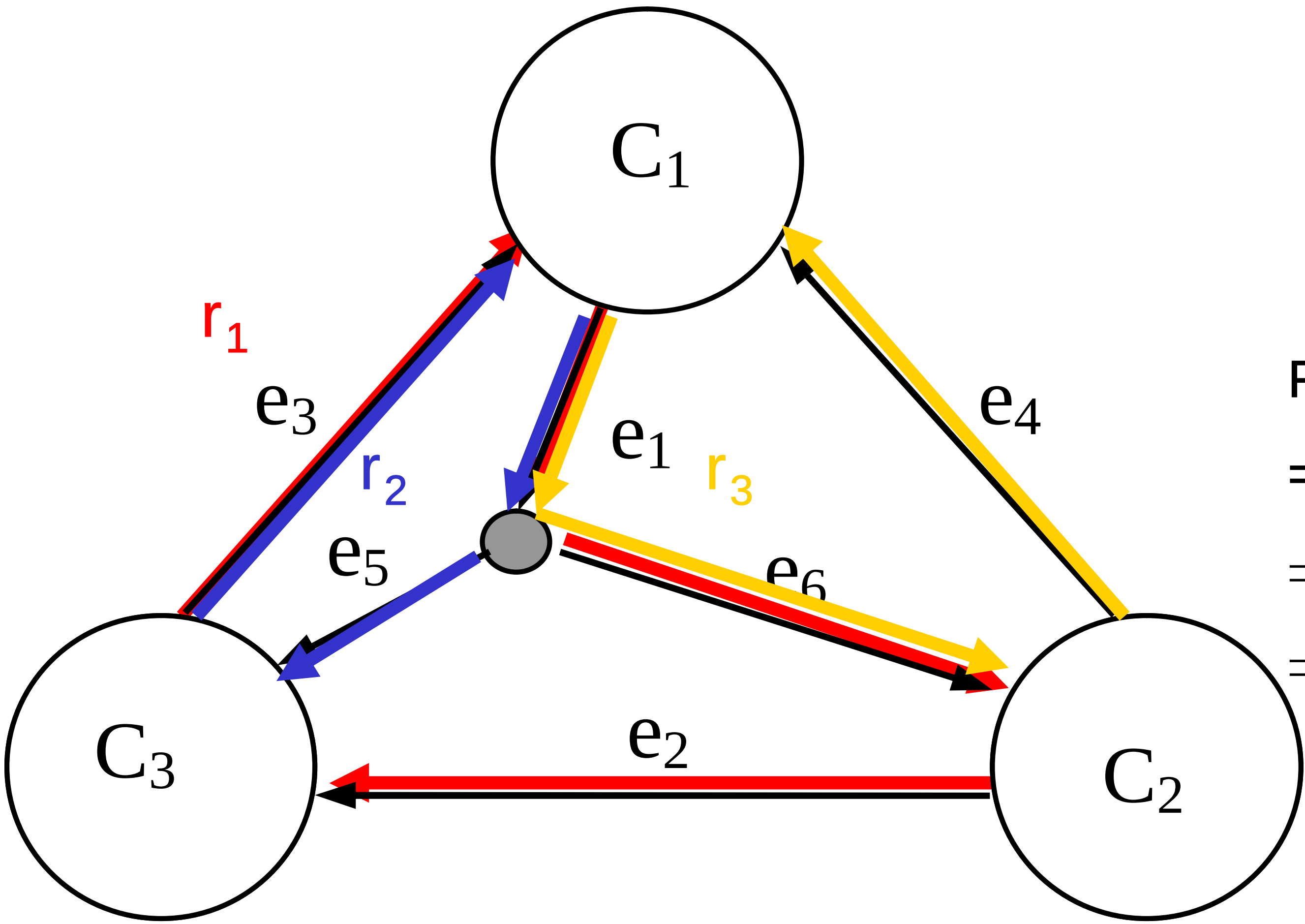
An Illustrative SoC Circuit for Interconnect Diagnosis



(a) Hypergraph

(b) Interconnect Diagnosis Model
=>Optimal Resolutation is Edge

An Illustrative Diagnosability Example



$r_1=\{e_1, e_2, e_3, e_6\}$

$r_2=\{e_1, e_3, e_5\}$

$r_3=\{e_1, e_4, e_6\}$

For Test Rings thru e_1

$\Rightarrow R_1=\{r_1, r_2, r_3\}$

$\Rightarrow$ $|R_1|=3$

$\Rightarrow$ Syndrome=[1,1,1]

Matrices for the Heuristic Diagnosability Checking

	e_1	e_3	e_6	e_2	e_4	e_5
r_1	1	1	1	1	0	0
r_2	1	1	0	0	0	1
r_3	1	0	1	0	1	0

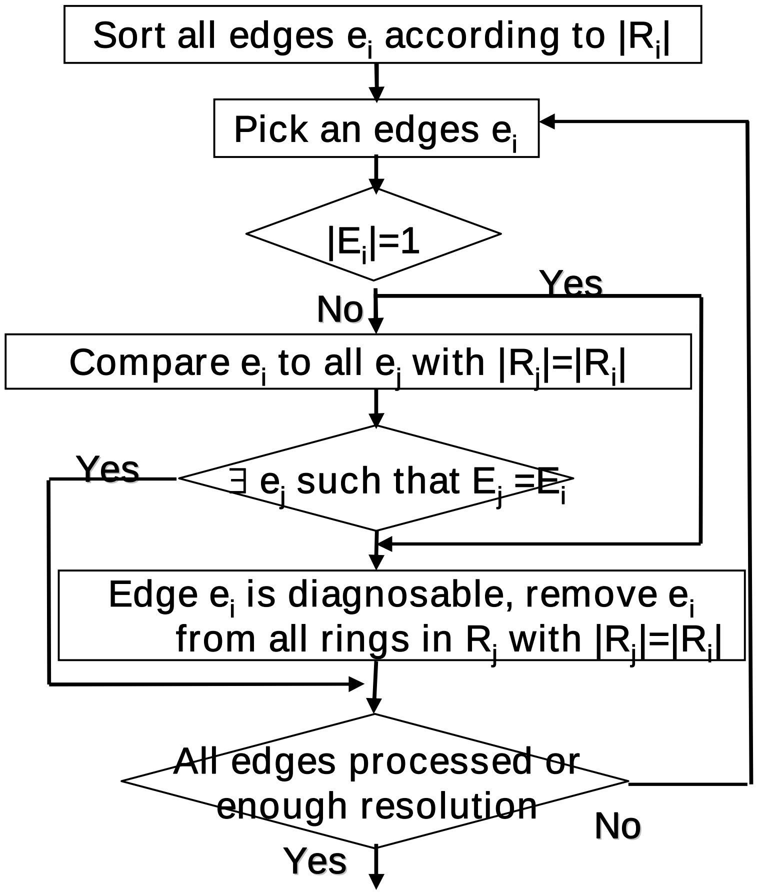
(a)

	√	√	√			
	e_1	e_3	e_6	e_2	e_4	e_5
r_1	1	1	1	1	0	0
r_2	1	1	0	0	0	1
r_3	1	0	1	0	1	0

(b)

Complexity for check: $O(n^2m)$

Flow Chart
of Diagnosability Checking



Interconnect Diagnosis Algorithm

- Diagosability Conditions
- Heuristic Diagnosability Check
- Number of Tests
- Interconnect Diagnosis Algorithm
  - IORT (Interconnect Oscillation Ring Test)
  - IORD (Interconnect Oscillation Ring Diagnosis)

Number of Tests

- IORT ($|R_t|$)
  - Lower Bound: 1
  - Upper Bound: n
- IORD ($|R_d|$)
  - Previous Example: n/2 distinct rings
  - N-bus Example: n-1 rings
  - Random Case: $|R_d|=|R_t|+$additional Diagnosis Rings predetermined rings

Theorem for Upper Bound of Predetermined Diganosis

- Assume:
  - m equivalence classes, whose sizes are s_1, s_2, …, s_m, respectively.
  - The upper bound on the number of additional diagnosis rings "$|R_d|-|R_t|$" as theoretical results:

$$\sum_{i=1}^{m}(S_i - 1) = \sum_{i=1}^{m} S_i - m = \#\,\mathrm{NoDiag} - \#\,\mathrm{EquClass}$$

An Illustrated Example of Predetermined Diganosis Ring Generation

	e_1	e_3	e_6	e_2	e_4	e_5
r_1	1	1	1	1	0	0
r_2	1	1	1	0	0	1
r_3	1	0	0	0	1	0

	e_1	e_3	e_6	e_2	e_4	e_5
r_1	1	1	1	1	0	0
r_2	1	1	1	0	0	1
r_3	1	0	0	0	1	0
r_4	0	1	0	0	1	0

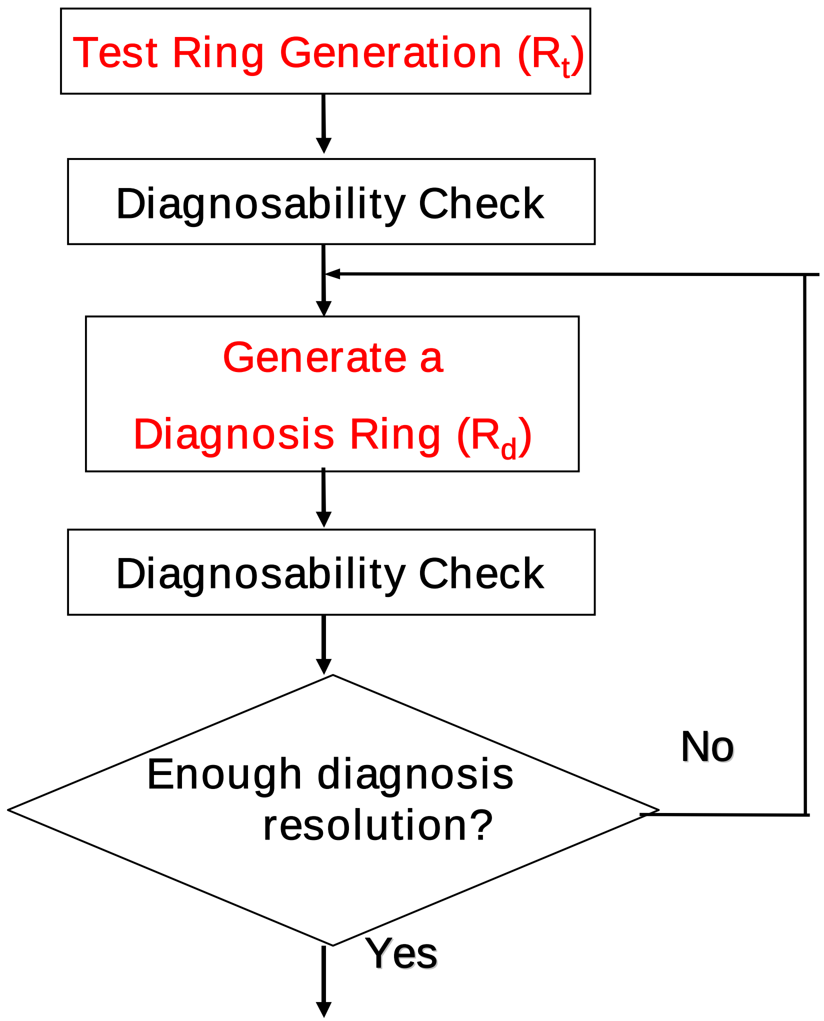
Add r_4 to distinguish between e_3 and e_6 in Group of $|R_i|=2$

=> Syndrome of e_3 and e_6 is different!

Interconnect Diagnosis Algorithm

- Interconnect Diagnosability Analysis
- Heuristic Diagnosability Check
- Number of Tests
- Interconnect Diagnosis Algorithm
  - IORT (Interconnect Oscillation Ring Test)
  - IORD (Interconnect Oscillation Ring Diagnosis)

Diagnosis Ring Generation Procedure



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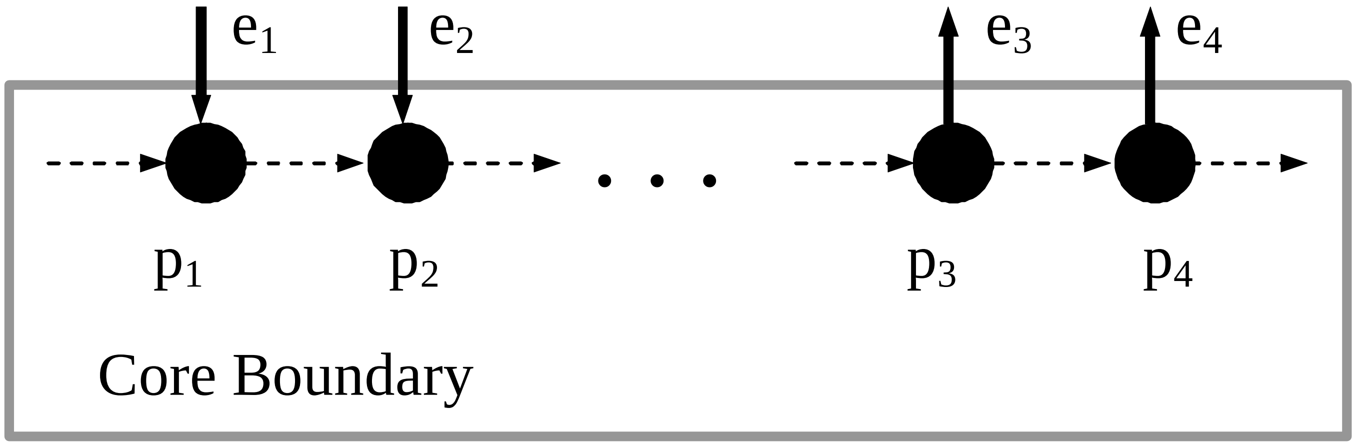
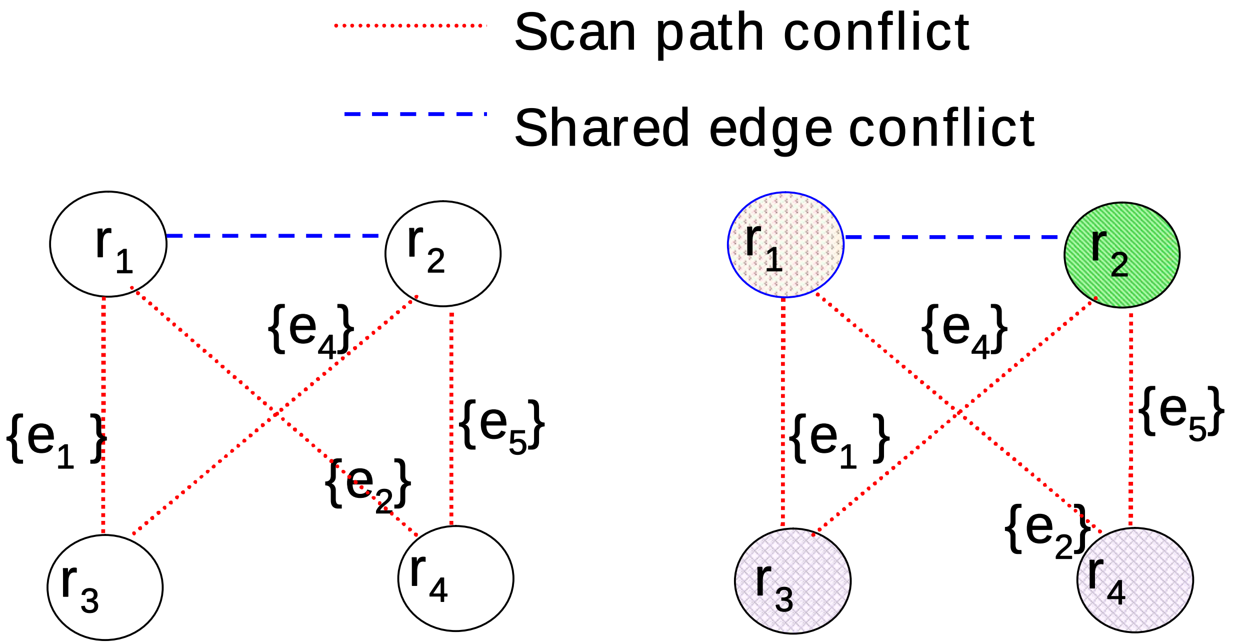
Optimization Techniques for Interconnect Diagnosis

- Concurrent Diagnosis: under Worst Case Scenario
  - Scan Path Constraint
  - Shared Edge Constraint
- Adaptive Diagnosis (R_a)
  - Use almost same test cost with IORT (R_t) only to reduce test time efficiently

Scan Path Constraints



Concurrent Test



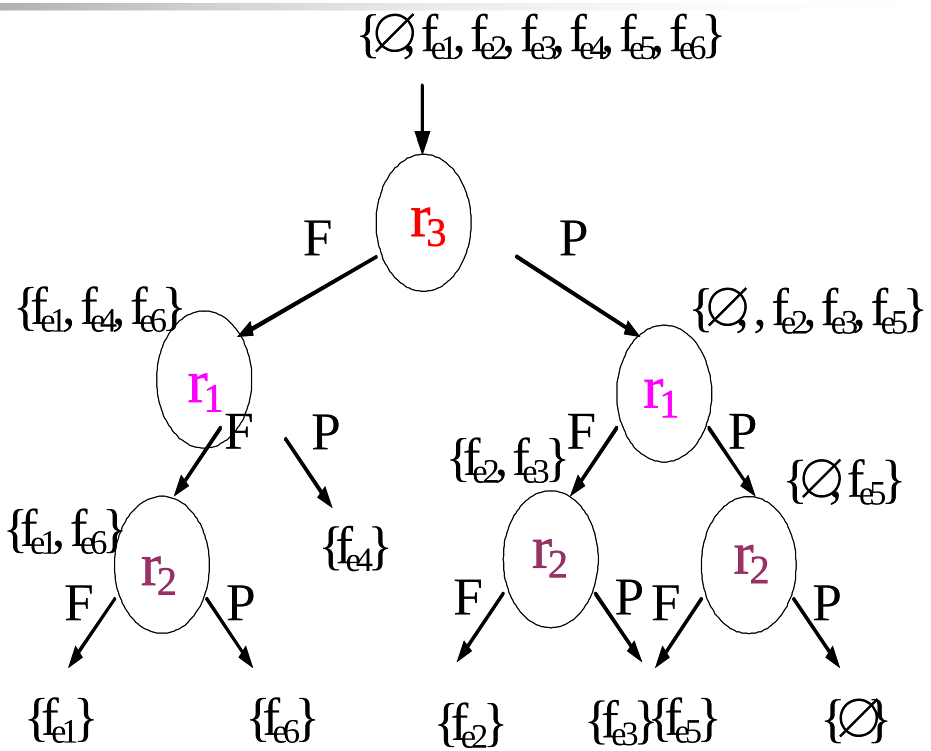
(a) Conflict Graph (b) Graph coloring

Optimization Techniques for Interconnect Diagnosis

- Concurrent Diagnosis
  - Scan Path Constraint
  - Shared Edge Constraint
- Adaptive Diagnosis (R_a)
  - Construct adaptive diagnosis tree
  - Diagnosis cost
    - Best Case: Balanced adaptive tree
    - Worst Case: Skewed adaptive tree

Adaptive Diagnosis Tree

	e_1	e_3	e_6	e_2	e_4	e_5
r_1	1	1	1	1	0	0
r_2	1	1	0	0	0	1
r_3	1	0	1	0	1	0



Diagnosability Checking Matrix

Upper Bound of Adaptive Diagnosis

- $|R_t|$: the number of test rings for detection (IORT)
- L_h: the length of the longest test ring
- Best Case
  - If the tree is balanced, the minimum number of diagnosis patterns required is $\lceil \log(n+1) \rceil$
- Worst case for Skewed Adaptive Tree,
  - Apply $|R_t|$ rings to find out that there is a faulty net, and
  - The last ring contains L_h net segments that are all passed by the ring only. It takes up to L_h-1 rings to distinguish these L_h possible faults, and thus the maximum number of diagnosis rings is $|R_t| + (L_h-1)$.

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Experimental Results for Interconnect Diagnosis both for Predetermined and Adaptive Methods

Circuit	Statistics				Predetermined			Analysis				Adaptive		
	#core	#pad	#hyp	#net_seg.	$\lvert R_t\rvert$	$\lvert R_d\rvert$	$\lvert R_d\rvert / \lvert R_t\rvert$	#OneRing	#NoDiag	#EquClass	$\lvert R_d\rvert - \lvert R_t\rvert$	max. EC	$\lvert R_a\rvert$	$\lvert R_d\rvert / \lvert R_a\rvert$
ac3	27	75	211	416	133 (33.3ms)	374 (93.5ms)	2.81	389	323	68	241	8	140 (35ms)	2.67
ami33	33	42	117	343	242 (60.5ms)	303 (75.8ms)	1.25	309	126	59	61	5	246 (61.5ms)	1.23
ami49	49	22	361	475	156 (39ms)	386 (96.5ms)	2.47	406	337	88	230	9	162 (40.5ms)	2.38
apte	9	73	92	136	73 (18.3ms)	122 (30.5ms)	1.67	127	94	40	49	4	76 (19ms)	1.61
hp	11	45	72	195	81 (20.3ms)	164 (41ms)	2.02	176	145	51	82	7	87 (21.8ms)	1.89
xerox	10	2	161	356	218 (54.5ms)	342 (85.5ms)	1.57	346	214	86	124	5	222 (55.5ms)	1.54
Compar.					0.9679								1	

Experimental Results – Concurrent Test Sessions

Circuit	$\lvert R_d \rvert$	$\lvert R_c \rvert$ (worst case)	$\lvert R_d \rvert - \lvert R_c \rvert$
ac3	374	373	1 (0.27%)
ami33	303	290	17 (5.86%)
ami49	386	352	34 (9.66%)
apte	122	119	3 (2.52%)
hp	164	160	4 (2.50%)
xerox	342	327	15 (4.59%)
Comparison	1.0432	1	4.57%

Experimental Results – Comparison between Theoretical Bounds and Experimental Results

Circuit	#NoDiag	#EquClass	(#NoDiag-#EquClass)	Extra Rings ($\|R_d\|-\|R_t\|$)	(#NoDiag-#EquClass) and ($\|R_d\|-\|R_t\|$)
ac3	323	68	255	241	14 (5.49%)
ami33	126	59	67	61	6 (8.96%)
ami49	337	88	249	230	19 (7.63%)
apte	94	40	50	49	1 (2.00%)
hp	145	51	94	82	12 (12.77%)
xerox	214	86	128	124	4 (3.13%)
Comparison			1.0712	1	6.64%

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Conclusion

- Present an Interconnect OR Test scheme for interconnect faults in SOC circuits
  - IORT scheme achieves 100% fault detection coverage for each net
  - IORD scheme achieves the maximum diagnosability for each net segment
- Present fast diagnosability check and diagnosis ring generation
  - with theoretical study and integrated them into the IORD algorithm
  - with difference around 6 or 7% between theoretical and experimental results

Conclusion (Cont'd)

- Two optimization techniques
  - Concurrent OR Test (R_c)
    - Under worst case scenario: average within 5% and up to 9.66%
  - Adaptive OR Test (R_a)
    - Improves by 1.23 X to 2.38 X compared with *predetermined diagnosis* R_d
    - with difference of *predetermined detection* IORT (R_t) by 3.21%

Thank you for your Kind Participation!