Cycle Error Correction in Asynchronous Clock Modeling for Cycle-Based Simulation

Junghee Lee and Joonhwan Yi

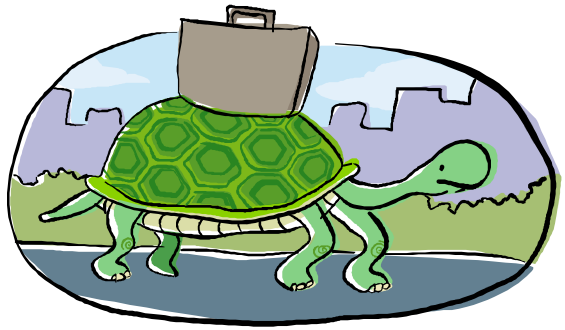
Telecommunication R&D Center
Samsung Electronics

Contents

- Introduction
- Preliminary
- Cycle error
  - Due to asynchronous clock model
  - Due to communicate and update mechanism
- Experiment
- Conclusion
- Reference

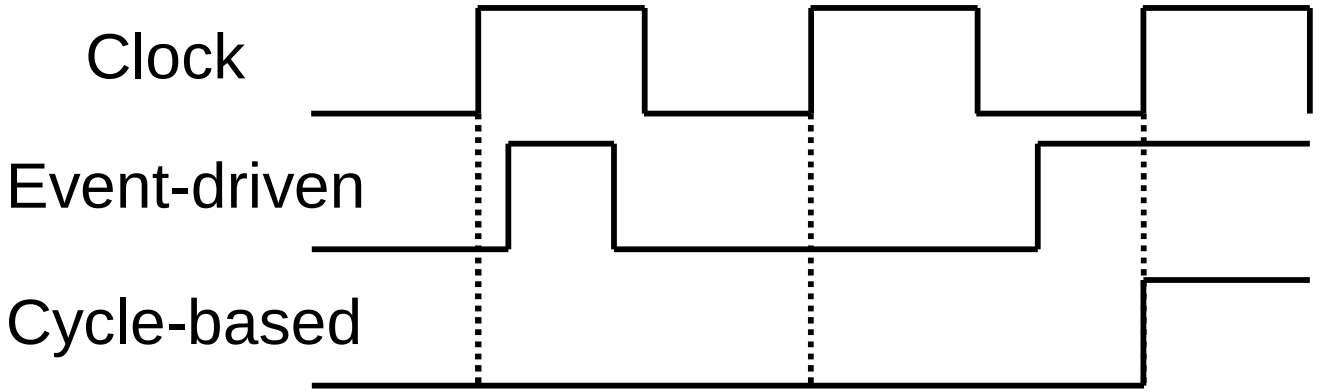
Introduction

- Ever increasing complexity of Systems-On-Chip (SoCs) makes the verification harder and harder.
- Co-simulation/verification of hardware and software is now widely recognized as an important and viable verification approach.
- Traditional event-driven simulator has limitations on run-time performance [1].



Cycle-based Simulation

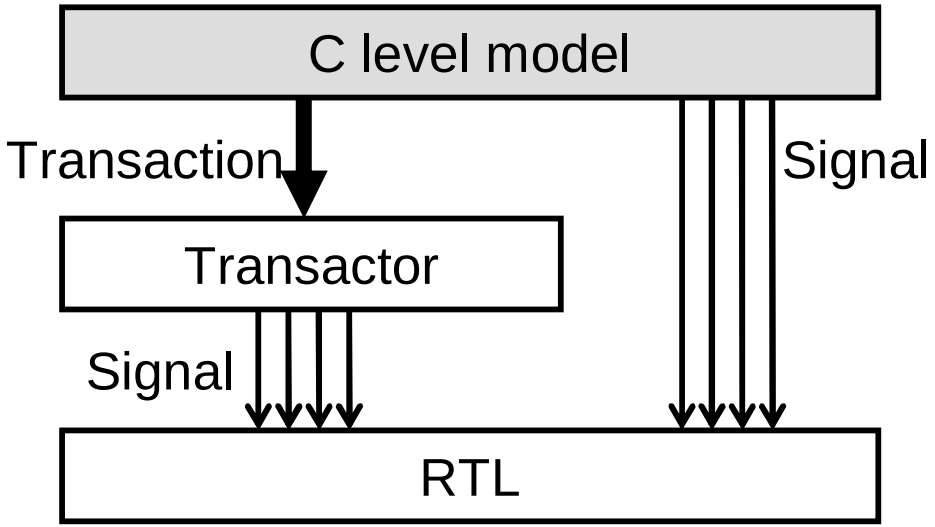
- Benefit
  - Fast simulation speed



- Limitation
  - Handling multiple asynchronous clocks [7].

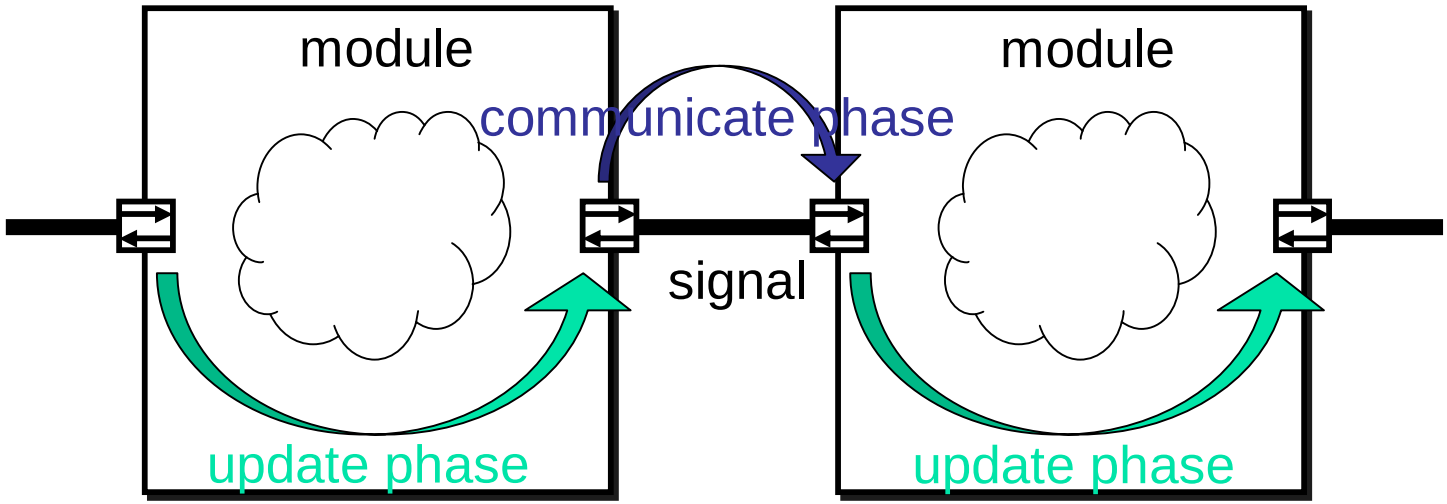
Asynchronous Clock Models

- Approximated as synchronous clocks.
  - Cycle errors are inevitable.
- Verification vector reuse

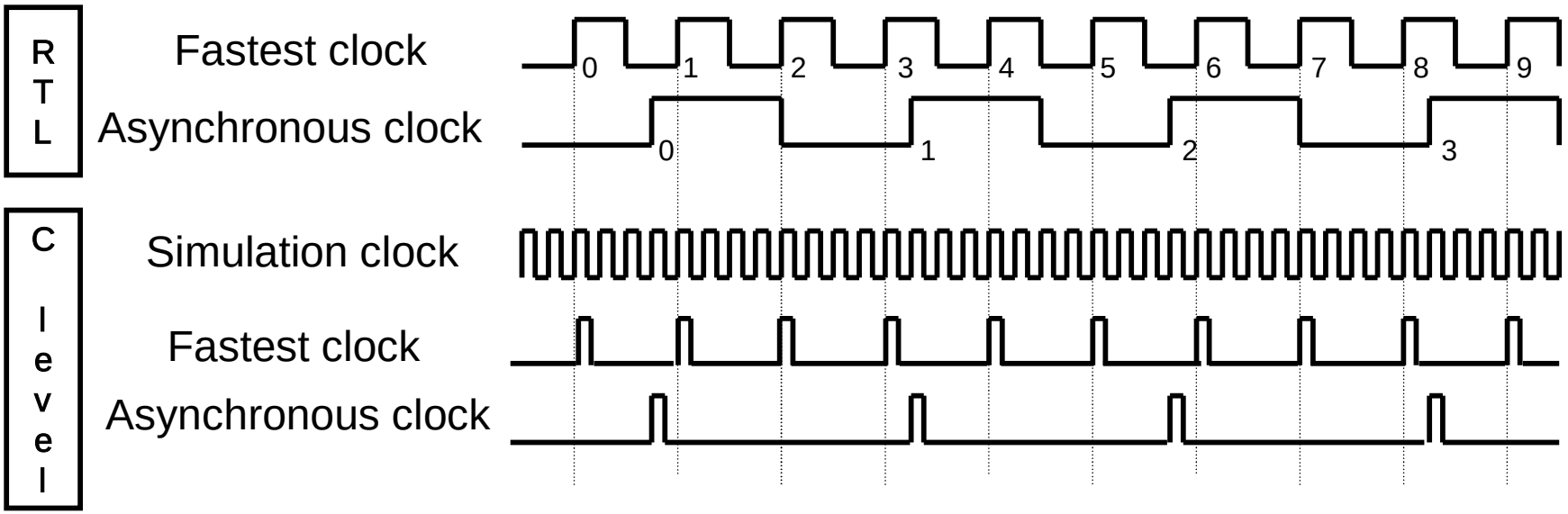


Preliminary

- Simulation clock
  - The only built-in reference clock
- Cycle-based simulation mechanisms
  - Communicate and update mechanism
  - Message-passing mechanism

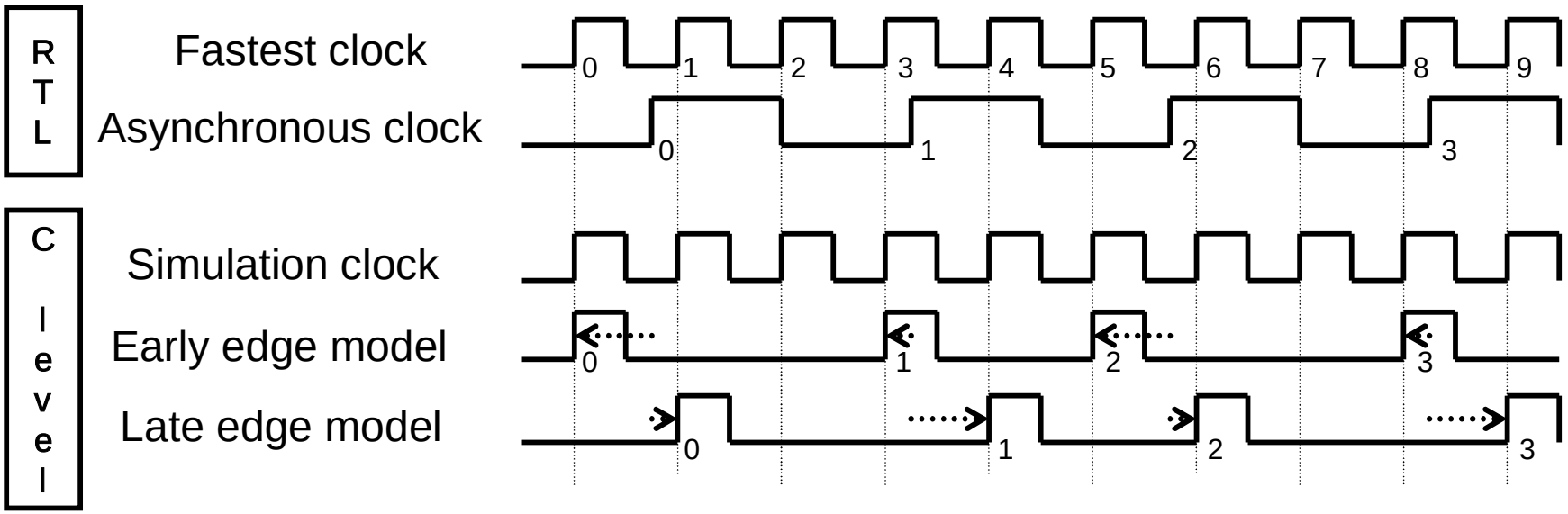


GCD (Greatest Common Divisor) Model



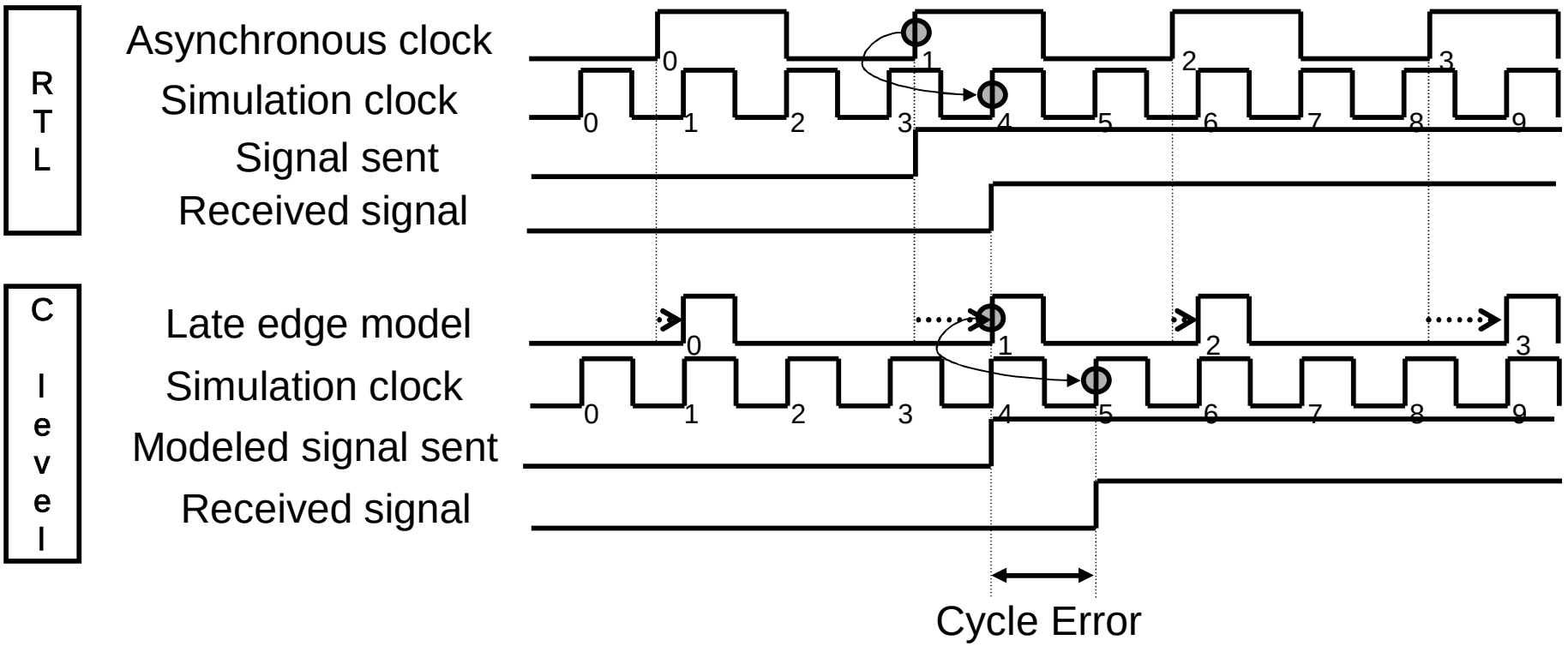
- Accurate and easy to implement.
- Impractical in real systems.

Early/Late Edge Model

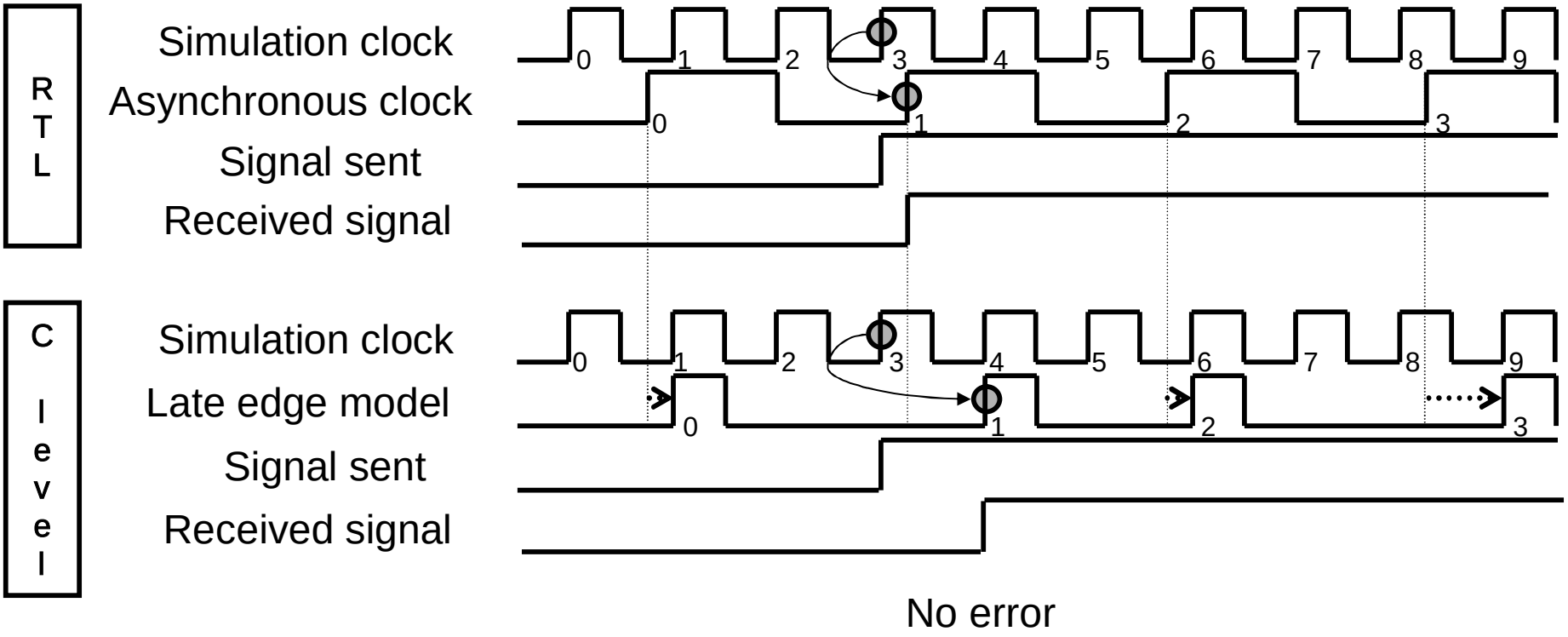


- Maximize the simulation performance.
- Cycle errors at the point of clock domain crossing.

Late Edge Model: Asynchronous to Simulation



Late Edge Model: Simulation to Asynchronous

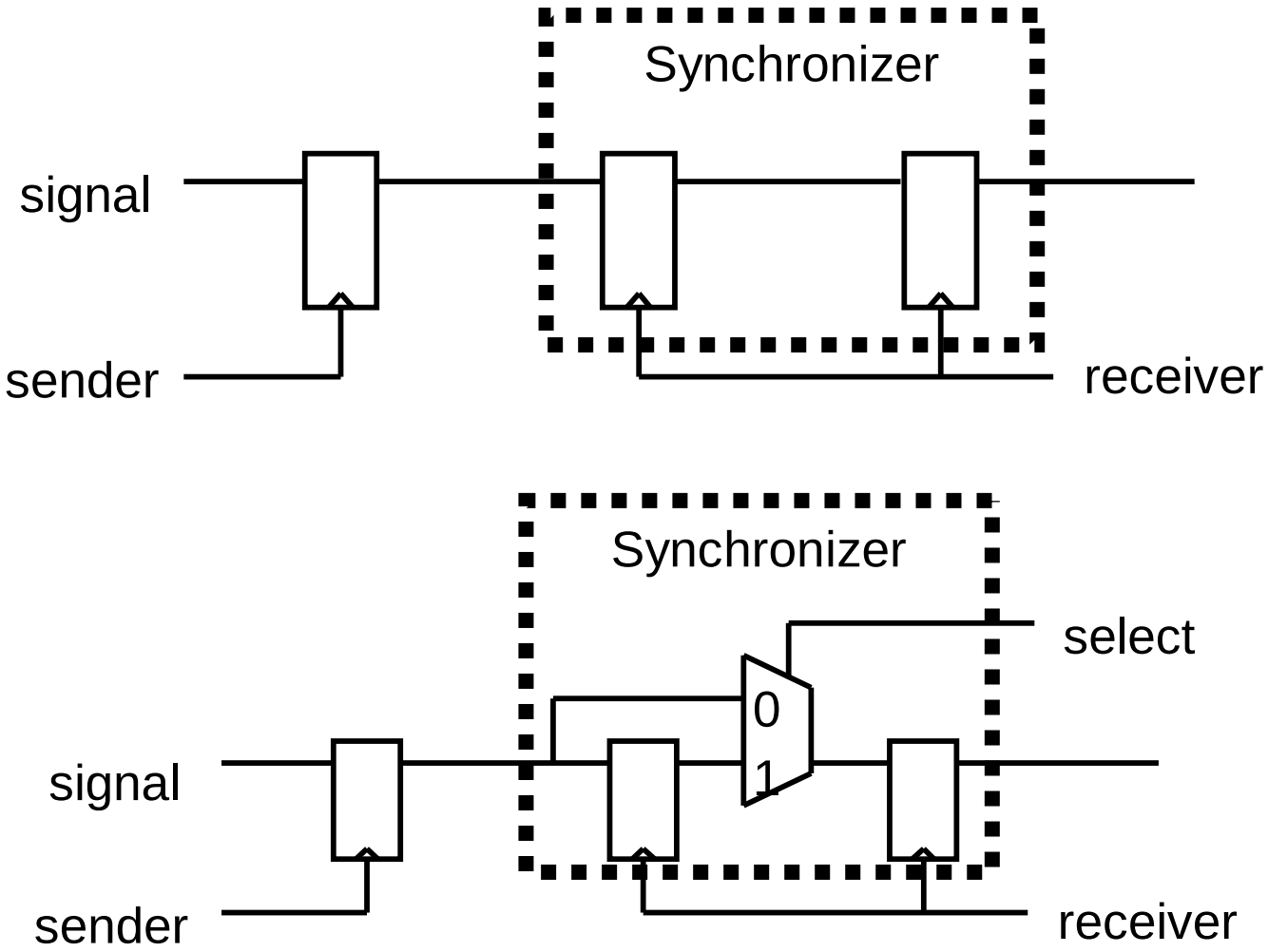


Cycle Errors due to Clock Models

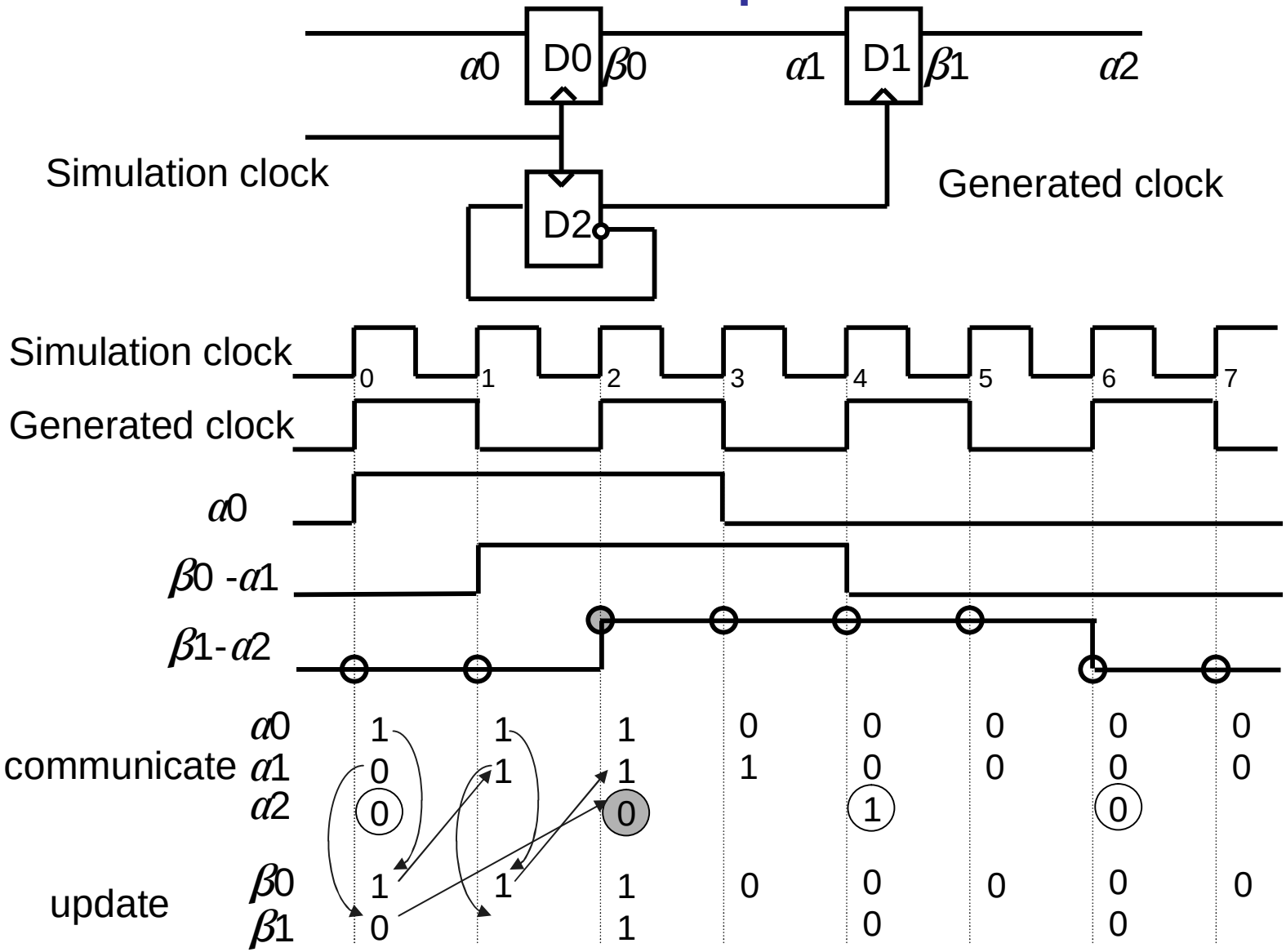
Clock model	Clock domain		Cycle error	Illustrated in
	From	To		
Late edge model	Sim	Async	zero	Slide. 10
	Async	Sim	one or zero	Slide. 9
	Async A	Async B	one or zero	
Early edge model	Sim	Async	one or zero	
	Async	Sim	zero	
	Async A	Async B	one or zero	

- The cycle error is advent when
  - an edge of the simulation clock and one of the asynchronous clock become identical in C-level
  - but their corresponding edges are not identical in RTL

Cycle Error Correction



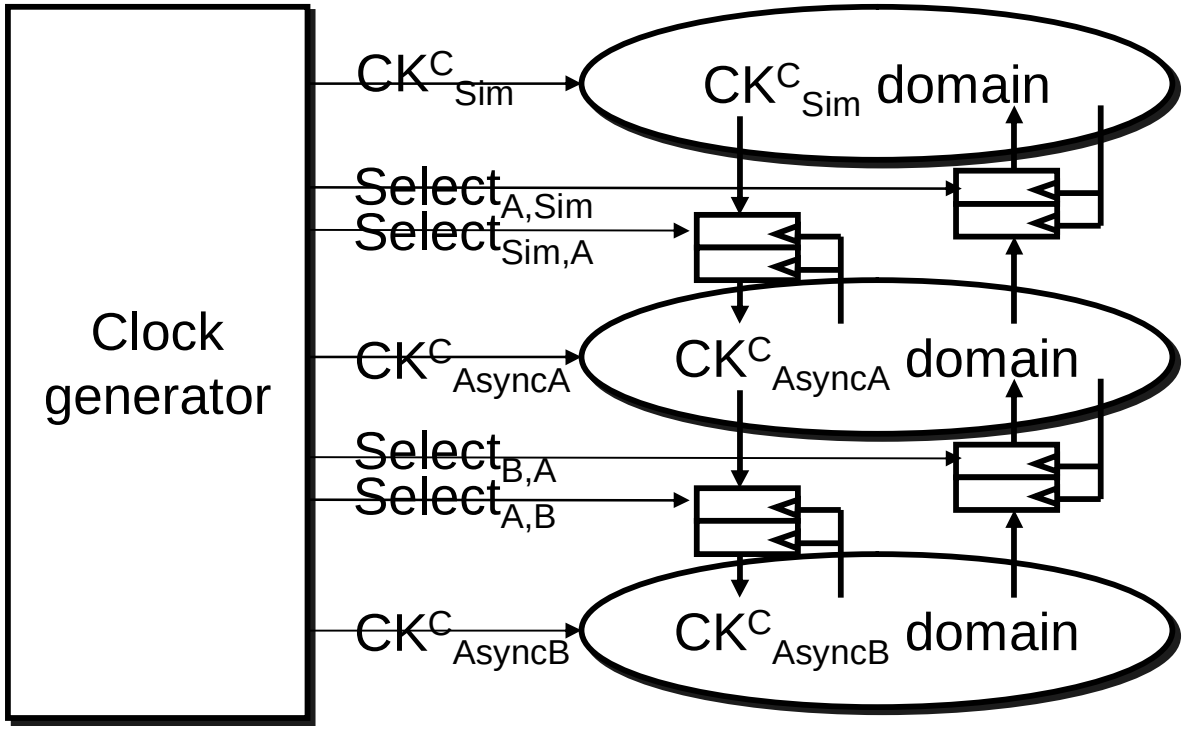
Communicate and Update Mechanism



Cycle Error due to Mechanism

- The method using the proposed synchronizer can be used to correct the cycle errors.
- The clock generator determines that a cycle error occurs …
  - if edges of C-level are identical but the corresponding edges are not in RTL
  - if the edge of the receiving clock is inactive

Experiment



- We simulated the sample circuit on a cycle-based simulator MaxSim [10].
- PC with a 2.53 GHz Pentium 4 processor with 512 MB memories.

Result

	Cycle accuracy			Simulation speed	
	Total clock cycle	Cycle difference	Accuracy	Cycle / sec	Ratio
RTL	93654				
GCD	93654	0	100 %	410702	100.0 %
Late edge model with correction	93654	0	100 %	588638	143.3 %
Late edge model without correction	105669	12015	87.2 %	688227	167.6 %

Conclusion

- Asynchronous clock models
  - GCD model
  - Early/late edge model
  - Early/late edge model with correction
- Overcome the limitation of the cycle-based simulation

Reference

- [1] Lisa Guerra et al., “Cycle and Phase Accurate DSP Modeling and Integration for HW/SW Co-Verification,” Proc. of Design Automation Conference, pp.964-969, 1999
- [2] G. Cabodi et al., “Exploiting timed transition relations in sequential cycle-based simulation of embedded systems,” Proc. of Computers and Digital Techniques, pp.305-312, 2000
- [3] B.H. Yaran, B.H., D. Rahmati, and A.S. Zebardast, “Applying cycle-based simulation technique to VITAL as a VHDL gate level standard,” Proc. of Canadian Conference on Electrical and Computer Engineering, pp.1076-1084, 2001
- [4] L. Ghasemzadeh and Z. Navabi, “A fast cycle-based approach for synthesizable RT level VHDL simulation,” Proc. of International Conference on Microelectronics, pp.281-284, 2000
- [5] Murali Kudlugi, Soha Hassoun, Charles Selvidge, and Duaine Pryor, “A Transaction-Based Unified Simulation/Emulation Architecture for Functional Verification,” Proc. of Design Automation Conference, pp.623-628, 2001
- [6] Kirk Ober, “Doing Behavioral Design the Right Way Minimizes Verification,” Proc. of Design and Verification Conference and Exhibition, 2004
- [7] K. Olukotun, M. Heinrich, and D. Ofelt, “Digital system simulation: methodologies and examples,” Proc. of Design Automation Conference, pp.658-663, 1998
- [8] T.J. Gabara, G.J. Cyr, and C.E. Stroud, “Metastability of CMOS master/slave flip-flops,” Proc. of Custom Integrated Circuits Conference, pp.29.4.1-29.4.6, 1991
- [9] G. Maturana et al., “Incas: a cycle accurate model of UltraSPARC,” Proc. of IEEE International Conference on Computer Design: VLSI in Computers and Processors, pp.103-135, 1995
- [10] MaxSim designer’s guide, AXYS design automation, Inc., 2004
- [11] J. Walker and A. Cantoni, “A new synchronizer design,” Proc. of IEEE Transactions on Computers, pp 1308-1311, 1996