Single-Chip Multi-Processor Integrating Quadruple 8-way VLIW Processors with interface timing analysis considering power supply noise

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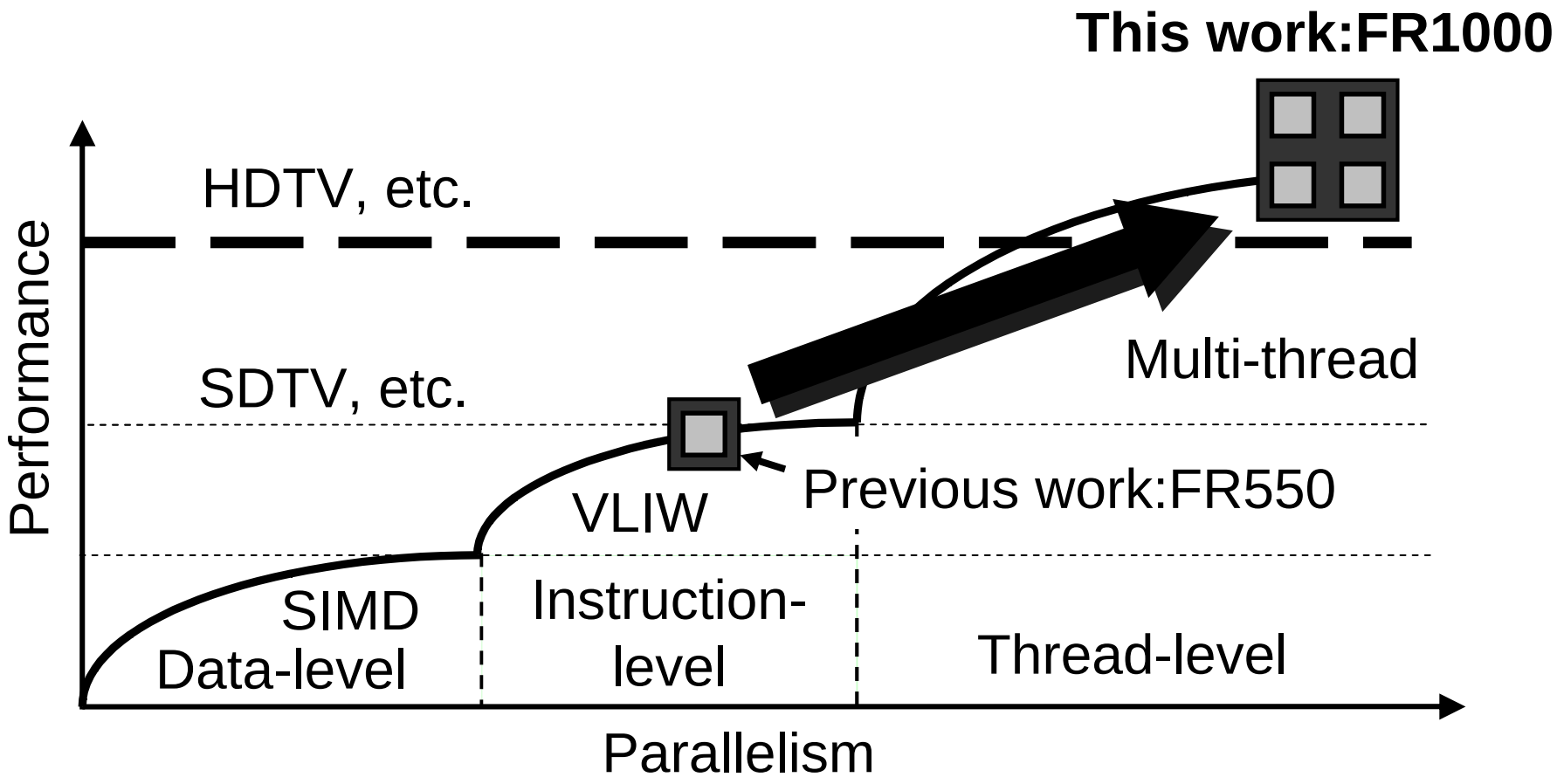
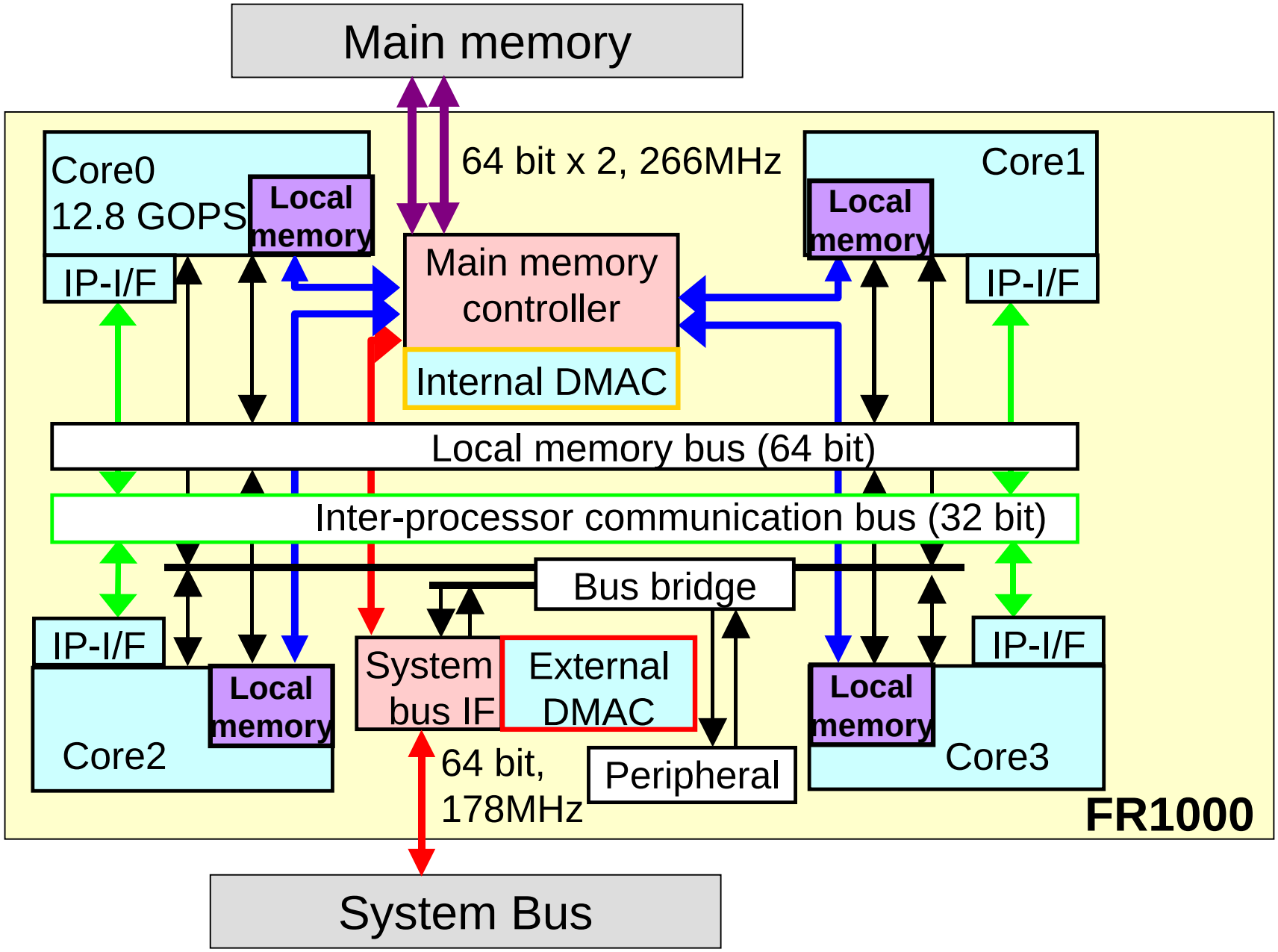
Outline

- Motivation
- Architecture
- Physical design
  - Design flow considering power supply noise
  - LSI model for power integrity analysis
  - Interface analysis example
- MPEG2 MP@HL decoding on evaluation board
- Summary

Motivation: high performance and low power

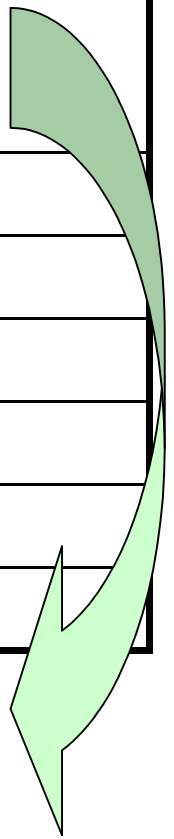


FR1000 block diagram



FR1000 chip specifications

Core	4 cores with 8-way VLIW architecture
Memory	32 KB+32 KB/core (D-cache, I-cache) 128 KB/core (Local memory)
DMA controller	16 ch (Internal) , 16 ch (External)
Interface	Main memory 266 MHz 64 bit x 2 ch System Bus 178 MHz 64 bit
Technology	**90-nm** CMOS, 9-metal layers
Transistor count	28M (Logic), 55M (Memory)
Operating frequency	533 MHz @1.2 V
Power consumption	**3.0 W** @1.2 V, 533 MHz
Package	900-pin FCBGA
size	**11.9 mm x 10.3mm**



High speed interface cause power supply noise issue

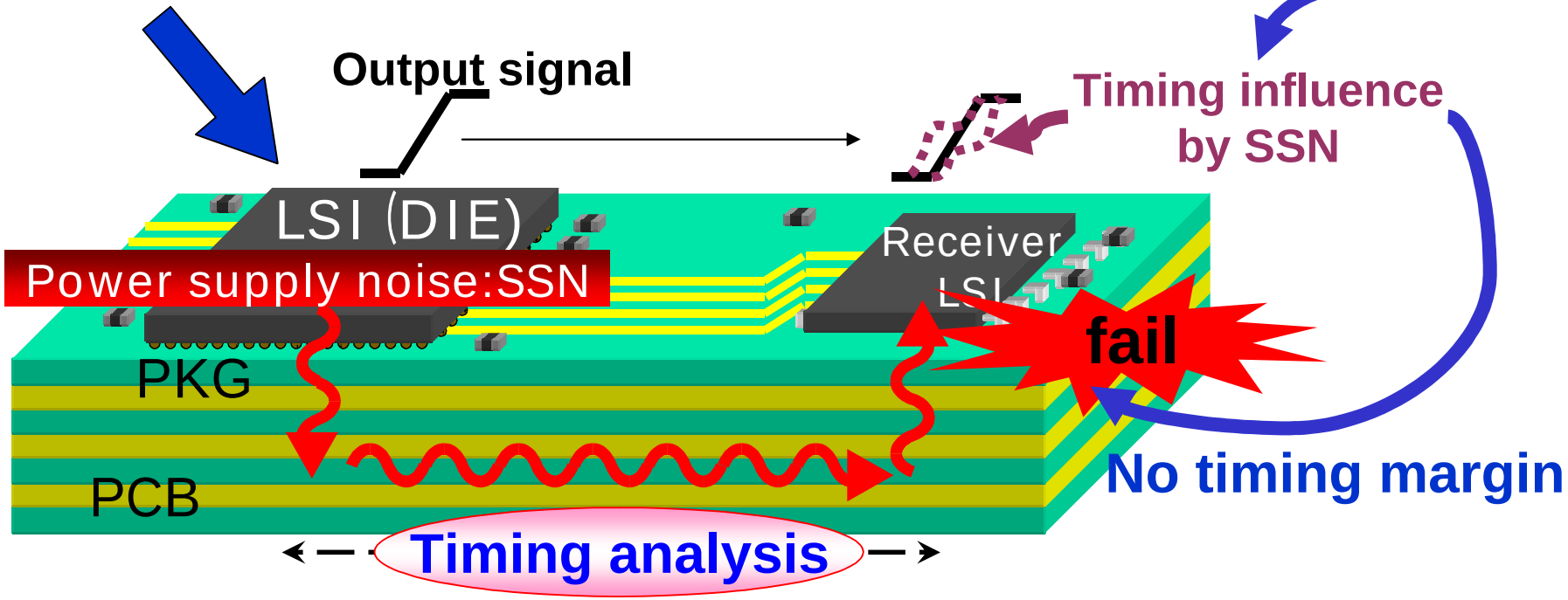
Power integrity issue on system board

Technology scaling

signal I/O frequency
signal I/O number

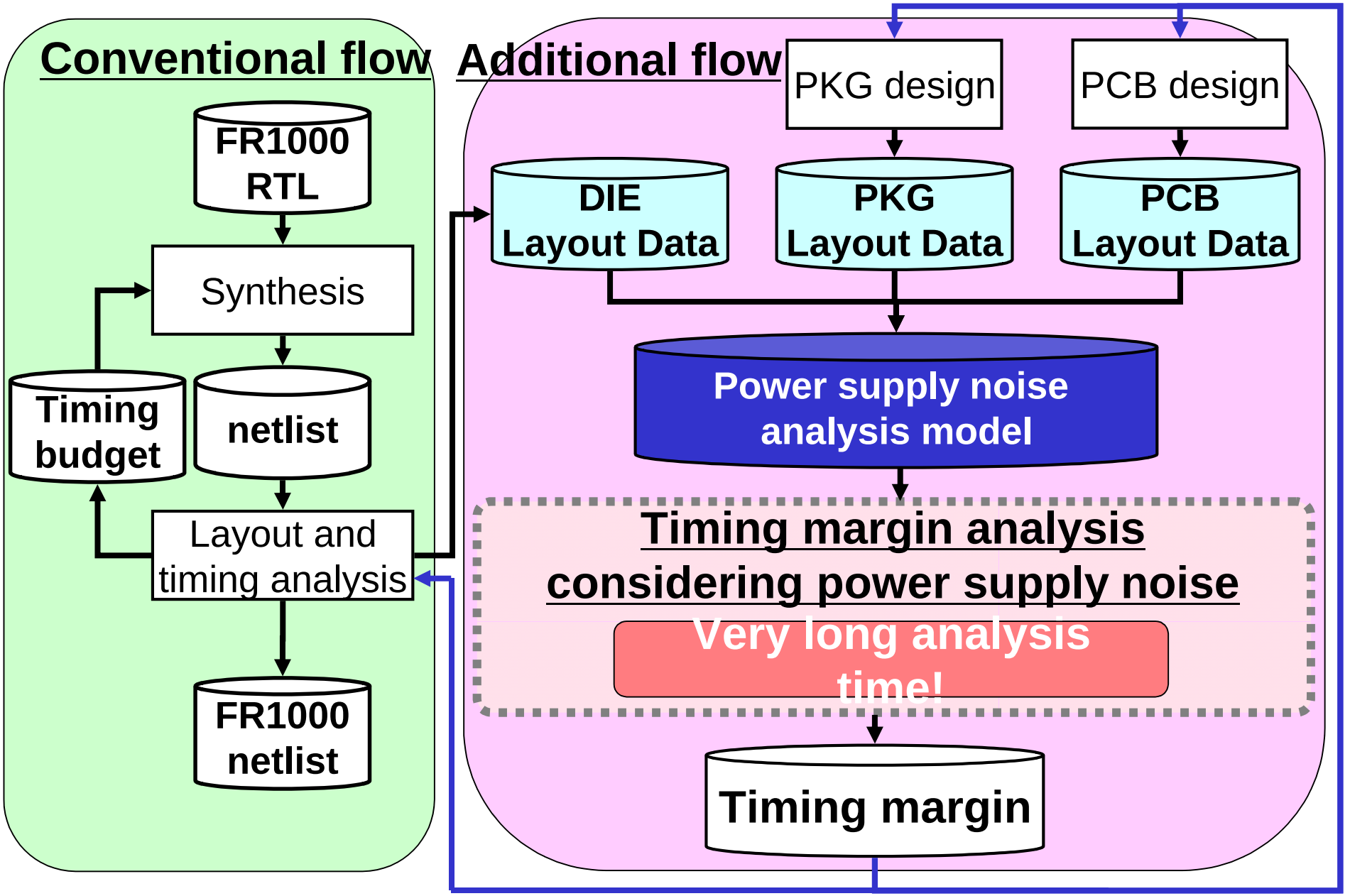
Increase of noise

FR1000: 230SSTL I/O buffers, 2ch 266MHz

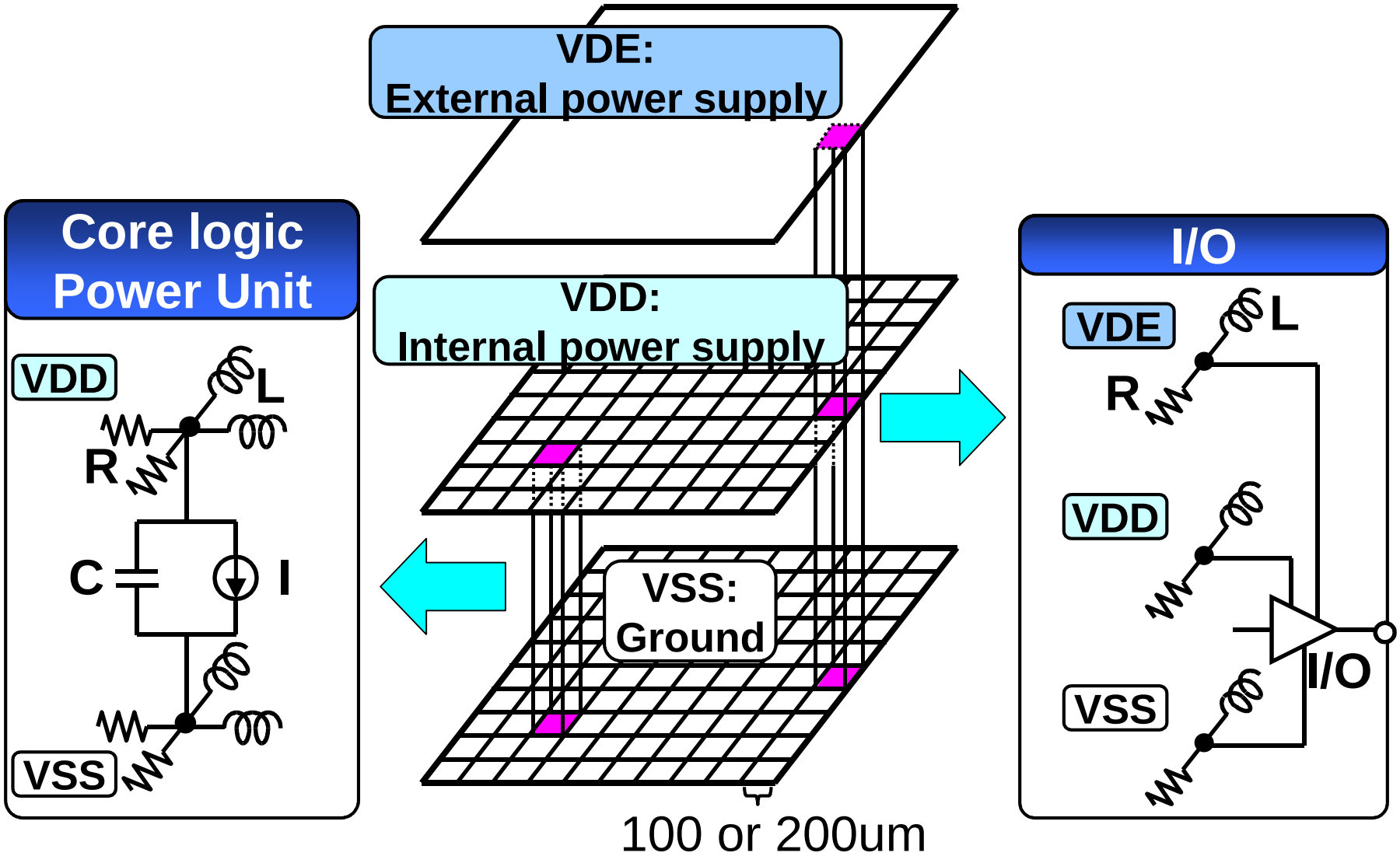


Timing margin analysis considering power supply noise of DIE, PKG and PCB is required

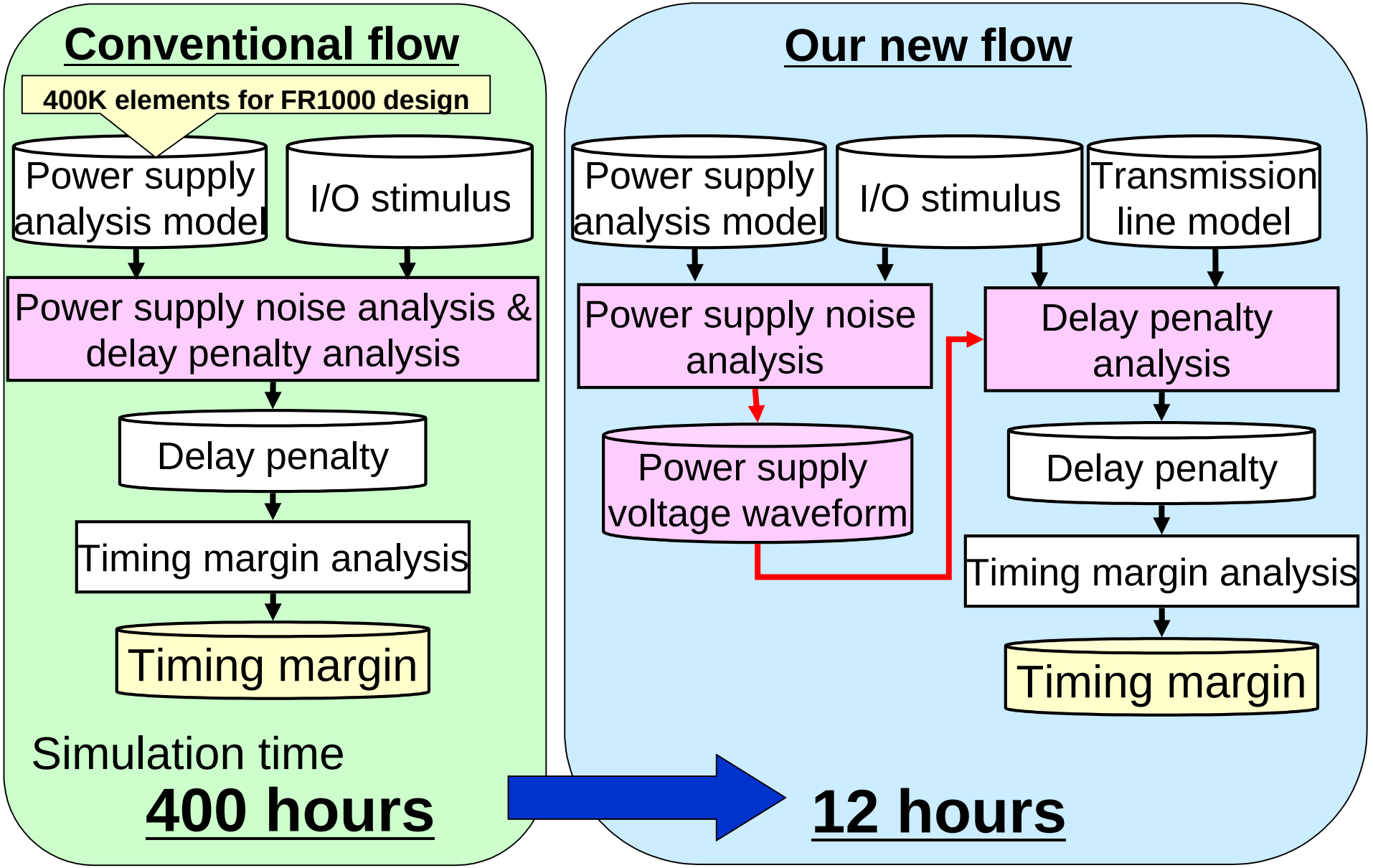
Design flow considering power supply noise



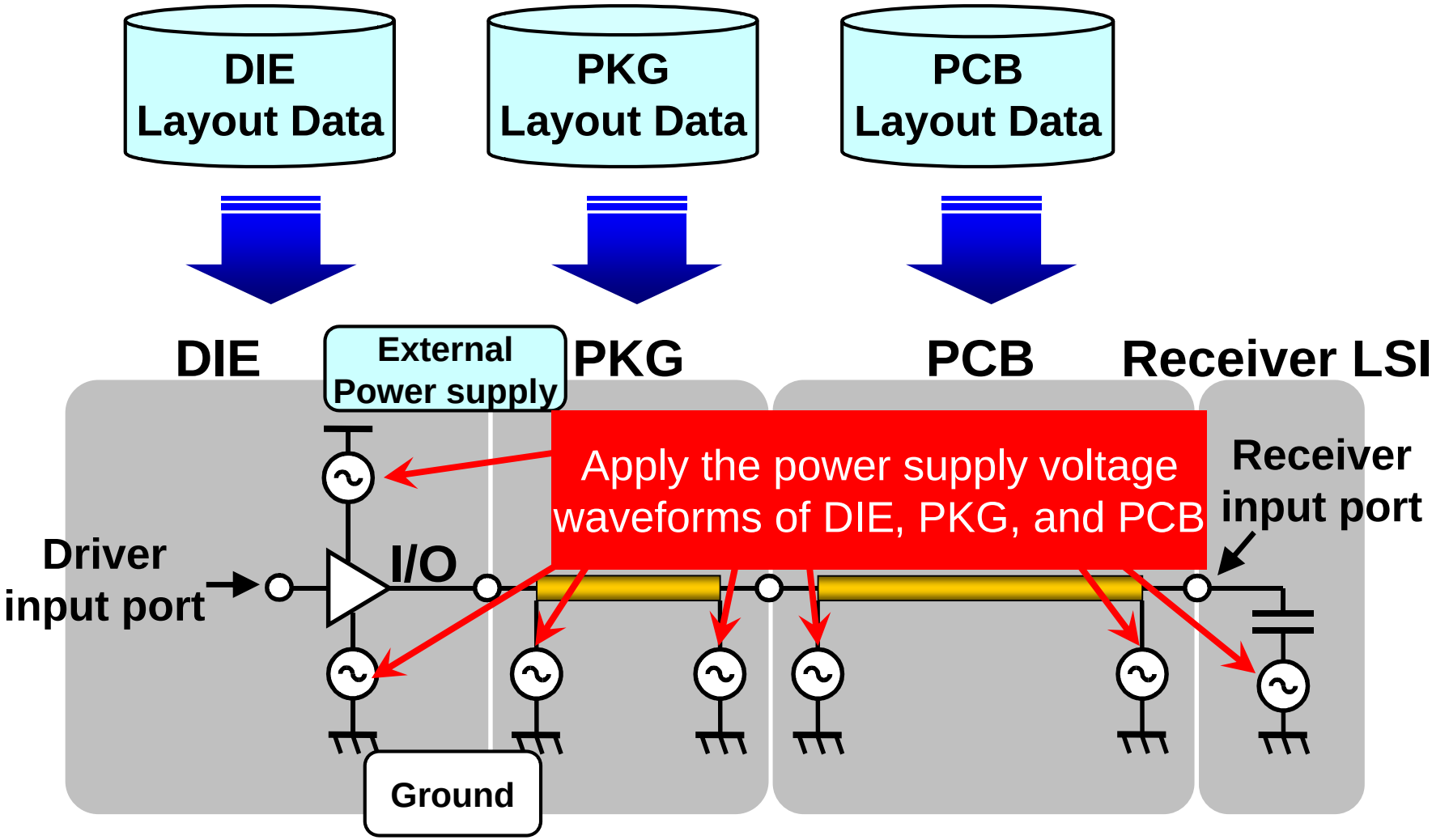
LSI power analysis model



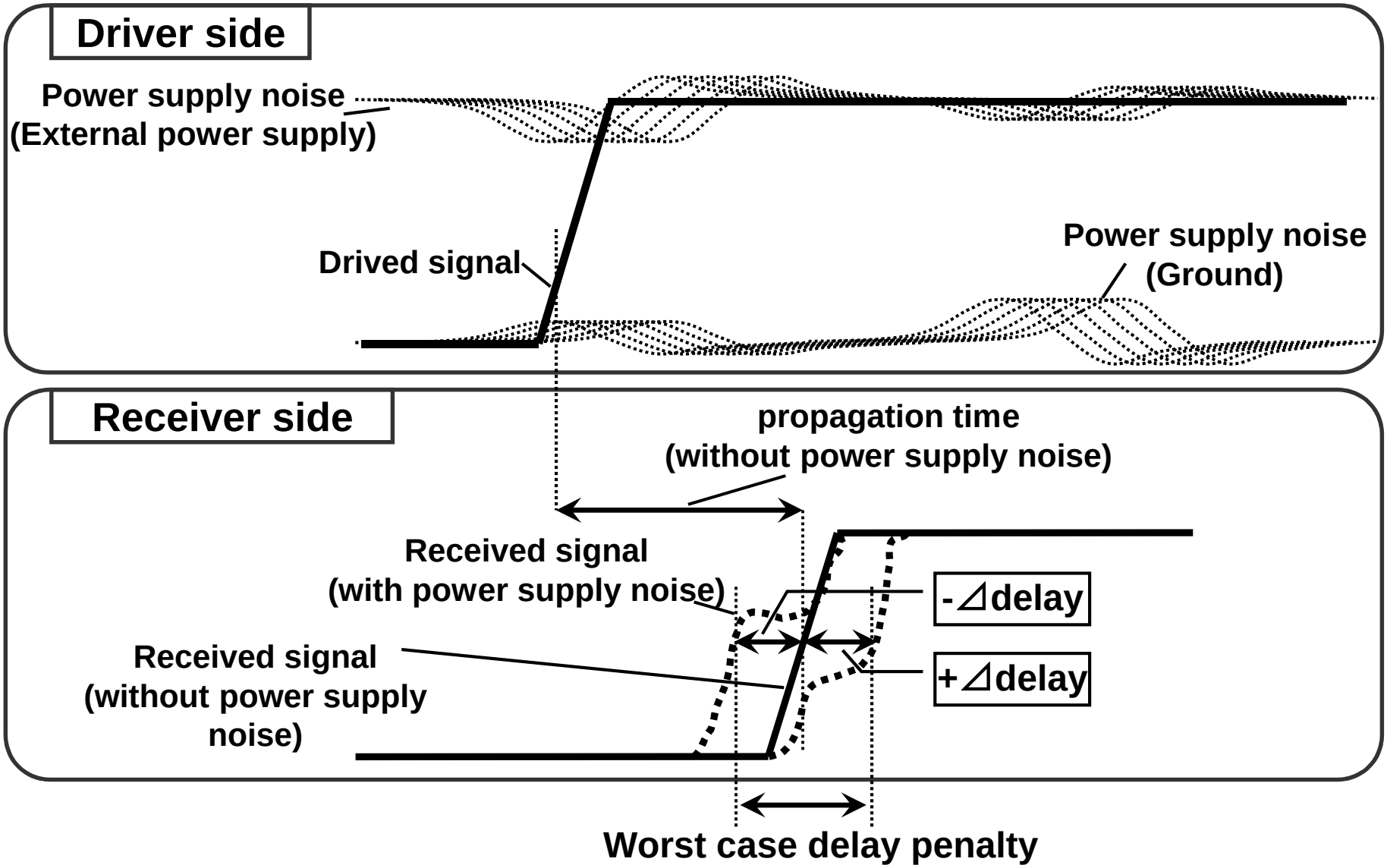
Our timing margin analysis flow



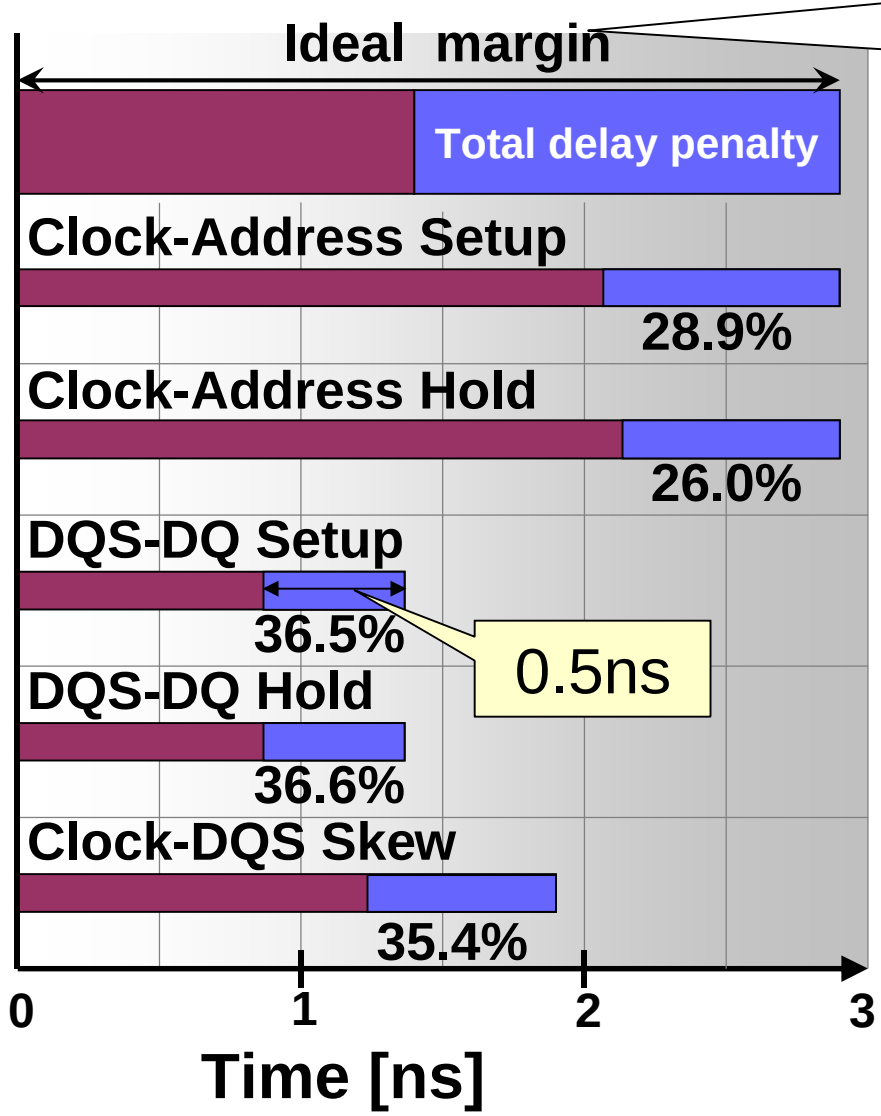
Transmission line model



Delay penalty by power supply noise analysis method



Analysis result of main memory interface



The margin without considering any delay penalty

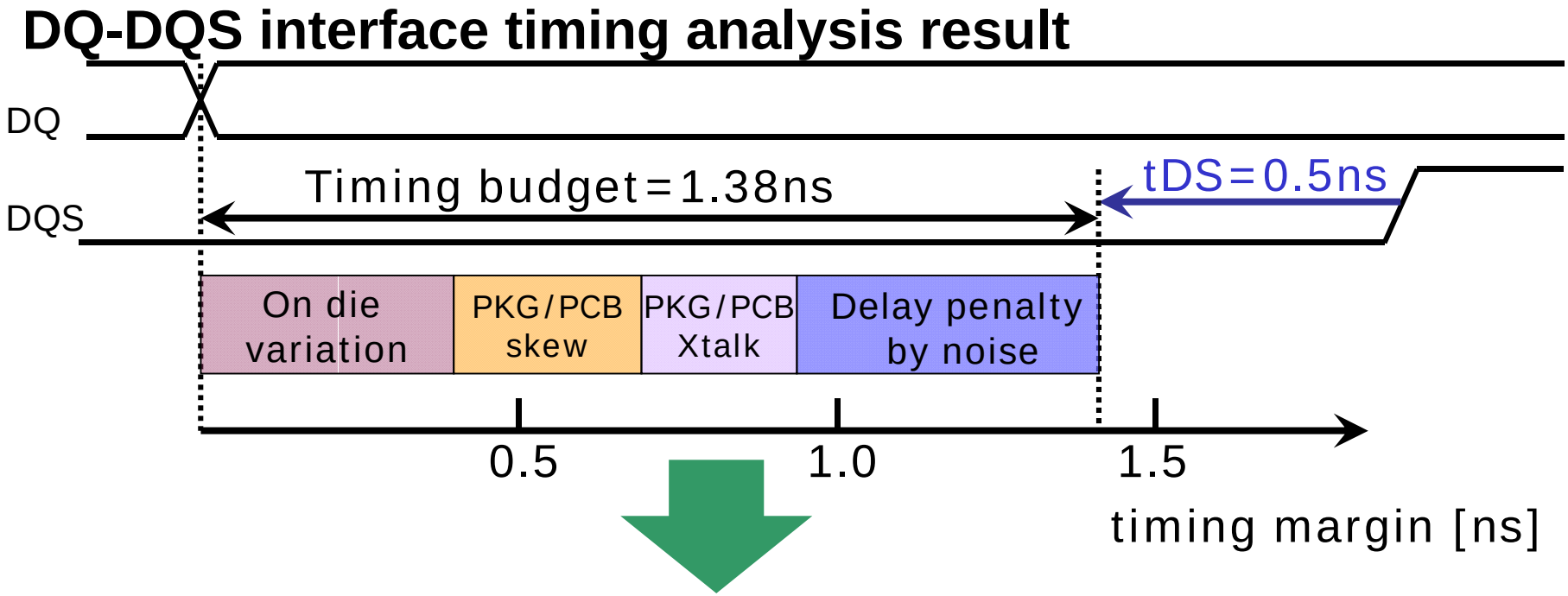
DQ:Data

DQS:Data strobe

Analysis condition

Process	slow
Voltage	VDE=2.3V , VDD=1.1V
Temperature	125℃
I/O	All active
Core logic	stop

PCB/Package design guideline



PCB/Package design guideline

- Power

  Plane resource, Decoupling capacitors

- Signal

  Layer usage, Line width/length/spacing

MPEG2 MP@HL decode for HDTV on FR1000

Summary

The low power single-chip multi-processor FR1000

-4 processor cores, internal DMAC, external DMAC

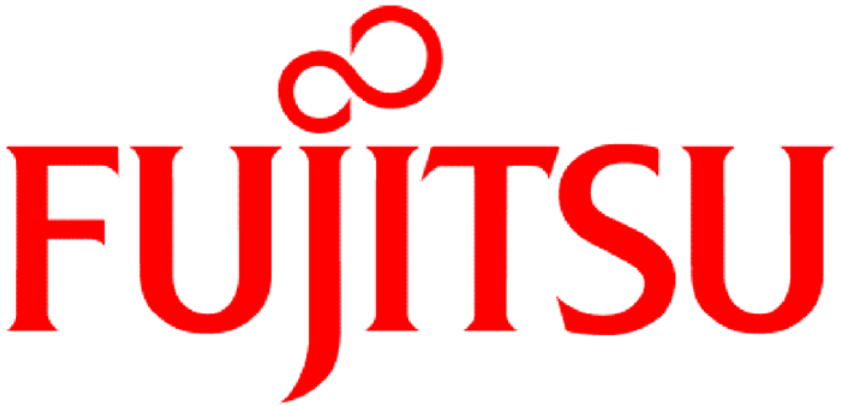
-MPEG2 MP@HL without any dedicated circuits

-3.0W@1.2V, 533MHz

Introducing interface timing analysis considering power supply noise

-DIE(LSI) noise model development

-Timing analysis method at shorter times



THE POSSIBILITIES ARE INFINITE