Mathematically Assisted Adaptive Body Bias (ABB) for Temperature Compensation in Gigascale LSI Systems

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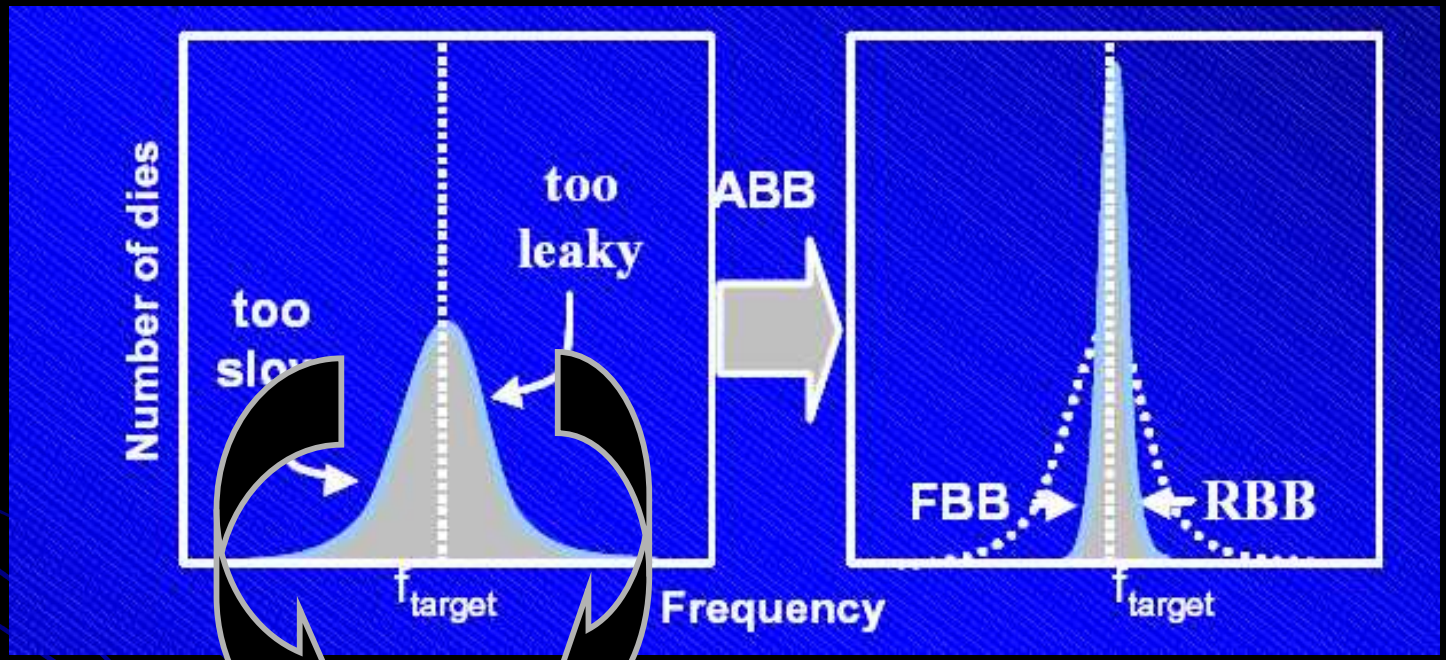
Outline

- Motivation
- Problem Statement
- Implementation Overview
- CAD Level Solution
- Experimental Results
- Conclusion

Motivation



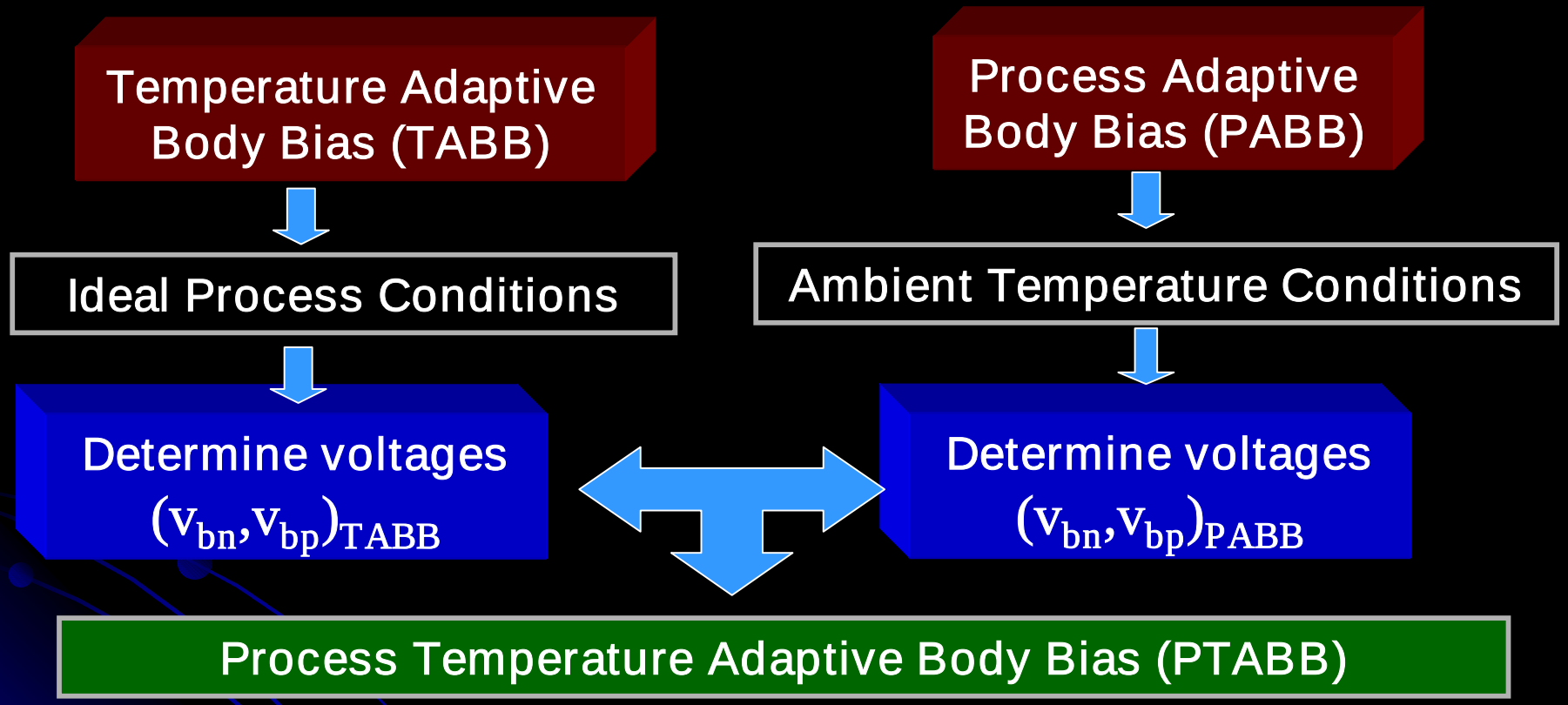
caused due to temperature and process variations

S.Borkar [Intel]

Problem Statement

- Determine the right amount of body bias to compensate for
  - process variations
  - temperature variations
- Generalized framework for
  - one-time compensation
  - run-time compensation
- Provide a CAD level solution to the problem of determining the exact body bias values.

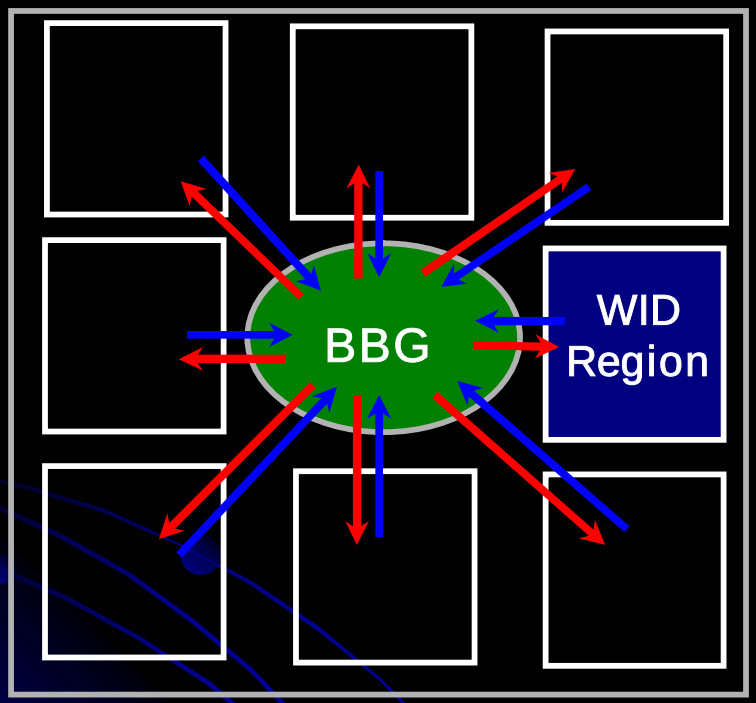
Our approach



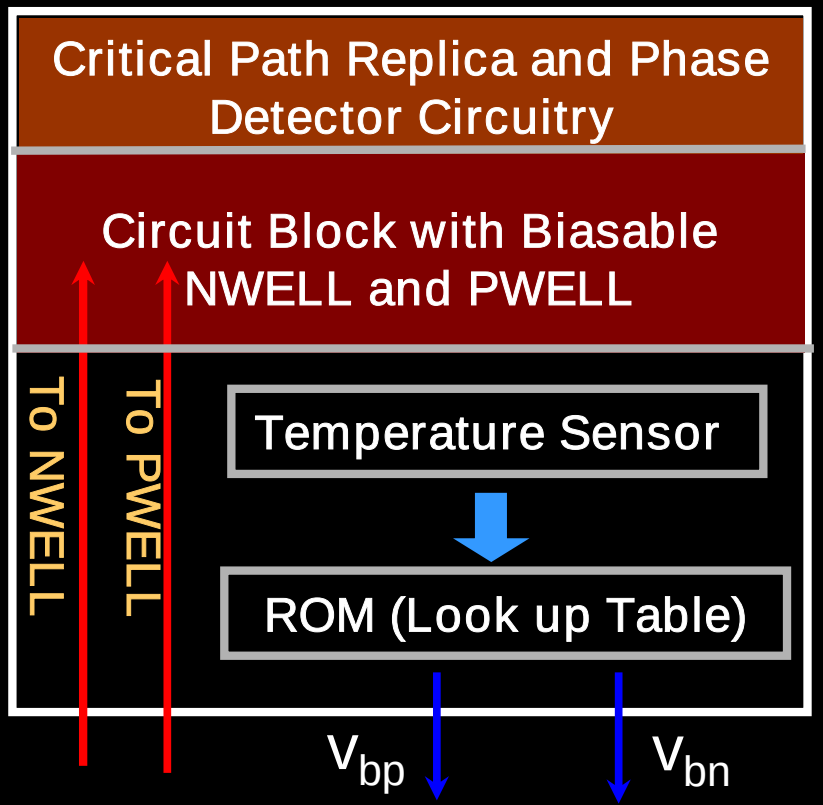
Compute voltages $(V_{bn},V_{bp})_{PTABB}$

Works at all temperatures for within-die variations

System Level Block Diagram



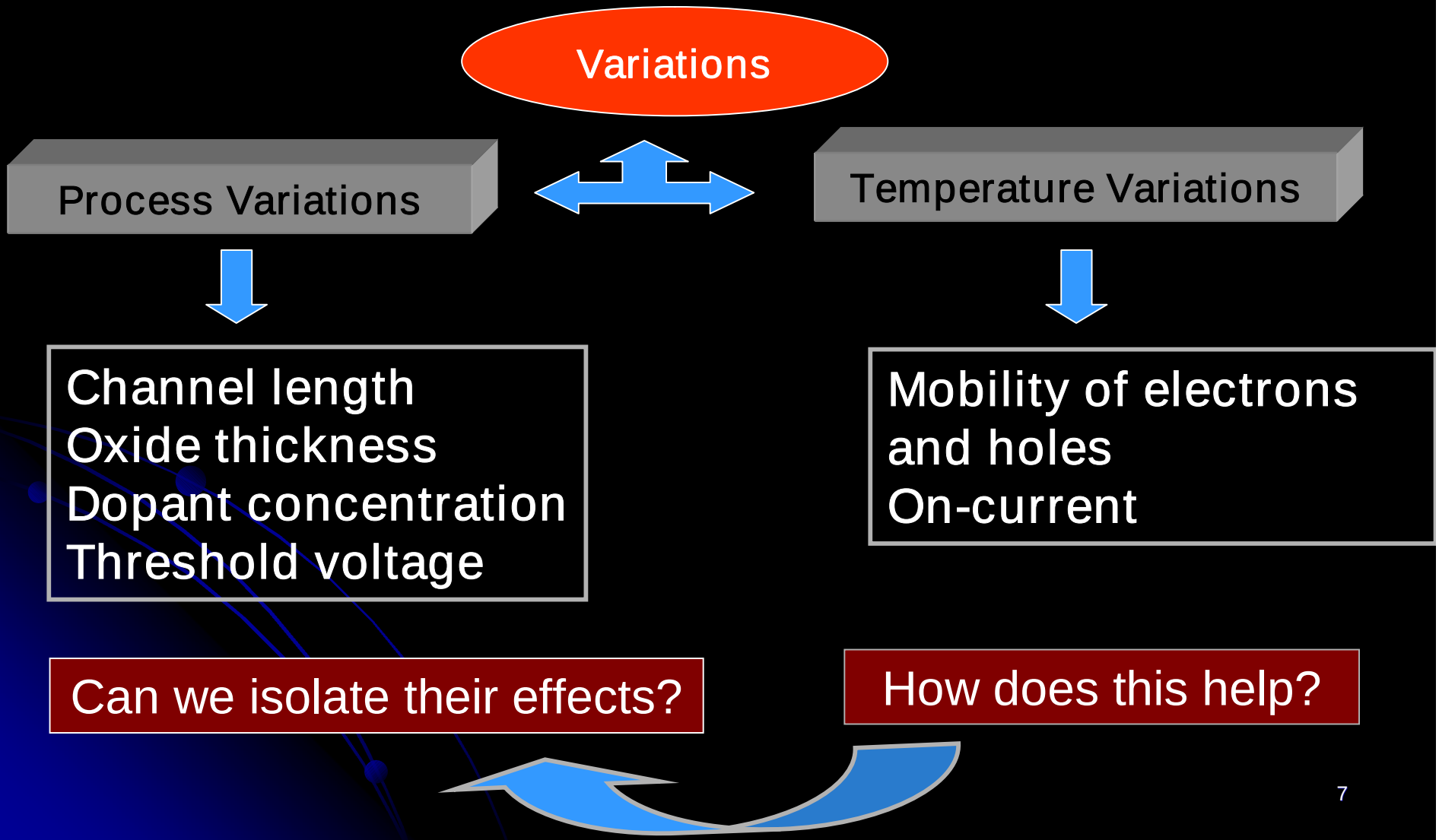
BBG: Body Bias Generator
(can be central or local)



From Body Bias Generator

To Body Bias Generator

Independence of Variations



Simulation Results for a Ring Oscillator

Temperature = 50ºC Process Corner = Low V_t Nominal Delay = 151ps

Delay through SPICE simulations = 145.6ps

ΔDelay = -5.4ps

Delay at T=50ºC & nominal process corner = 154.9ps

ΔDelay = 3.9ps

Delay at low V_t process corner & nominal temperature = 141.8 ps

ΔDelay = -9.2ps

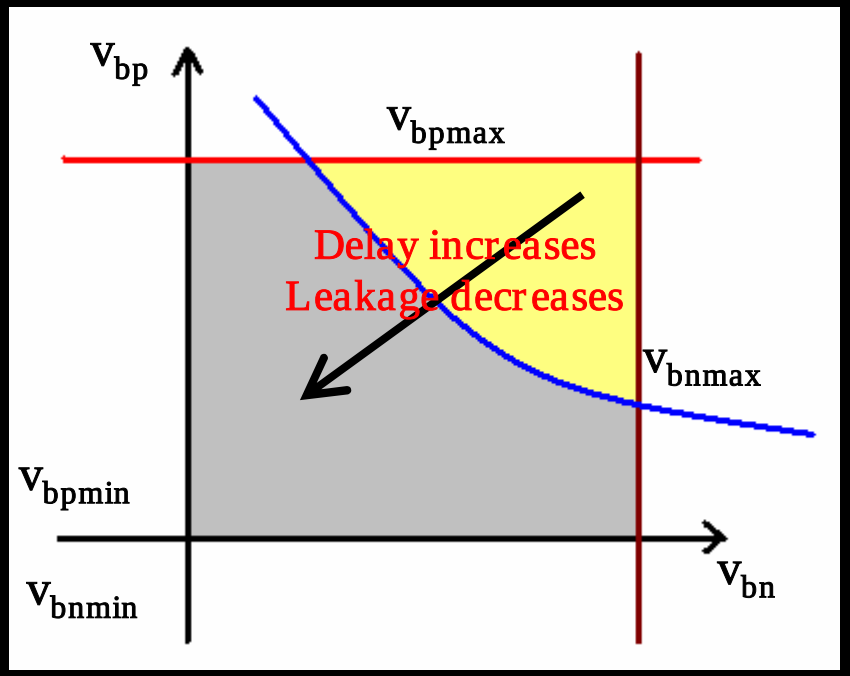
Delay using the principle of superposition = 145.7 ps

ΔDelay = 3.9ps – 9.2ps = – 5.3ps

% Error = 1.8

Temperature Compensation

Determine the exact body bias voltage $(V_{bn},V_{bp})_{TABB}$ at each temperature point assuming ideal process conditions.



Performed using deterministic simulations

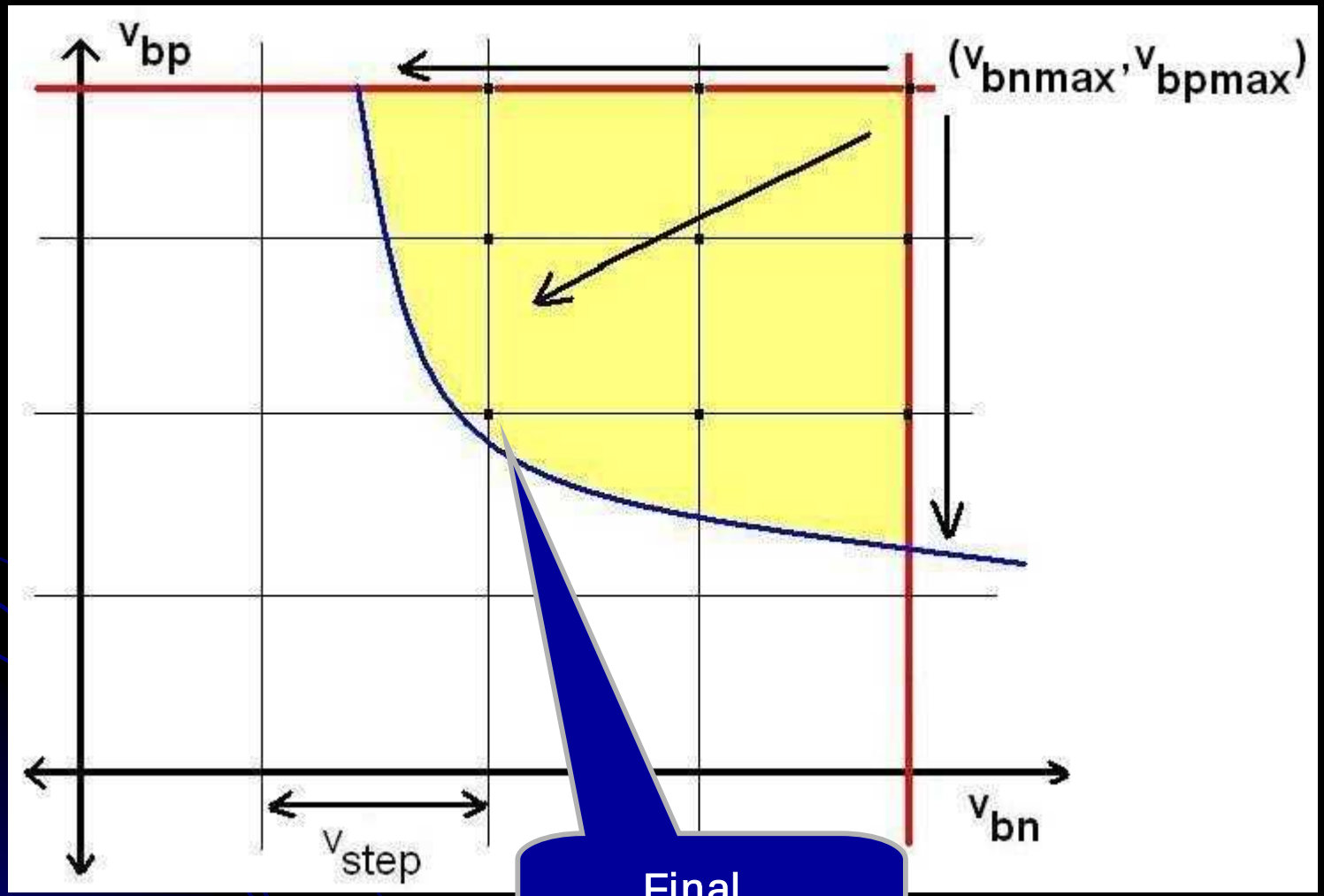
Mathematically assisted TABB

Bounded enumeration based TABB

Set of points which do not meet delay

Set of points which meet delay

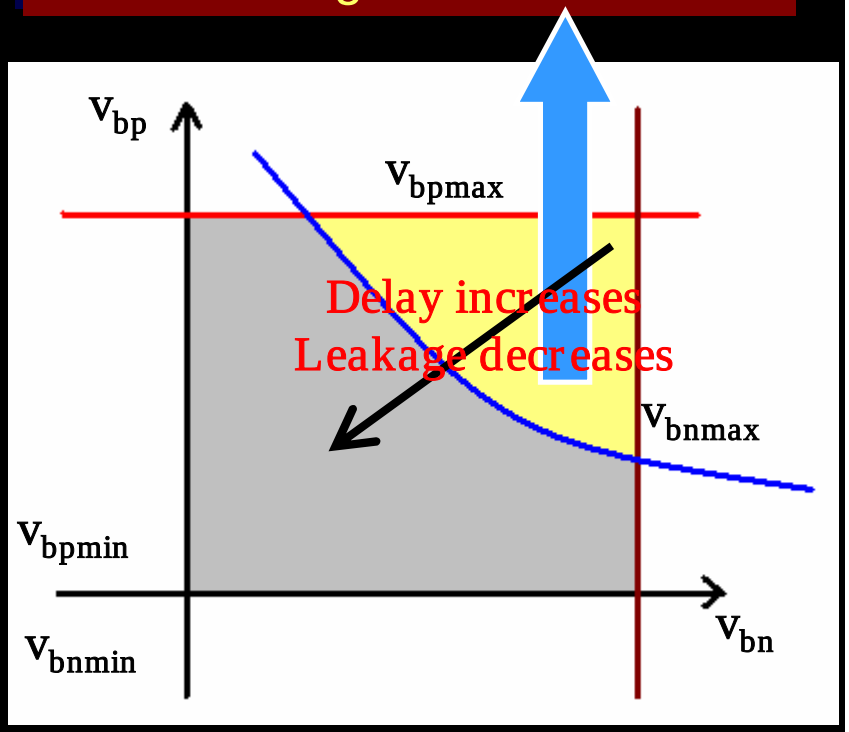
Bounded Enumeration based TABB



Mathematically Assisted TABB

- Problem statement (NLPP) :
  - Minimize $L(v_{bn},v_{bp})$ s.t.
    - $D(v_{bn},v_{bp}) \leq D^*$
    - $v_{bnmin} \leq v_{bn} \leq v_{bnmax}$
    - $v_{bpmin} \leq v_{bp} \leq v_{bpmax}$.
- Need models for $L(v_{bn},v_{bp})$ and $D(v_{bn},v_{bp})$.
- Use 2nd order polynomial best fit expressions.
- Measure leakage and delay at sample points through deterministic simulations.

Find the exact solution which lies along the blue line.



Set of points which do not meet delay

Set of points which meet delay

Solving the NLPP

$$D(v_{bn}, v_{bp}) = D_0[\sum_{i=0}^{2}(\sum_{j=0}^{2} a_{ij} v_{bn}^{j}) v_{bp}^{i}]$$

Express delay as a product of two independent polynomials

$$D = h(v_{bn}, v_{bp}) \approx f(v_{bn}) * g(v_{bp})$$
$$f(v_{bn}) = 1 + x_1 v_{bn} + x_2 v_{bn}^2$$
$$g(v_{bp}) = 1 + y_1 v_{bp} + y_2 v_{bp}^2$$

Eliminate one variable (say V_{bn})

Express L in terms of v_{bp} and find the minimum value using Newton Raphson method.

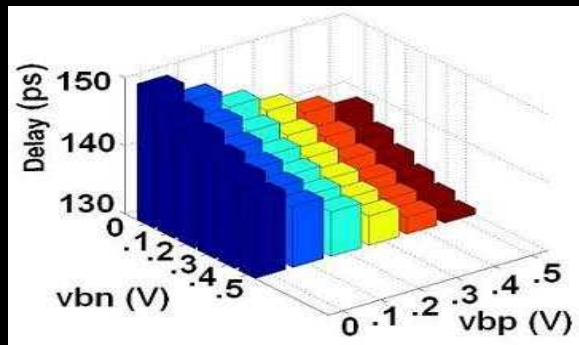


Fig 3(a). Delay of the RO at various points obtained through HSPICE simulations.

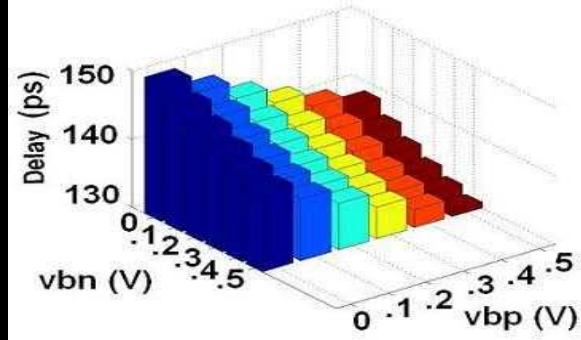


Fig 3(b). Delay of the RO at various points obtained by multiplying curve fitted data for vbn and vbp.

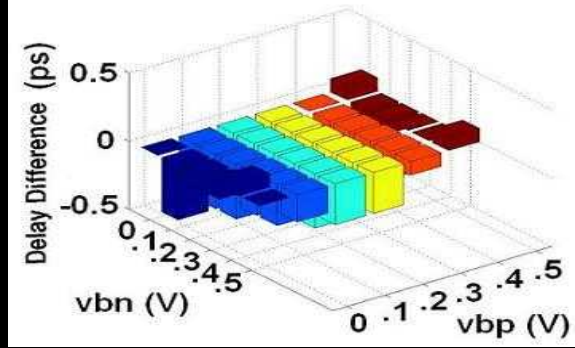


Fig 3(c). Difference in delay between HSPICE simulations and curve fitted values.

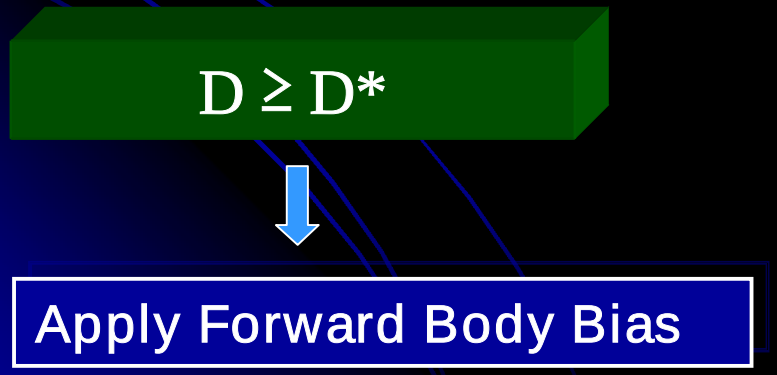
Comparing the 2 methods

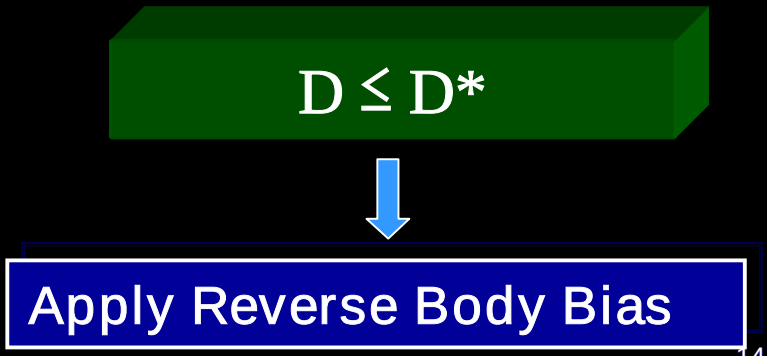
- **Bounded Enumeration based TABB**
  - Highlights
    - Simple
    - Few computations
  - Drawbacks
    - Depends on the granularity of the voltages
    - Worst case complexity $O(n^2)$
    - Round-off error due to minimum voltage resolution
- Mathematically assisted TABB
  - Highlights
    - No elaborate search
    - Does not depend on the voltage resolution
    - Exact solution (which can be added with PABB)
  - Drawbacks
    - 1% modeling error
    - Overkill for P-well processes
    - Can be slower than TABB (if search space is limited)

Process Compensation

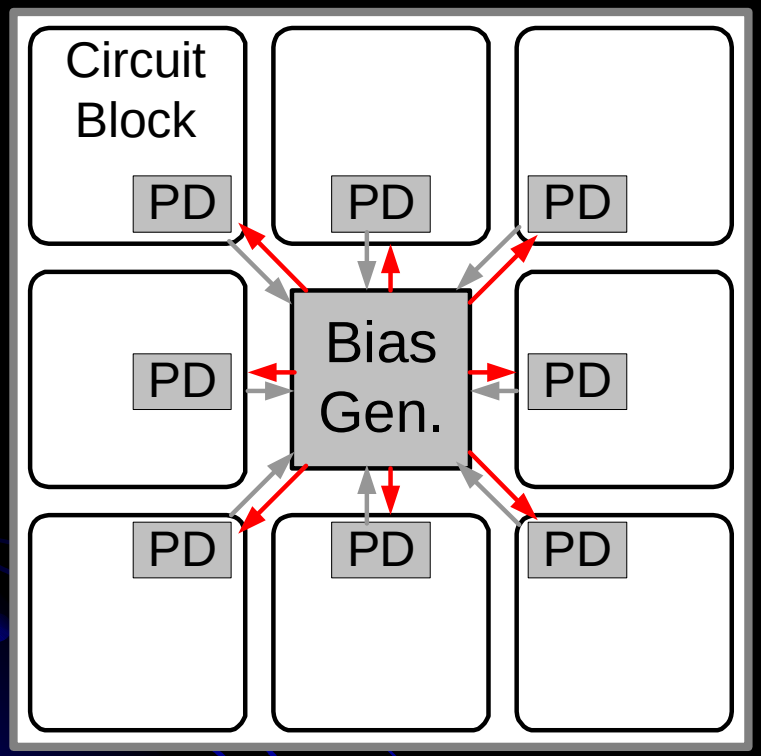
- Problem Statement:
  - Determine the body bias pair (v_{bn},v_{bp}) for each WID variational region of each die at room temperature.

Measure the delay and leakage of each WID variational region at room temperature.

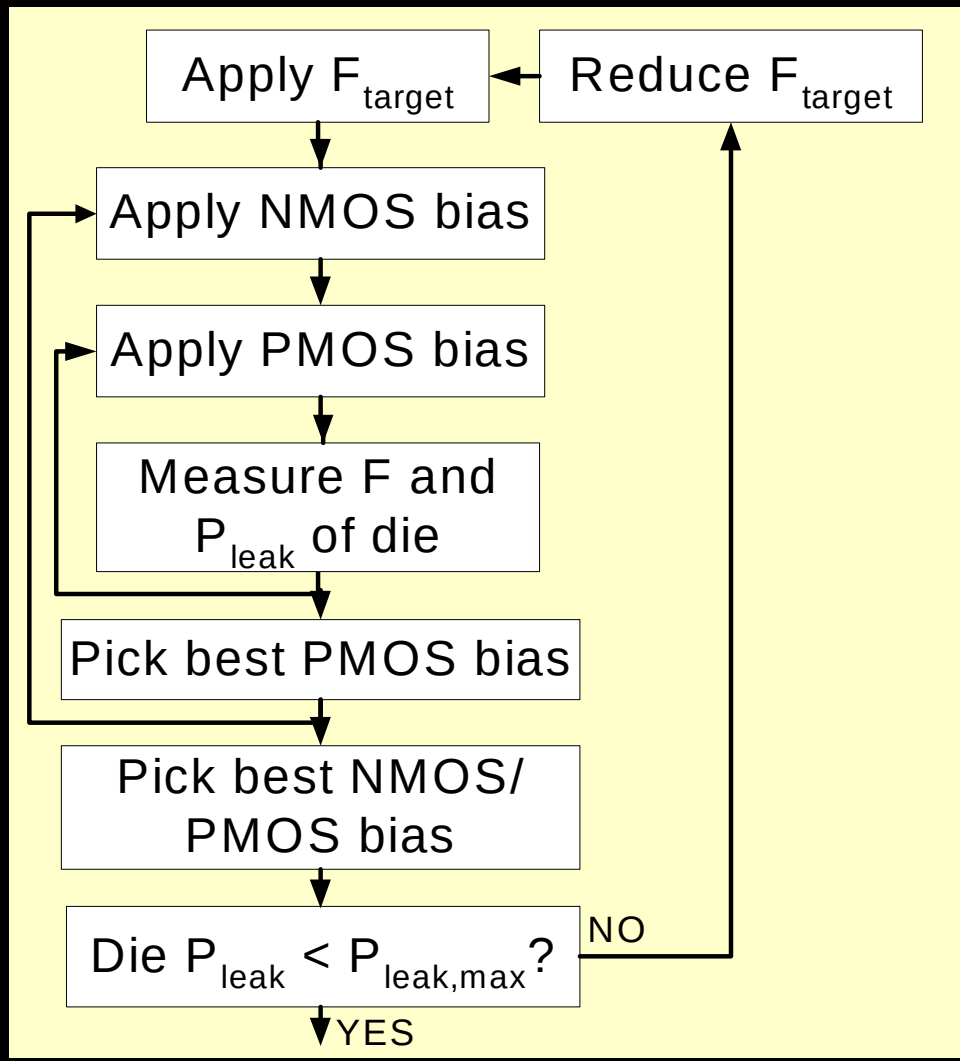




Adaptive Body Bias (ABB)

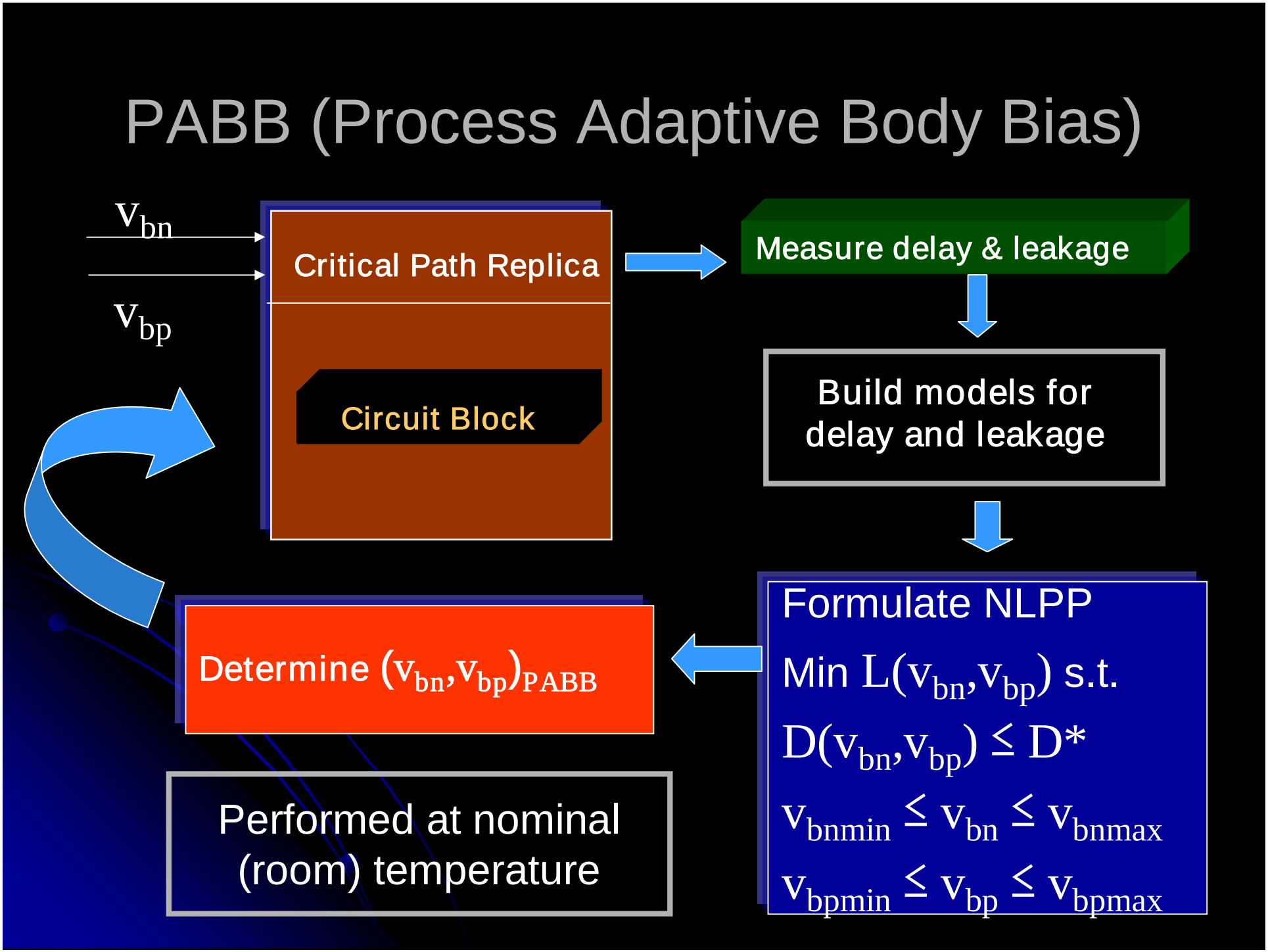


Accounts for WID variation



[Intel]

PABB (Process Adaptive Body Bias)



Simulation Set-up for PTABB

- ISCAS85 benchmarks used.
  - Simulations performed with BPTM 100nm technology and V_{dd}=1.0V.
- Synthesis performed using SIS.
  - Library of 26 gates (10 NOT gates, 5 NAND2 gates, 5 NOR2 gates, 3 NAND3 gates and 3 NOR3 gates) of different sizes.
- Each benchmark placed in a different WID zone
  - Can be independently compensated.
- Bias range (-0.5 to 0.5V) for v_{bn} and v_{bp}.
  - v_{step} = 0.1V

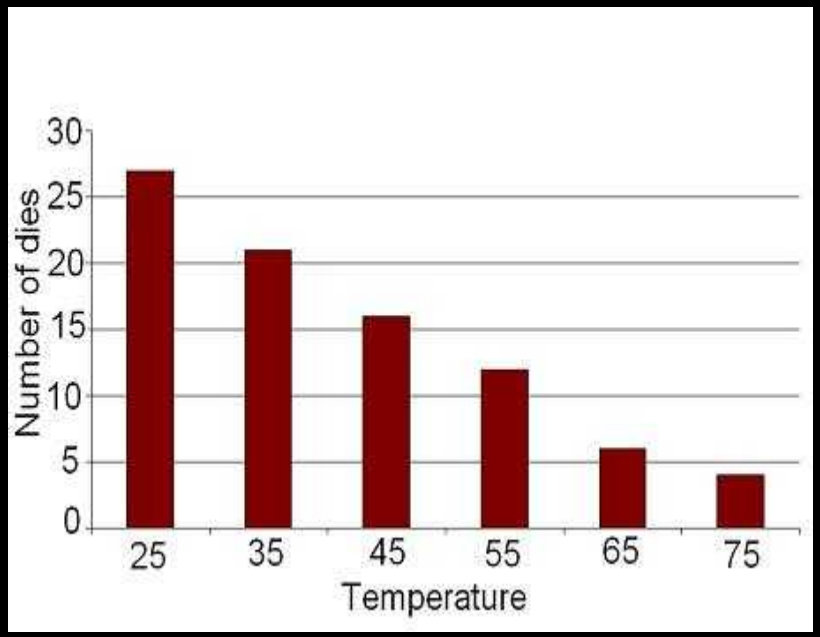
Test structure showing each WID variational zone.

Results of TABB

Bench mark	T (C)	D* (ns)	No ABB		Enum TABB		Math TABB		Run time Ratio (t_{Math}/t_{Enum})
			Dly (ns)	Lkg (uW)	v_{bn} (V)	v_{bp} (V)	v_{bn} (V)	v_{bp} (V)	
C432	50	0.902	0.941	4.78	0.2	0.2	0.13	0.13	0.51
C432	75		0.986	11.2	0.4	0.4	0.36	0.42	1.63
C880	50	0.763	0.801	2.90	0.2	0.3	0.16	0.24	0.52
C880	75		0.838	6.85	0.5	0.5	0.49	0.44	3.11
C1355	50	0.83	0.841	5.06	0.2	0.3	0.17	0.24	0.55
C1355	75		0.879	11.9	0.5	0.5	0.5	0.5	3.10
C3540	50	1.33	1.39	16	0.2	0.1	0.19	0.08	0.41
C3540	75		1.45	37.5	0.3	0.4	0.37	0.32	0.89
C5315	50	1.20	1.25	14.9	0.2	0.2	0.19	0.19	0.42
C5315	75		1.30	35	0.3	0.5	0.40	0.38	1.17
C6288	50	3.64	3.82	24.7	0.2	0.2	0.17	0.19	0.47
C6288	75		3.99	57.7	0.4	0.5	0.37	0.46	1.75

Process Compensation

- PABB actually performed using post-silicon tuning.
  - Simulations provide an overview of the utility of our method.
- Test structure (critical path replica) is a RO simulated using 100nm BPTM.
  - RO used to determine Go-No Go for each WID.
- Monte Carlo simulations (50) done using Gaussian distributions for v_{tn0} and v_{tp0}.



Simulations show that the yield is ≈ 50% at room temperature and decreases gradually with increase in T.

Process Compensation

- For each WID region, for each die, calculate the voltages (v_{bn},v_{bp}) by solving the NLPP.
- For simulation purposes, we assume that all WID regions have the same v_{tn0} and v_{tp0} distribution.
  - One set of simulations on the RO can be extended to all ISCAS benchmarks.

	NMOS-RBB PMOS-RBB	NMOS-RBB PMOS-FBB	NMOS-FBB PMOS-RBB	NMOS-FBB PMOS-FBB
No of dies	6	42	0	2

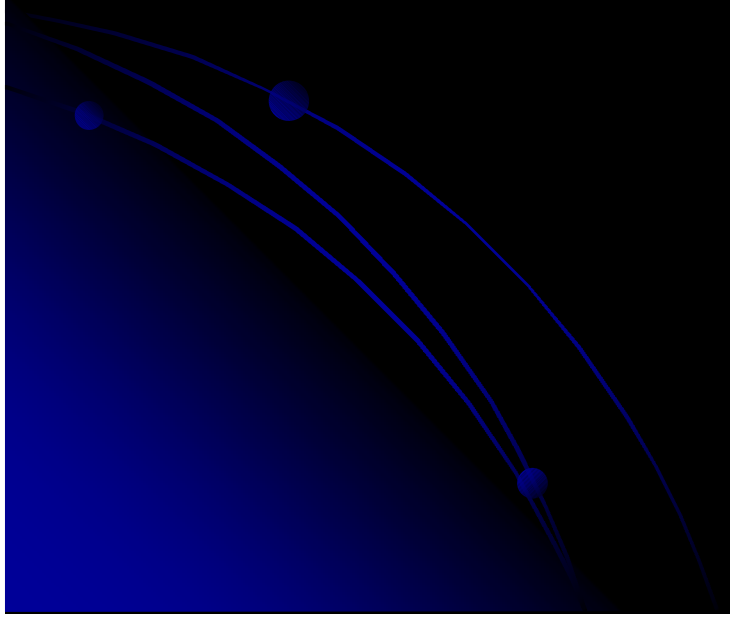
PTABB Compensation

	Temp	%Yield	Accepted Dies (out of 50)	P-FBB N-RBB	P-RBB N-RBB	P-FBB N-FBB
C432	50	100	50	35	0	15
C432	75	76	38	0	0	38
C880	50	100	50	24	0	26
C880	75	54	27	0	0	27
C1355	50	100	50	24	0	26
C1355	75	48	24	0	0	24
C3540	50	100	50	0	4	46
C3540	75	92	46	0	0	46
C5315	50	100	50	29	0	21
C5315	75	76	38	0	0	38
C6288	50	100	50	27	0	23
C6288	75	78	39	0	0	39

Conclusion

- Bidirectional Adaptive Body Bias can be used to improve the yield of dies for reasonable ranges of operating temperatures.
- New scheme to determine the exact values of body bias, PTABB compensation developed.
- One-time compensation for process variations and run-time compensation for temperature variations performed.

Backup



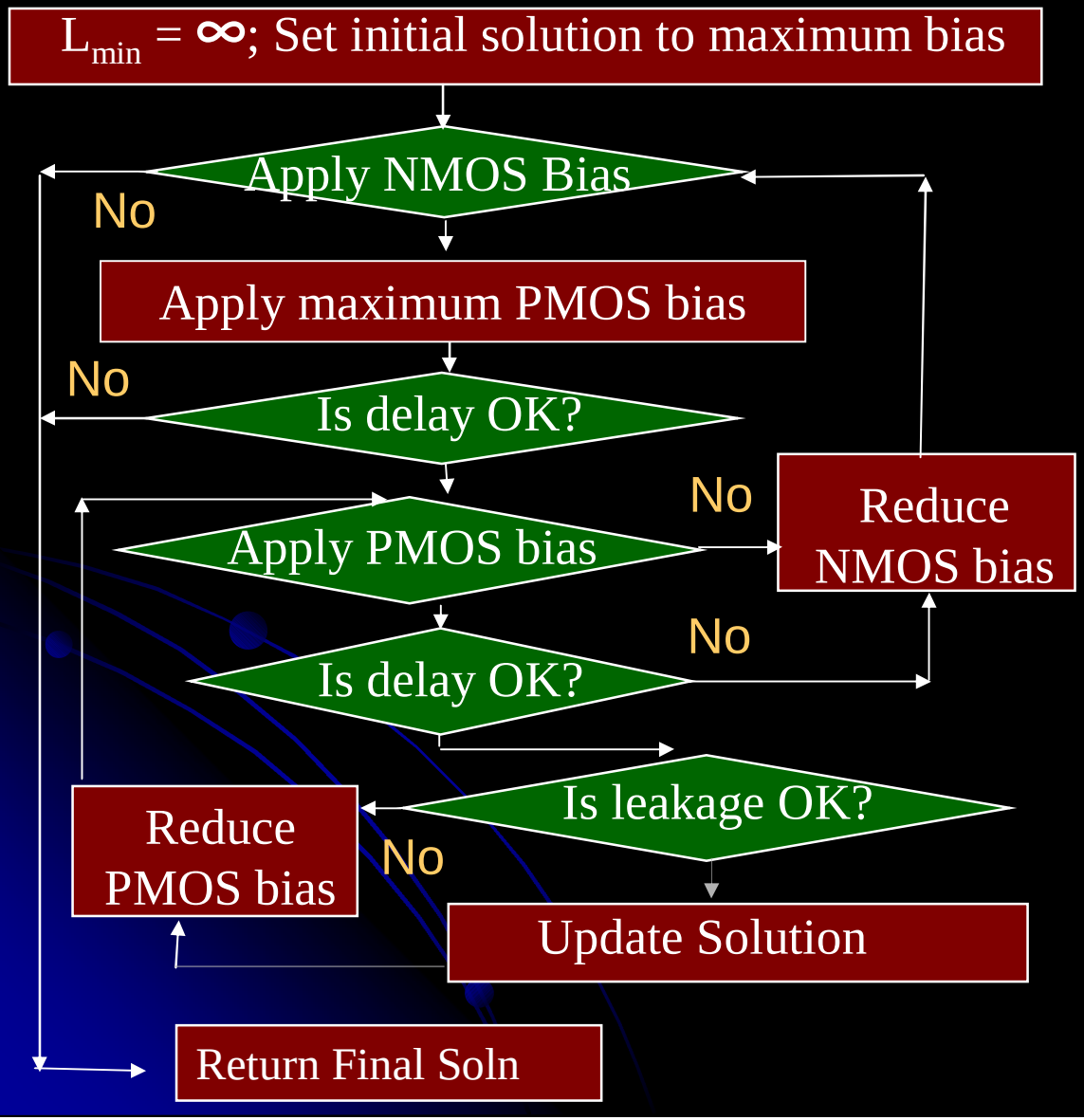
Independence of Variations

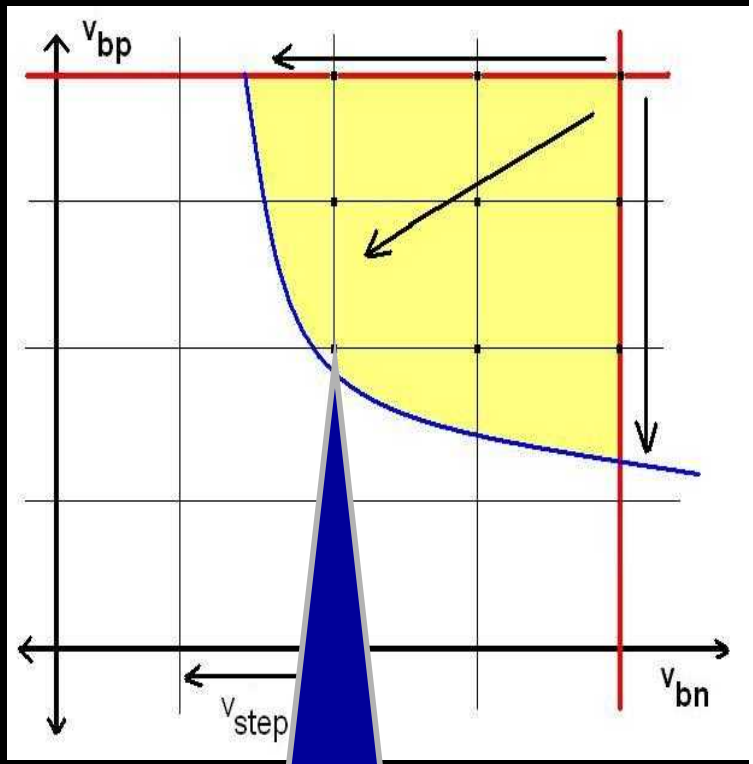
- Delay of a combinational circuit in the presence of temperature and process variations: $D=f(x, T)$
  - x is the vector of process variables
  - T is the operating temperature.
- x_0 and T_0 are the nominal values : $f(x_0,T_0)=D^*$.
- At any other point (x_1,T_1) ΔD can be written as $\Delta D = f(x_1,T_1) - f(x_0,T_0)$
- If x and T are independent variables,

$$\Delta D = \frac{\partial f}{\partial x}\left(T = T_0\right).\Delta x + \frac{\partial f}{\partial T}\left(x = x_0\right).\Delta T$$

$$\Delta D \approx \left[f(x_1,T_0) - f(x_0,T_0)\right] + \left[f(x_0,T_1) - f(x_0,T_0)\right]$$

Bounded Enumeration based TABB





PTABB Computations

$$(v_{bn},v_{bp})PTABB = (v_{bn},v_{bp})PABB + (v_{bn},v_{bp})TABB$$

T=25º	v_{bn}	v_{bp}

T=50º	v_{bn}	v_{bp}

T=75º	v_{bn}	v_{bp}

\+ $(v_{bn},v_{bp})PABB$ →

Temp	v_{bn}	v_{bp}
25		
50		
75		

TABB values for each circuit block determined through simulations.

PABB values for each circuit block determined through post-silicon tuning.

PTABB values programmed into the ROM for each WID variational region.

Results of Simulation on RO

Simulation using BPTM 100nm model files

RO delay with nominal temperature and process conditions = 151ps

Temp	Process Corner	DelayPT $f(x_1,T_1)$	DelayP $f(x_1,T_0)$	DelayT $f(x_0,T_1)$	ΔDelayPT	ΔDelayP + ΔDelayT	Diff
50	Low V_t	145.6	141.8	154.9	-5.4	-5.3	-0.1
50	Low V_t	165.3	161.2	154.9	14.3	14.2	0.1
75	High V_t	149.2	141.8	158.6	-1.8	-1.5	-0.3
75	High V_t	169.3	161.2	158.6	18.3	17.8	0.5