Analysis and Optimization of Gate Leakage Current of Power Gating Circuits

Hyung-Ock Kim and Youngsoo Shin

Dept. of EE, KAIST

Korea

KAIST

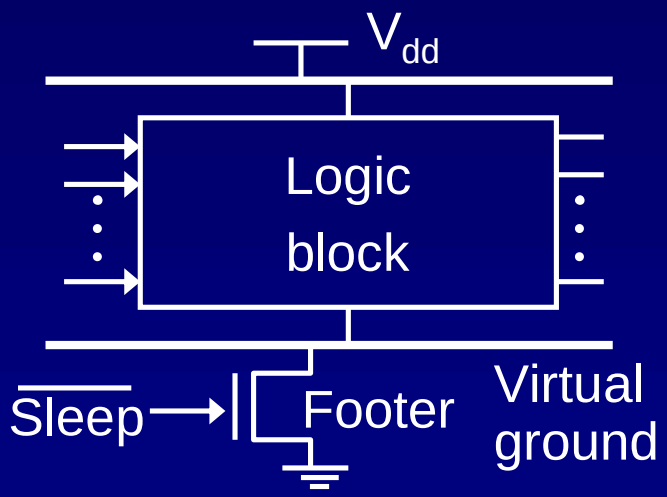
VLSI Design Technology Lab.

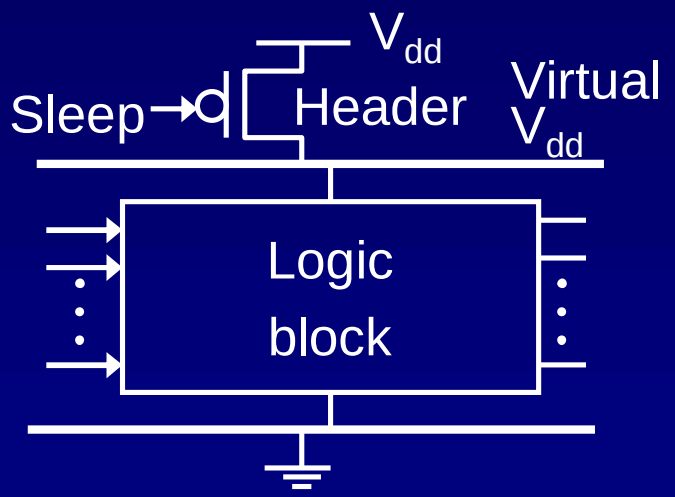
Outline

- Introduction
- Current switch design
  - Gate leakage current of power gating circuits
  - Current switch design of power gating circuits
- Power optimization through input control
- Experiments
- Summary

Introduction

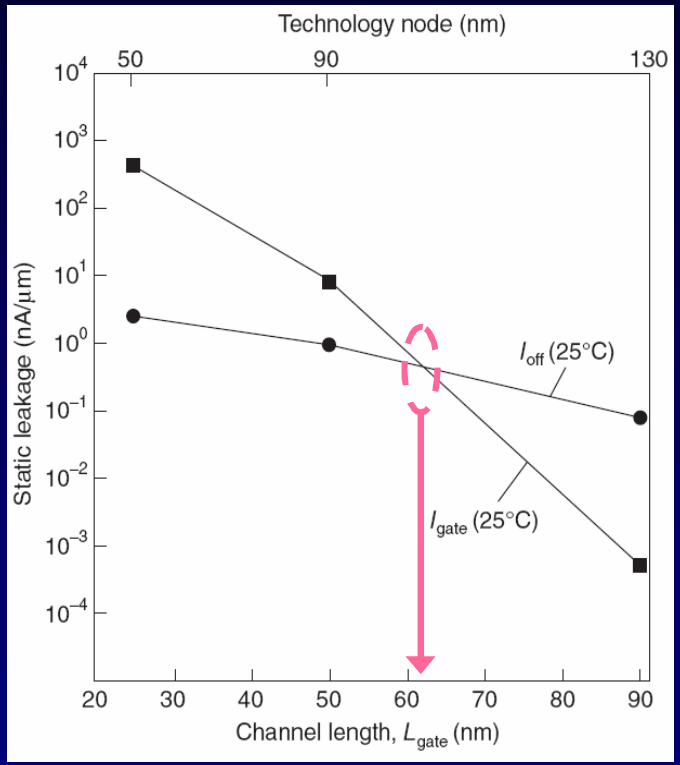
- Power gating circuits
  - Efficient to reducing subthreshold leakage current
  - Current switch made of
    - Low V_t or high V_t
    - Footer and/or header
  - PMU turns on or off the current switch





Introduction

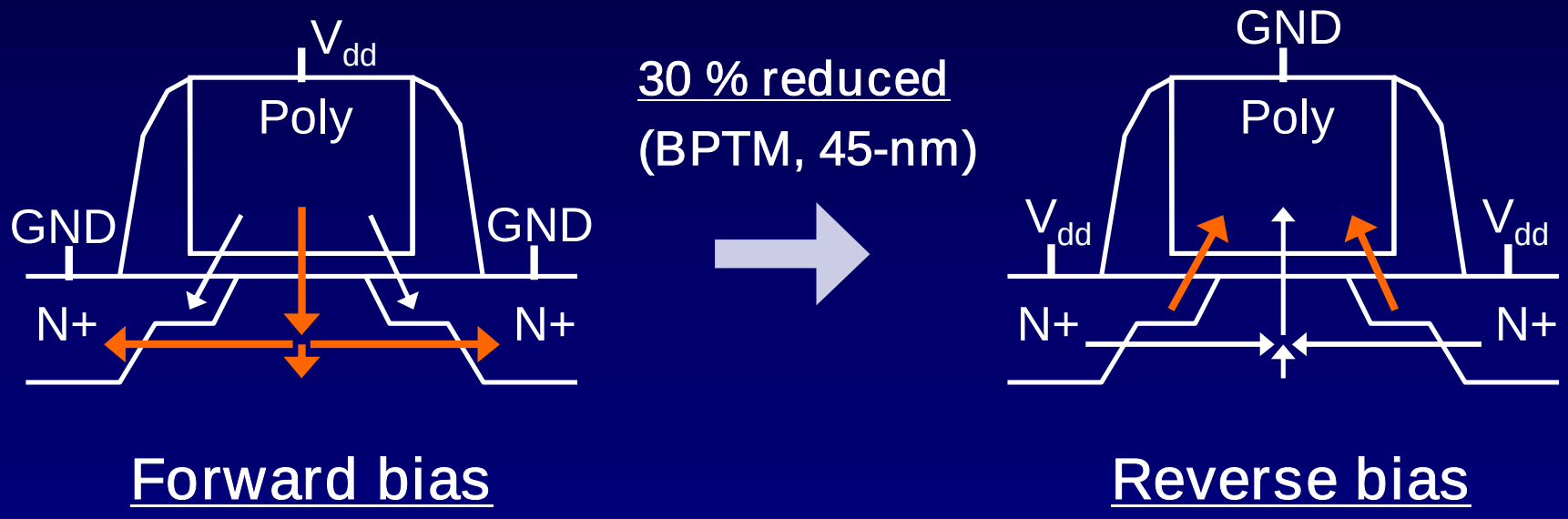
- Gate leakage current (I_g)
  - Power gating circuits suffer from I_g in nano-scaled devices
  - 500 x per technology generation (ITRS 2001)
  - One order smaller I_g in pMOSFET than in nMOSFET (hole vs. electron)



N. Shirisantana et al, IEEE D&T 2004

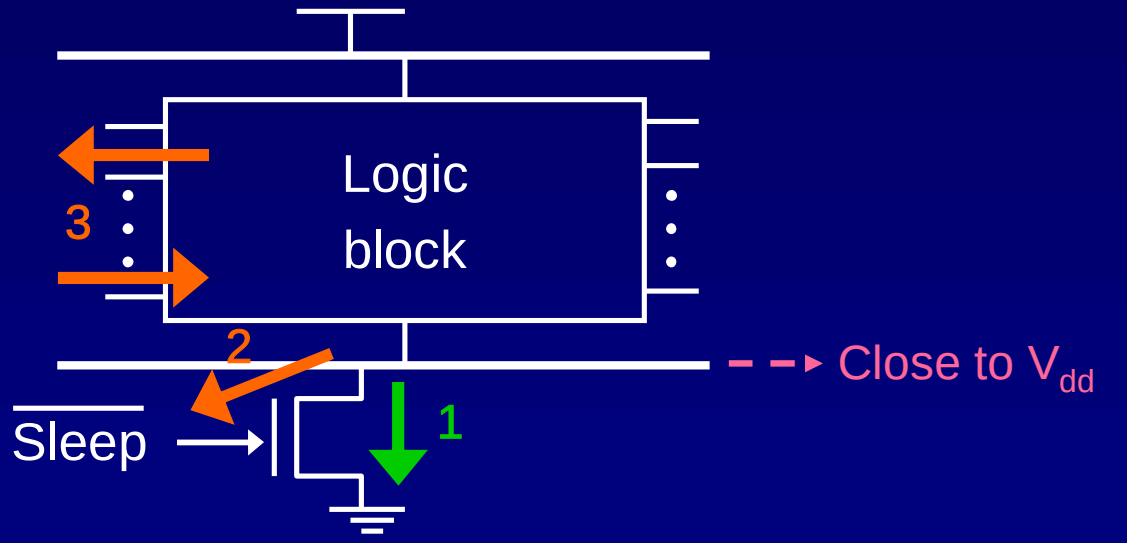
Introduction

- Gate leakage current (I_g)
  - Gate-to-channel tunneling current
  - Edge-direct tunneling current



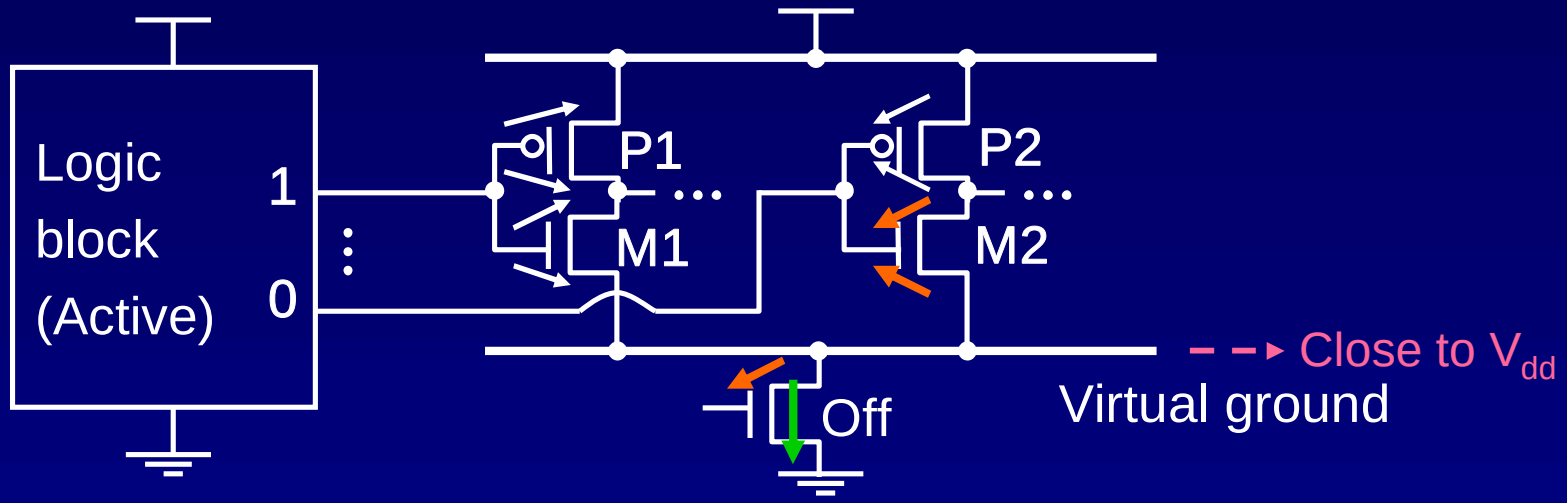
Leakage of Power Gating Circuits

- Sources of leakage current in power gating circuits when sleep
  1. Subthreshold leakage current of current switch
  2. Gate leakage current of current switch
  3. Gate leakage current at input (input dependent)



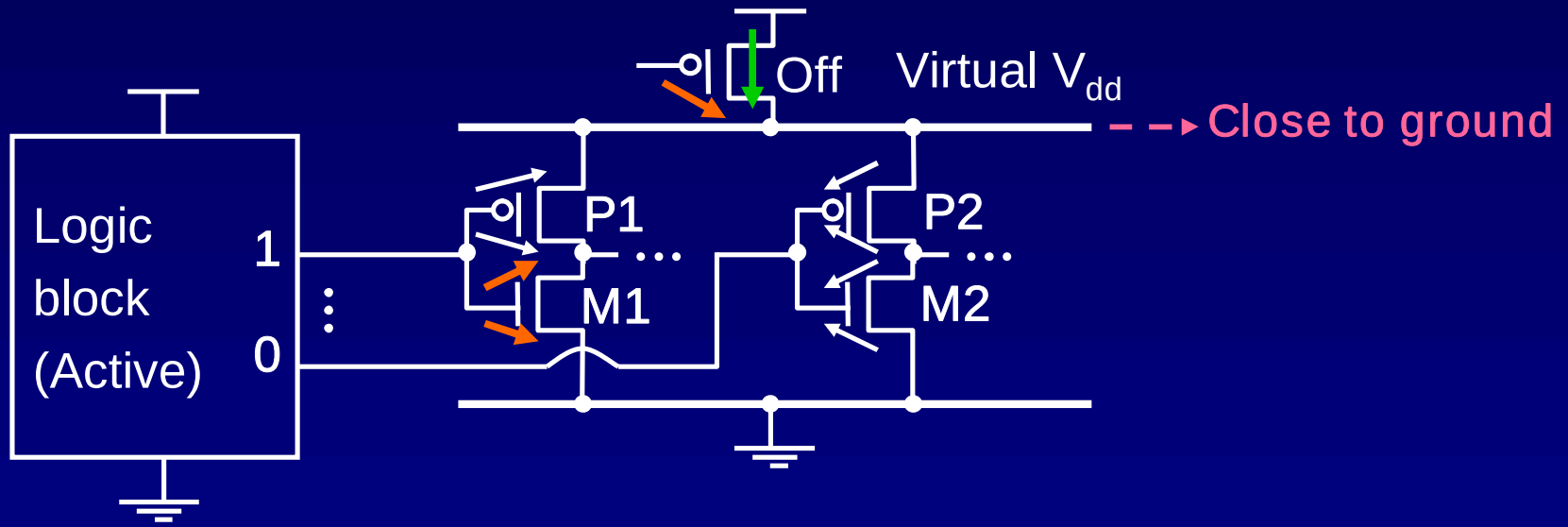
Leakage of Power Gating Circuits

- Mechanism of gate leakage current in footer
  - P1: forward, pMOSFET P2: reverse, pMOSFET
  - M1: forward, nMOSFET M2: reverse, nMOSFET
  - M2 + footer: main component



Leakage of Power Gating Circuits

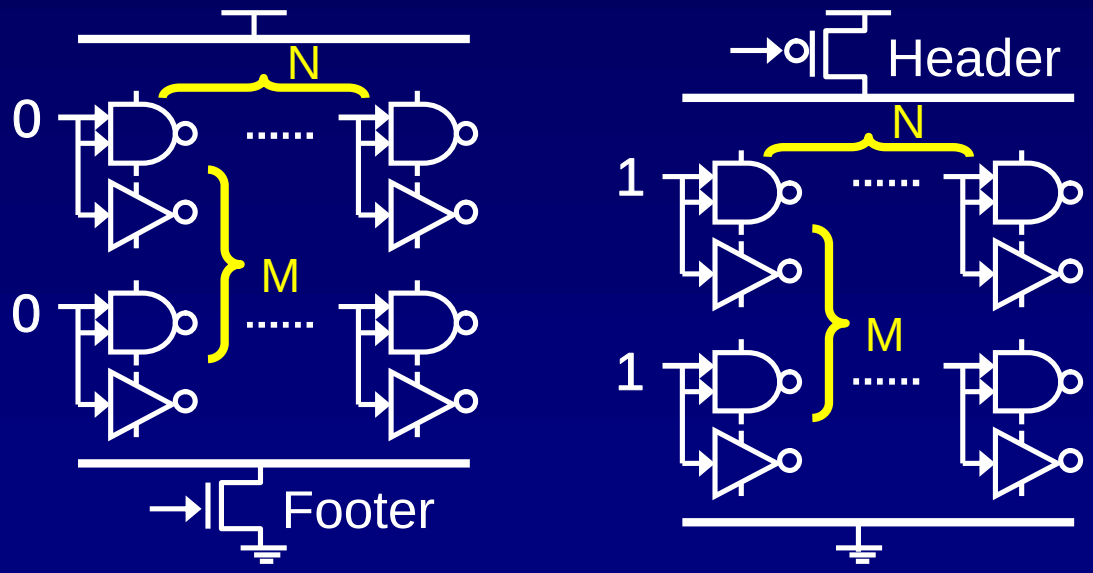
- Mechanism of gate leakage current in header
  - P1: forward, pMOSFET P2: reverse, pMOSFET
  - M1: forward, nMOSFET M2: reverse, nMOSFET
  - M1 + header: main component



Input Gate Leakage

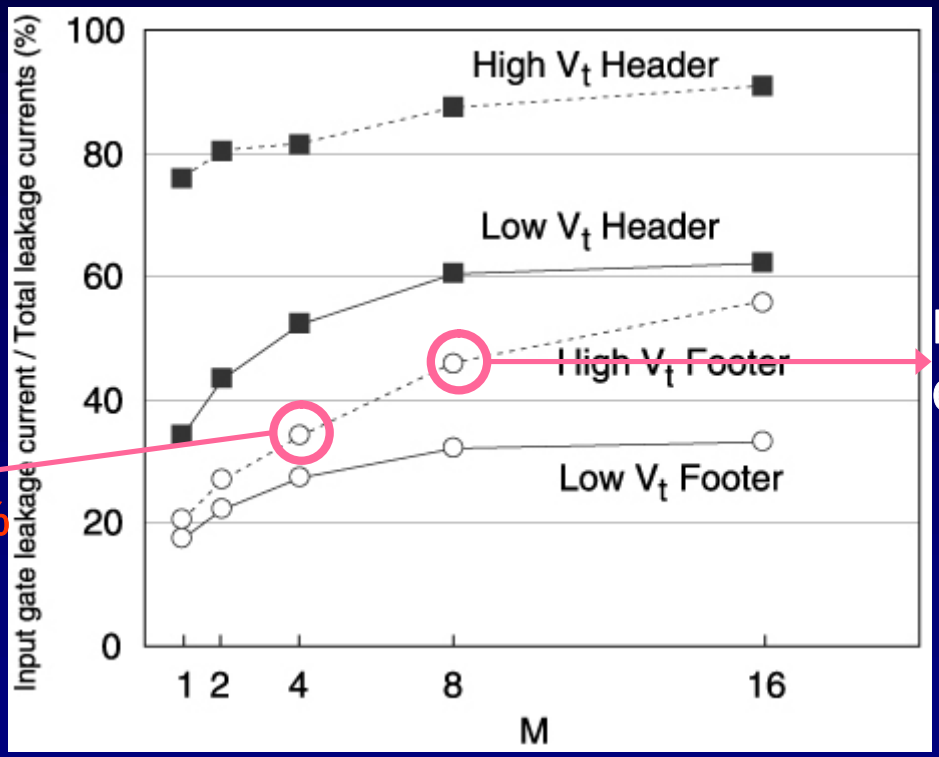
- Impact of input gate leakage
  - M: # inputs, N: # stages (M x N = 48)
  - Current switch sizing: 3 % delay penalty
  - 45-nm technology

Simulation circuit: inv-nand chains



Input Gate Leakage

- Impact of input gate leakage
  - Significant, especially with large # inputs & high V_t

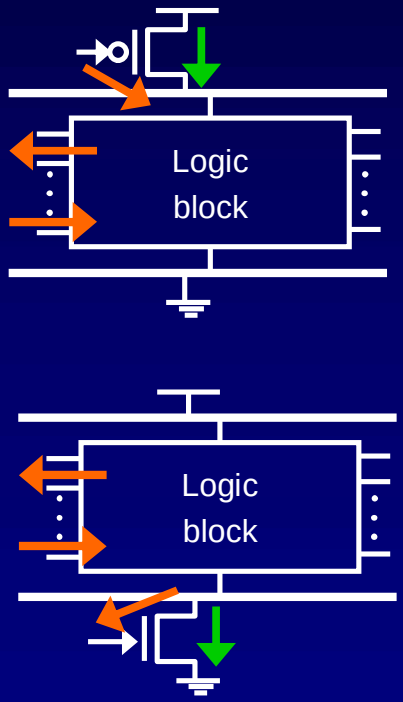


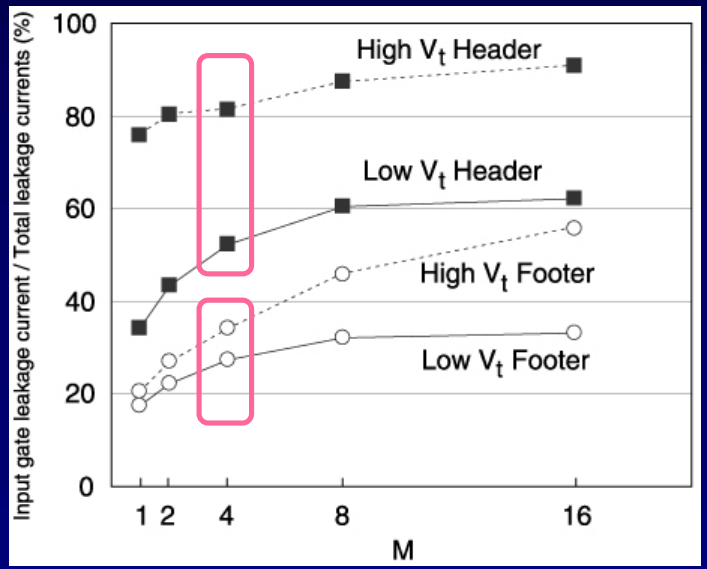
Input TR.: 8.3 %
Gate leakage: 34 %

Input TR.: 16.6 %
Gate leakage: 45 %

Input Gate Leakage

- Impact of input gate leakage
  - Header vs. footer

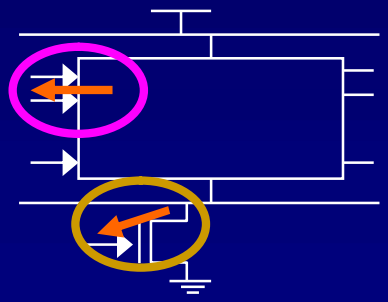


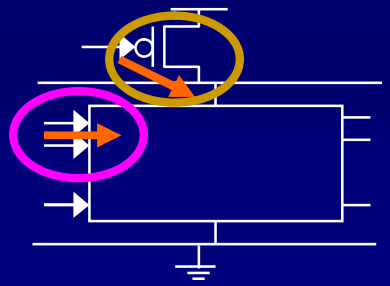


Current Switch Design

- Decision of footer or header

	Footer	Better?	Header
Input gate leakage	Reverse bias	>	Forward bias
Gate leakage of current switch	nMOSFET	<	pMOSFET

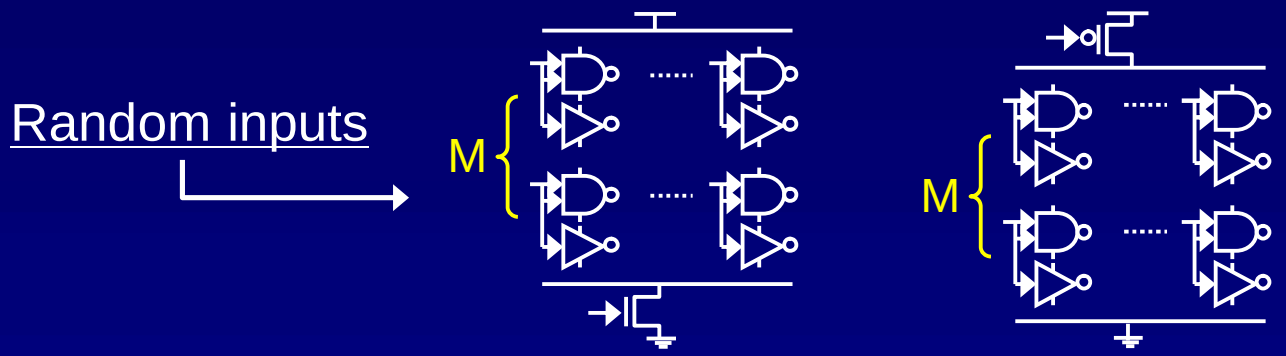




Current Switch Design

- Design of power optimal current switch

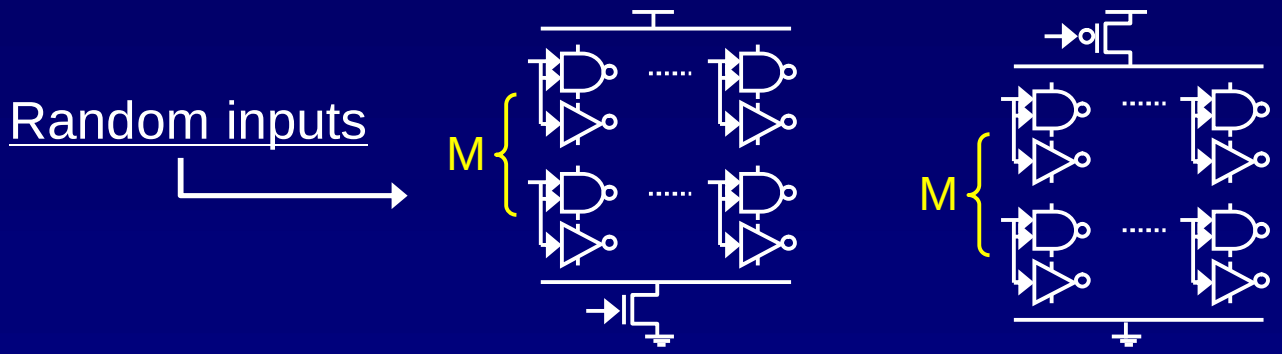
Tech. (nm)	Delay Penalty	M			
		2	4	8	16
45	3 %	Header	Header	Footer	Footer
	6 %	Header	Header	Footer	Footer



Current Switch Design

- Design of power optimal current switch

Tech. (nm)	Delay Penalty	M			
		2	4	8	16
65	3 %	Header	Header	Header	Footer
	6 %	Header	Header	Footer	Footer

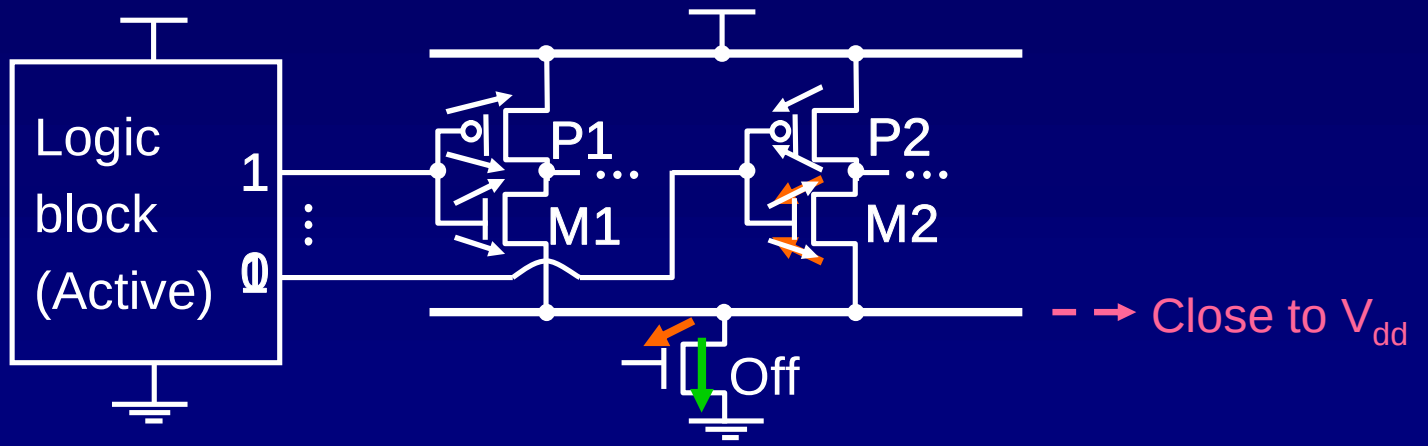


Current Switch Design

- Design of power optimal current switch
  - C5315: 9-bit ALU, ISCAS 85 benchmark
  - Input transistors: 9.2 %
  - Header is better when delay penalty is 3 %
  - Footer is better when delay penalty is 6 %
  - In low V_t current switch design, footer is always better due to subthreshold leakage current
    - Small current switch size in footer

Power Optimization through Input Control

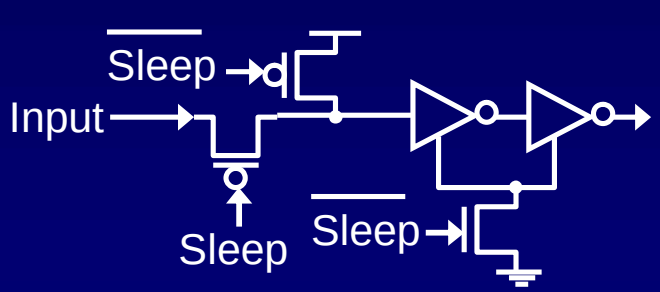
- Input gate leakage
  - Significant portion of total leakage
- Input gate leakage and input values
  - All input values 1 for footer
  - All input values 0 for header



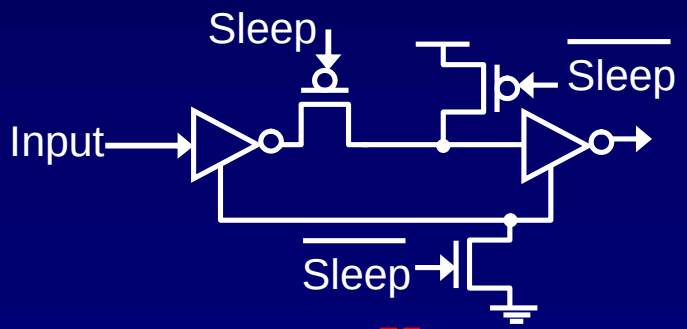
Power Optimization through Input Control

- Gate-leakage-efficient input control circuits
  - Functionally transparent in active
  - Clamping inputs to specific value in sleep

Input control circuits for footer



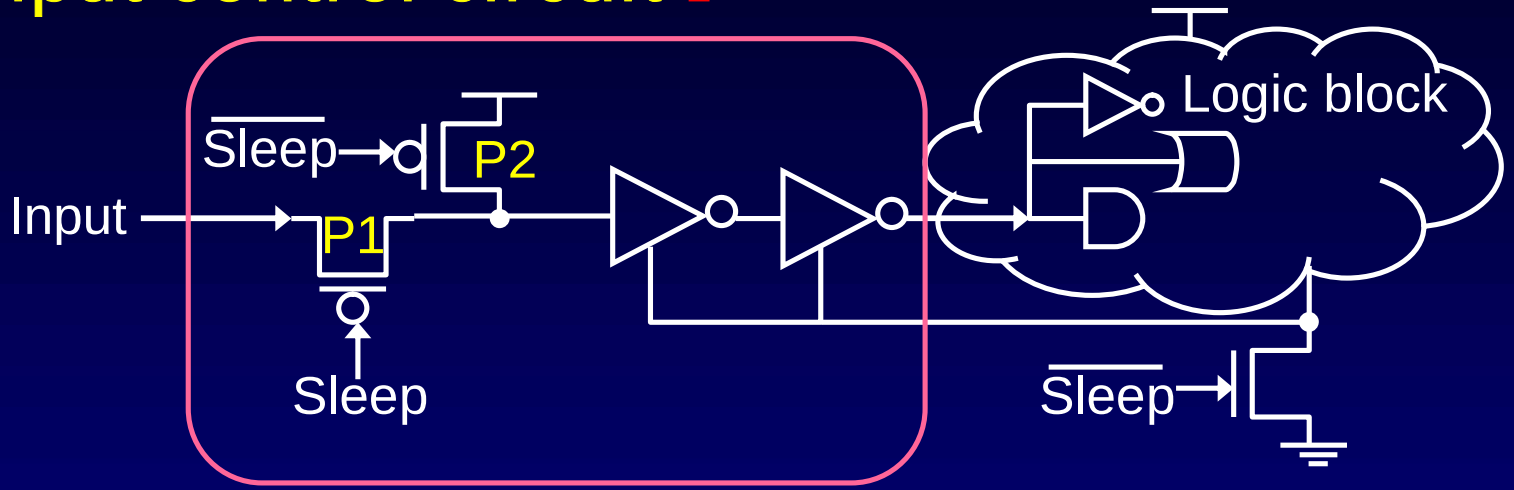
I



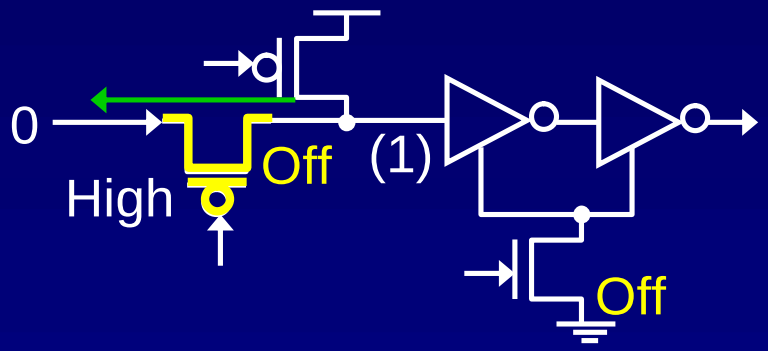
II

Power Optimization through Input Control

- Input control circuit I

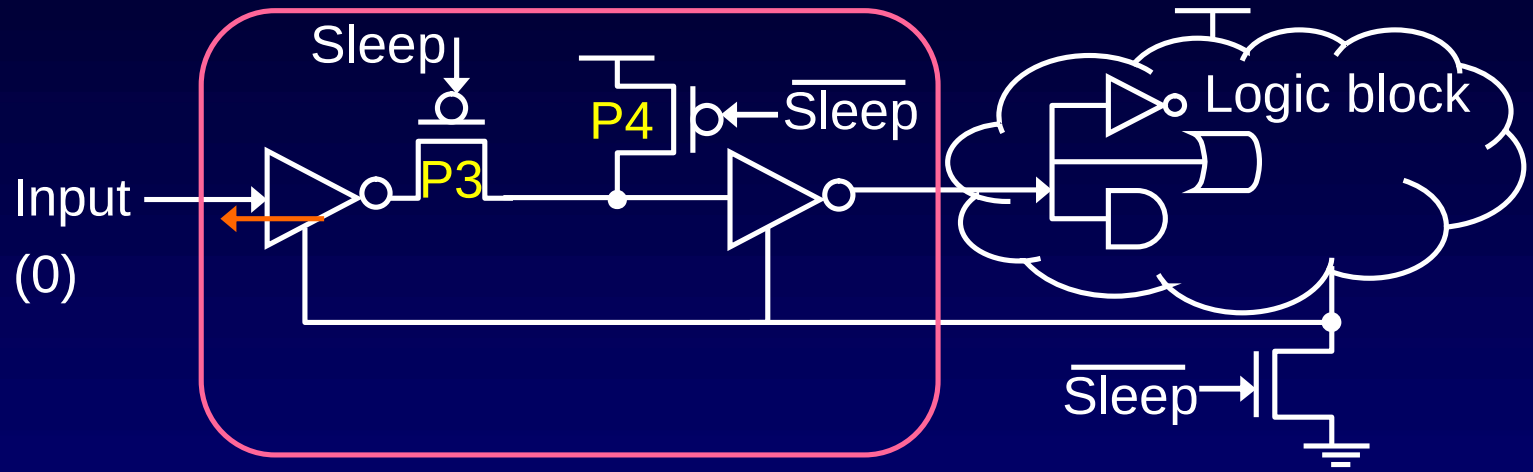


Reduce more
leakage current

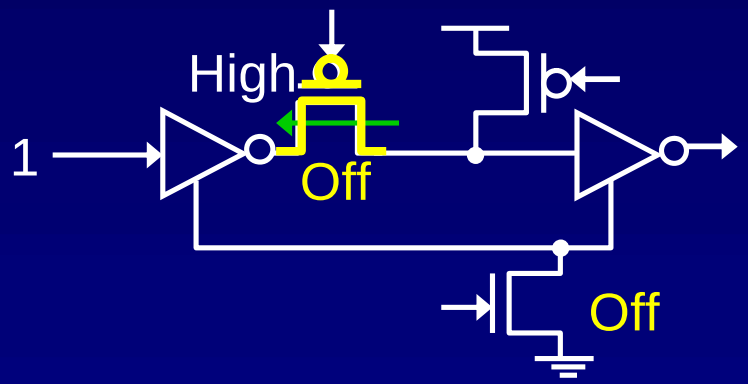


Power Optimization through Input Control

- Input control circuit II



Reduce more
leakage current

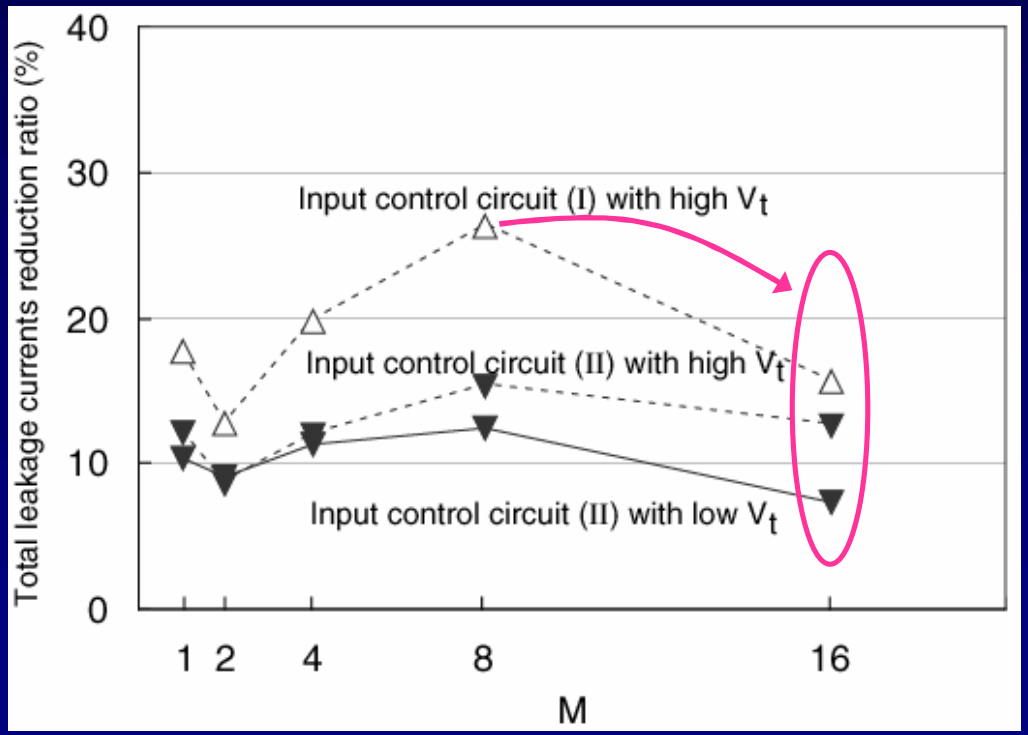


Power Optimization through Input Control

- Input control circuits
  - Optimize input gate leakage current

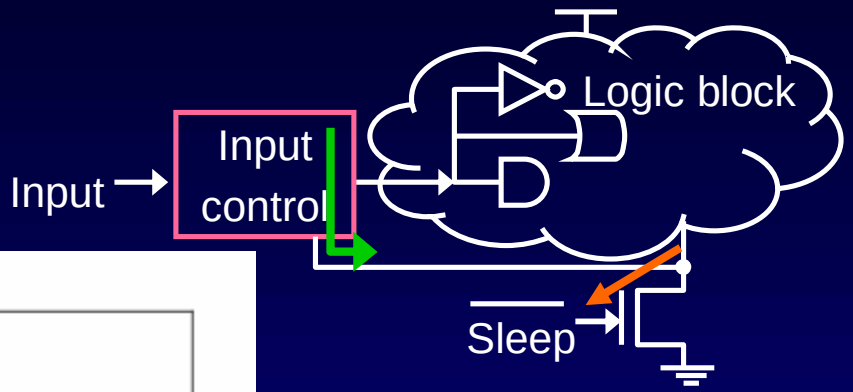
Low V_t: input control circuit II

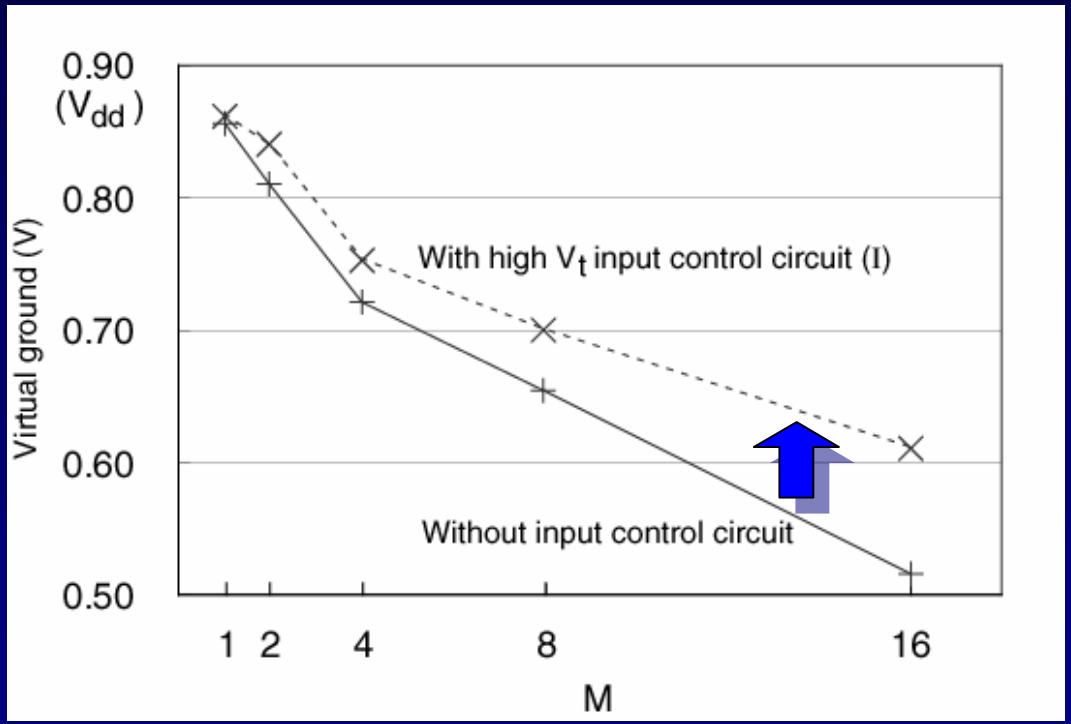
High and low V_t: input control circuit I



Power Optimization through Input Control

- Input control circuits





Power Optimization through Input Control

- Experiments

	Circuit II	Circuit I	Circuit II	Circuit I
	Low V_t footer	High V_t footer	Low V_t header	High V_t header
C1908	2.0 %	11.4 %	-3.3 %	35.3 %
C2670	4.7 %	22.6 %	-17.1 %	45.9 %
C3540	7.1 %	27.1 %	1.1 %	61.0 %
C5315	8.3 %	30.8 %	-5.7 %	52.0 %
C7552	2.1 %	11.9 %	-8.3 %	33.5 %
64-b CLA	-10.2 %	1.6 %	-7.8 %	43.7 %
avg.	2.8 %	19.1 %	-7.4 %	47.0 %

Summary

- Power gating circuits, efficient for subthreshold leakage, suffer from gate leakage
- Input gate leakage is important in the decision of footer vs. header
- Input gate leakage can be reduced by input control circuits