Delay Modeling and Static Timing Analysis for MTCMOS Circuits

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Outline

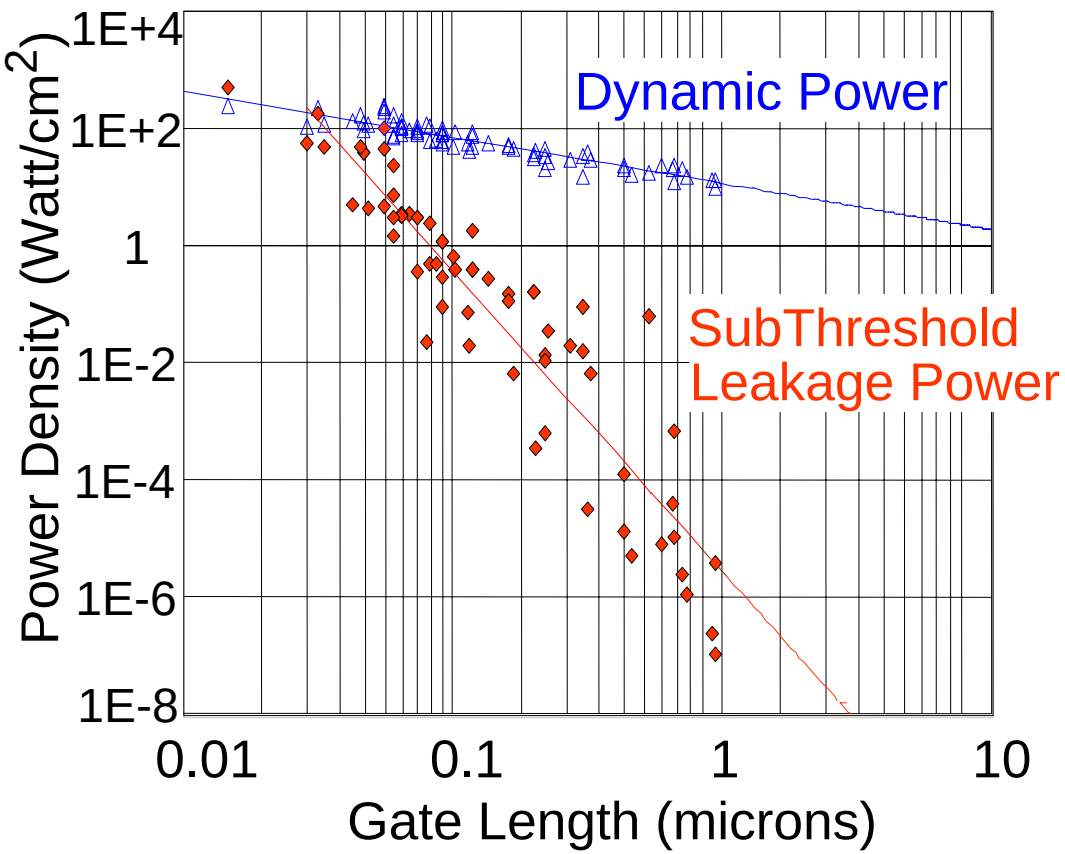
- Background
- Conventional Delay Modeling
- Technique We Proposed
- Application to the Static Timing Analysis
- Experimental Results
- Conclusions and Future Work

Background

- Low power design methodology maintaining high performance is required

  - Leakage power is significantly increasing with scaling

  - High performance is also needed in recent multimedia applications



Source: R. Puri, et al, DAC '05

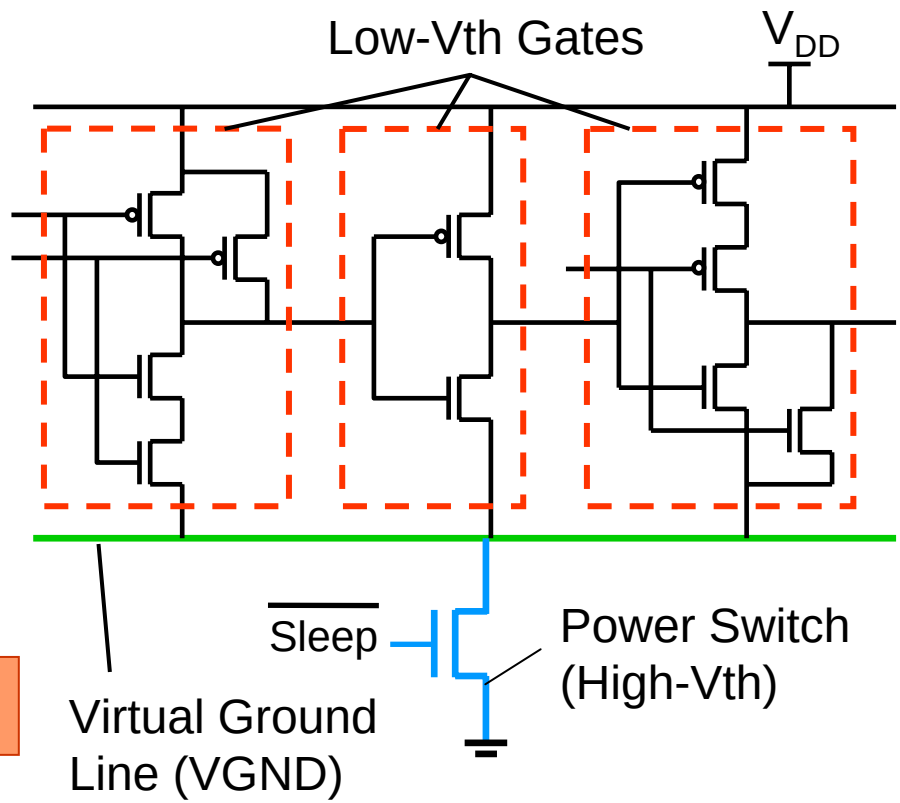
MTCMOS Circuits

MTCMOS (Multiple Threshold CMOS)

Use two types of transistors

Low-Vth transistor : High speed
High leakage

High-Vth transistor : Low speed
Low leakage



In active mode

High speed operation (Low-Vth)

In standby mode

Reduce leakage power (Power Switch : off)

Selective-MT Technique

- Applies MTCMOS technique only to the critical path

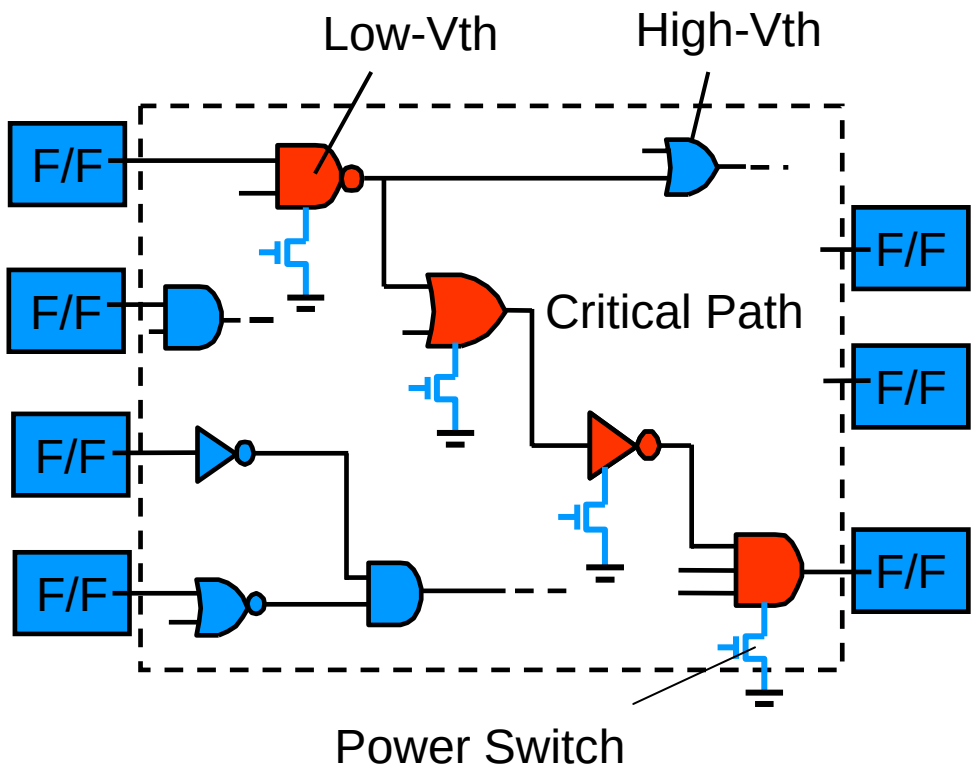
Critical Path

Using Low-Vth gates and connect the power switch individually

Maintain the Circuit Performance

Non-critical paths

Using High-Vth gates



Source: K. Usami, et al, ISLPED '02

Reduces both static and active leakage power

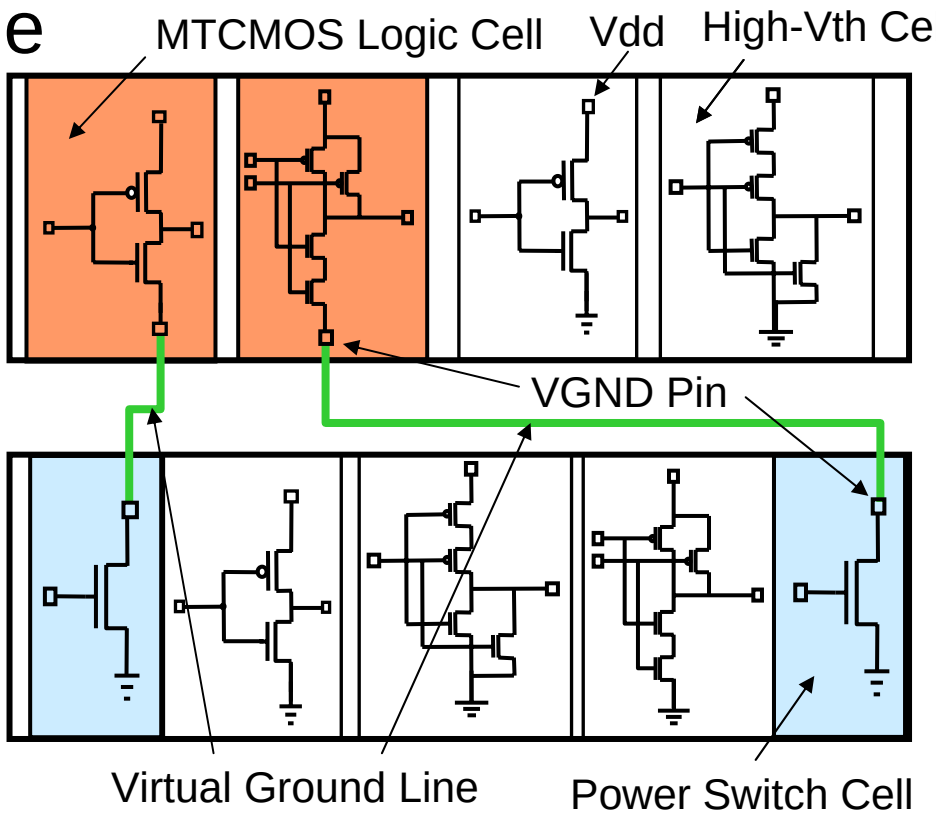
Physical Implementation Example of Cell-based Selective-MT

- Layout model we assume

MTCMOS Logic Cells (equip a VGND pin)

Connected by the VGND Line

Power-Switch Cell



Source: T. Kitahara, et al, DATE '05

- VGND length depends on where power switch is placed
- Modeling and analysis for VGND line are needed

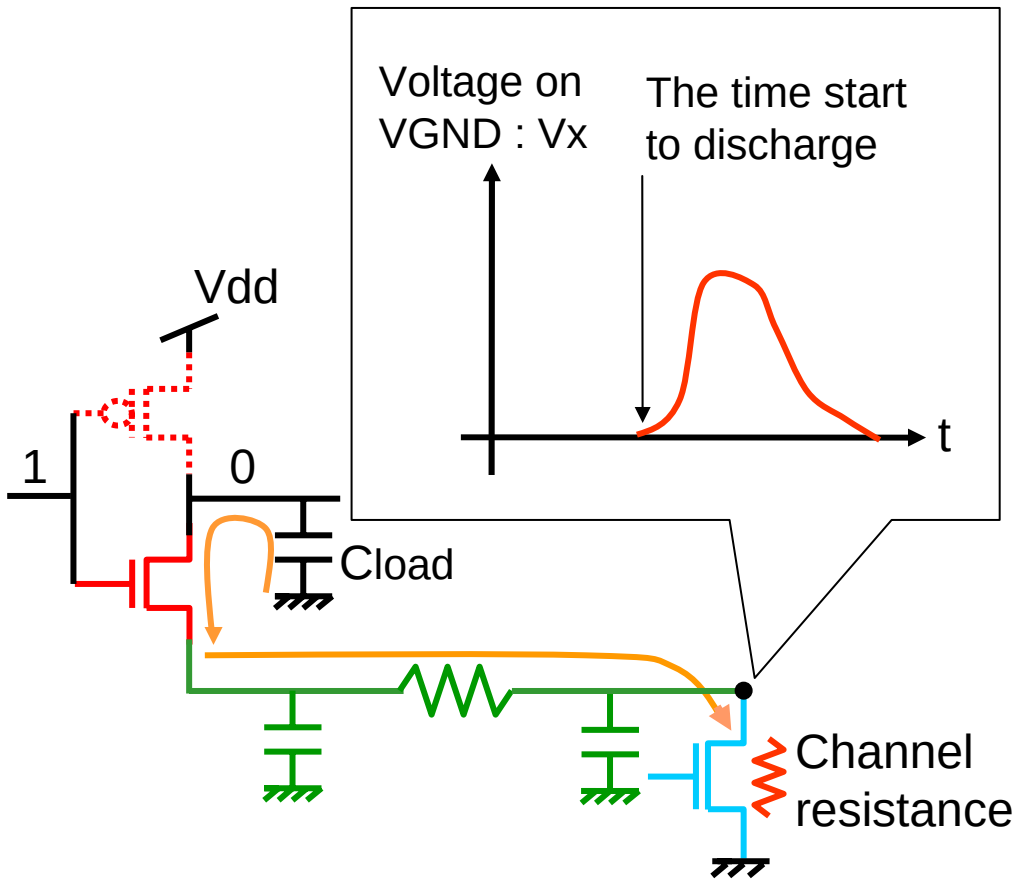
Problems in MTCMOS Circuits

- Delay increases due to a voltage fluctuation of VGND line

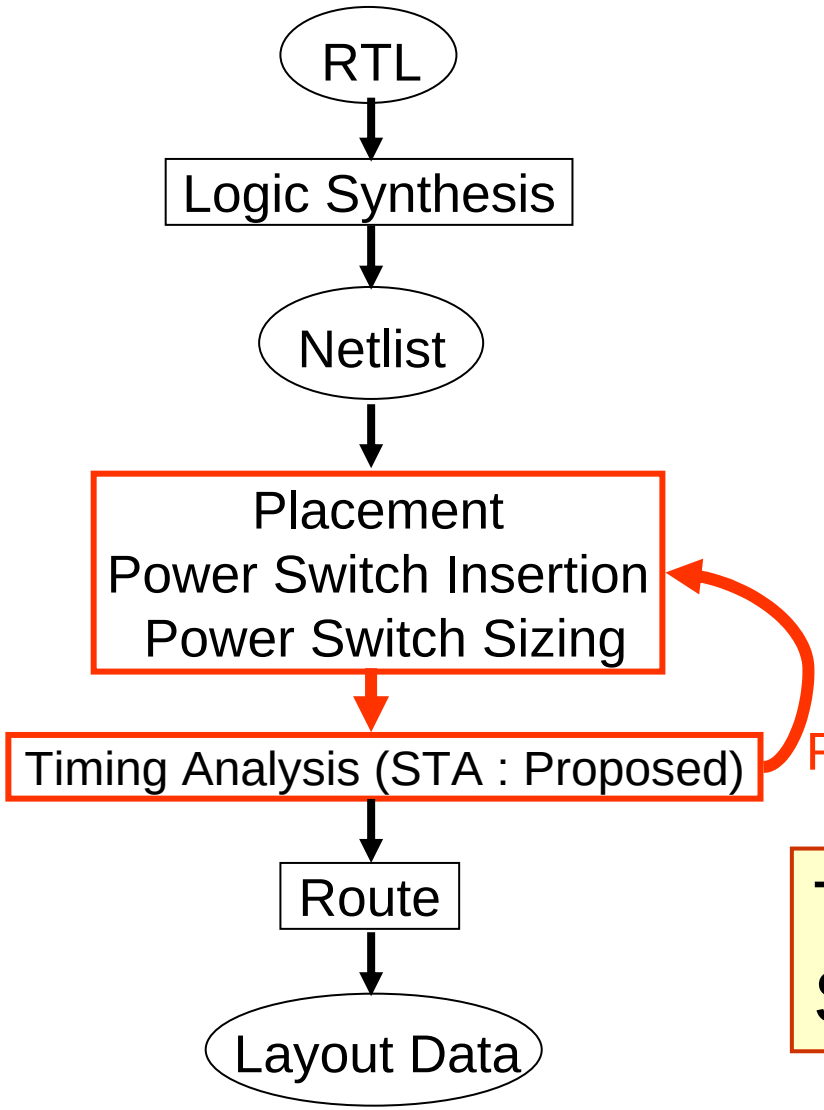
At the “fall” transition

Resistance and capacitance trigger the voltage fluctuation of VGND

Influence the circuit delay



MTCMOS Design Flow



Due to the power switch insertion, timing violation and area increase occur

To avoid this

Change the power-switch size and location

To optimize the design quickly, STA is required

Objectives of Our Study

- Develop a delay modeling for MTCMOS circuits
  - Analyze the impact of VGND length and power switch size
- Propose a static timing analysis methodology for MTCMOS circuits

Using TOSHIBA 90nm Technology for Analysis
(This research was supported by TOSHIBA Corp.)

Conventional Delay Modeling

Delay Modeling using Table-lookup model

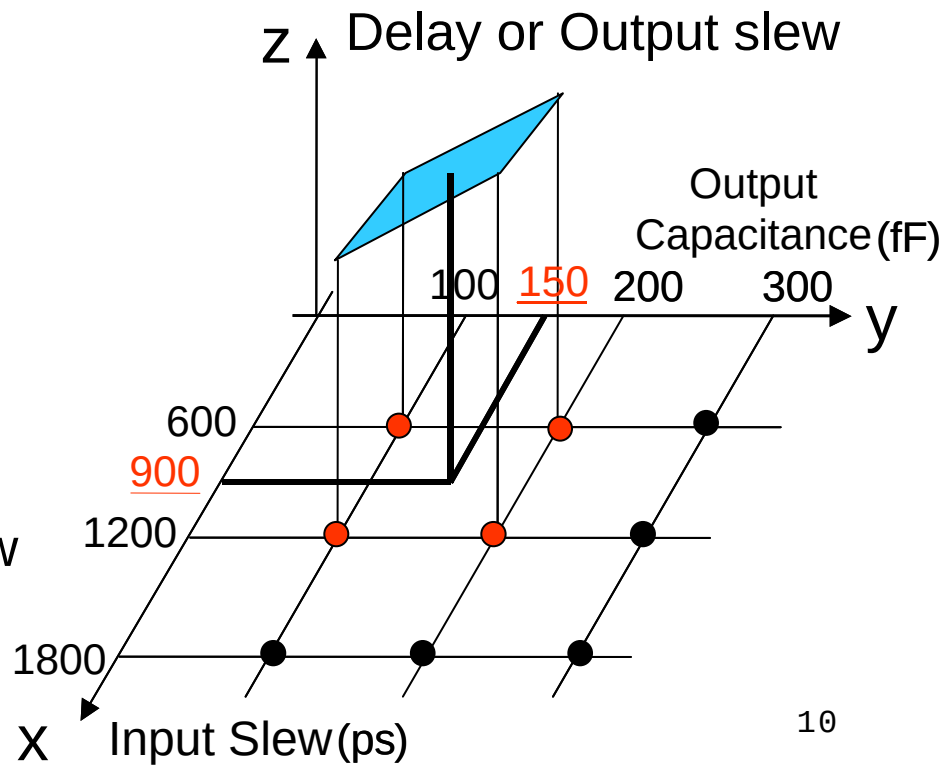
- Interpolate the delay and the output slew using LUT
- LUT consists of the input slew and the output capacitance

Interpolation Equation

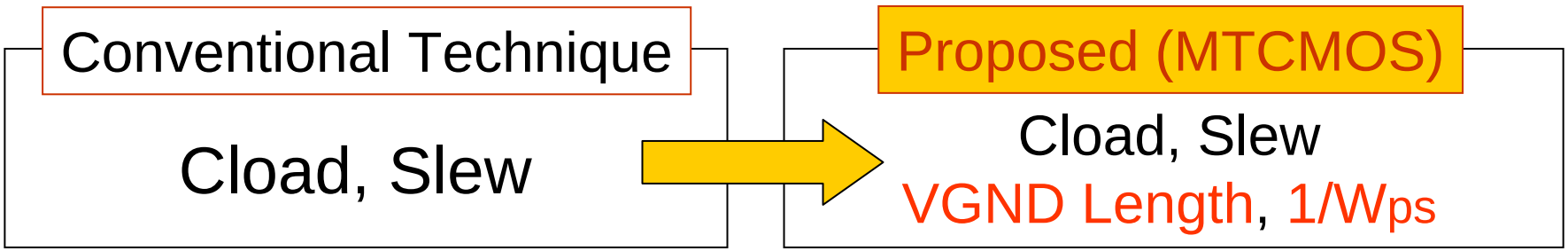
$Z = A + Bx + Cy + Dxy$

Solve coefficients A,B,C,D by using four nearest value

Compute the delay and the output slew by substituting given x, y values



Proposed Delay Modeling



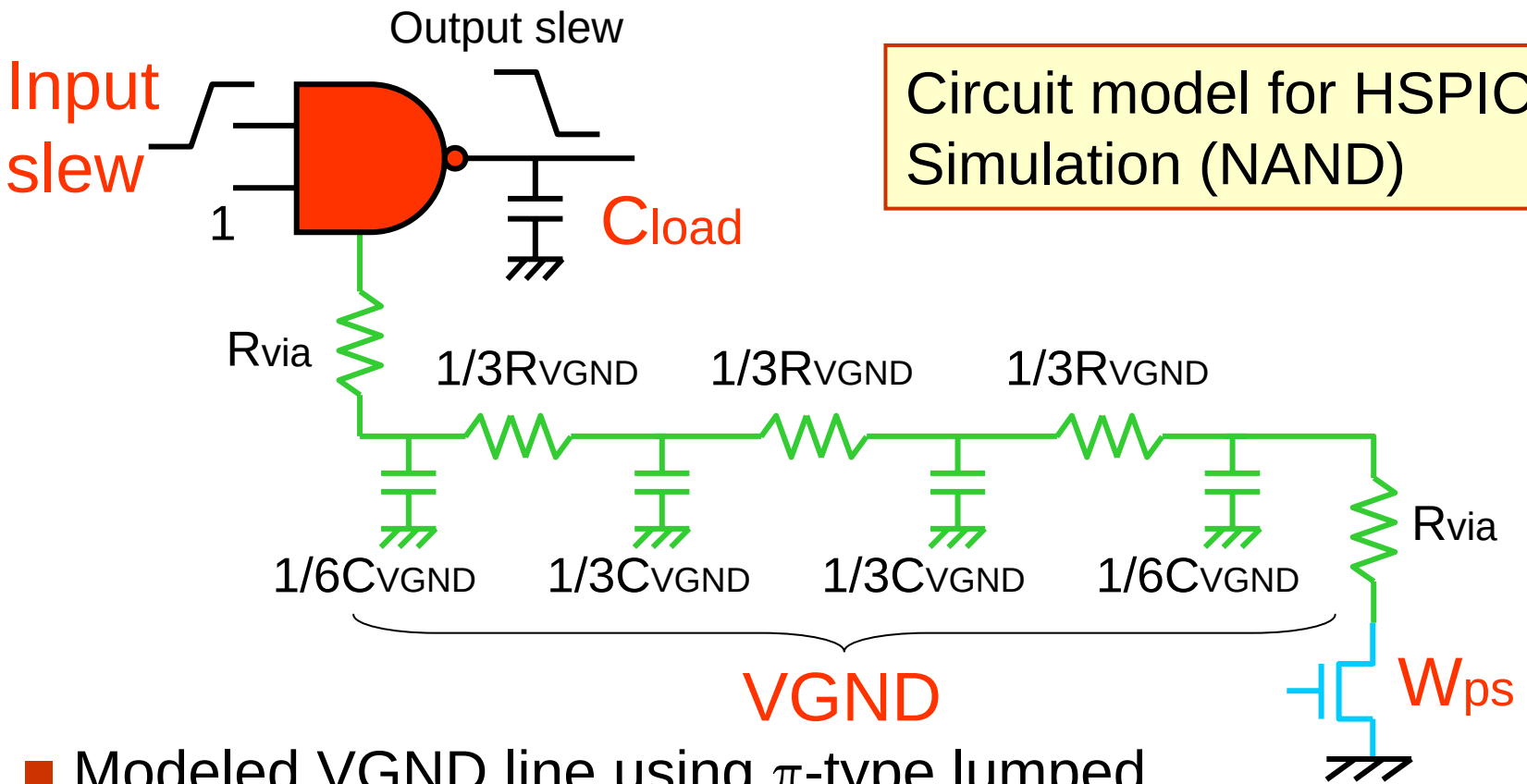
Extend to four coefficients

Extend the interpolation equation

$$Z = A + Bv + Cw + Dx + Ey + Fvw + Gvx + Hvy + Iwx + Jxy + Kxy + Lvwx + Mvwy + Nvxy + Owxy + Pvwxy \text{ (parameters : v,w,x,y)}$$

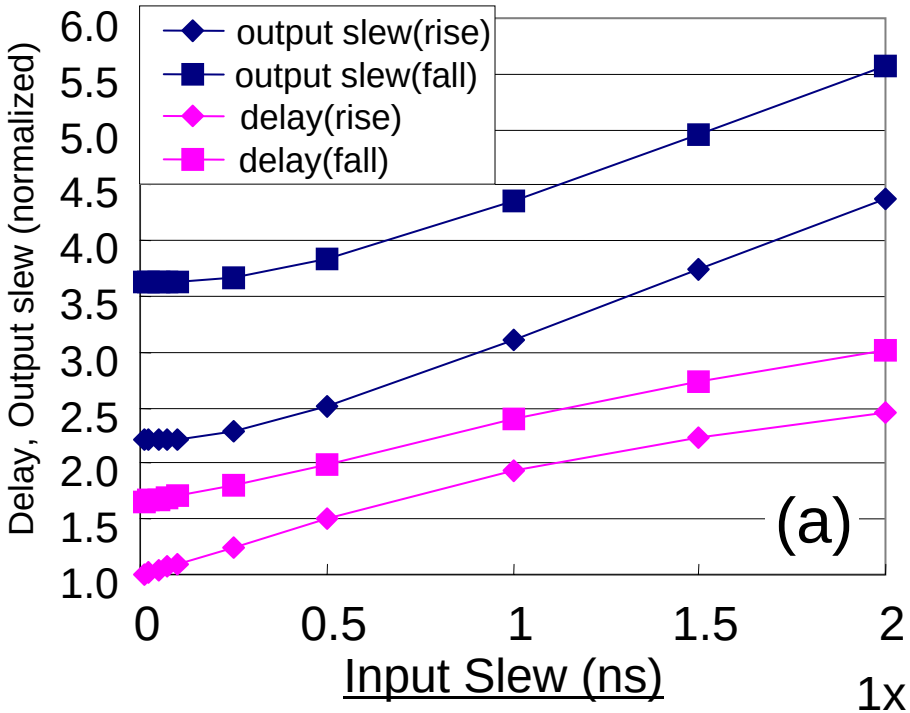
Solve the coefficients by applying the Gaussian elimination

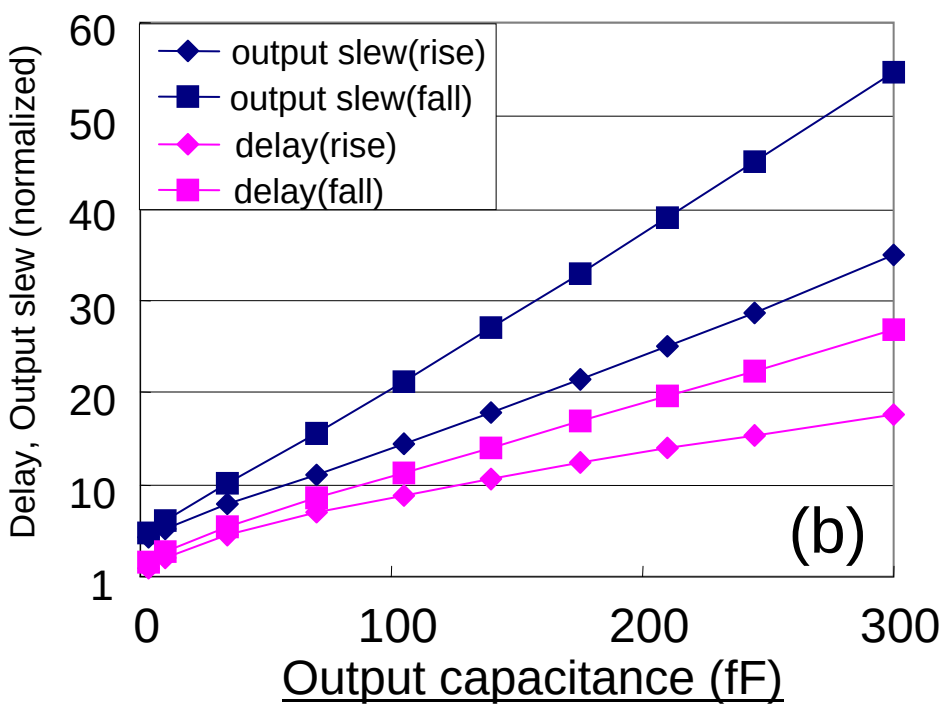
Analysis on the impact of parameters

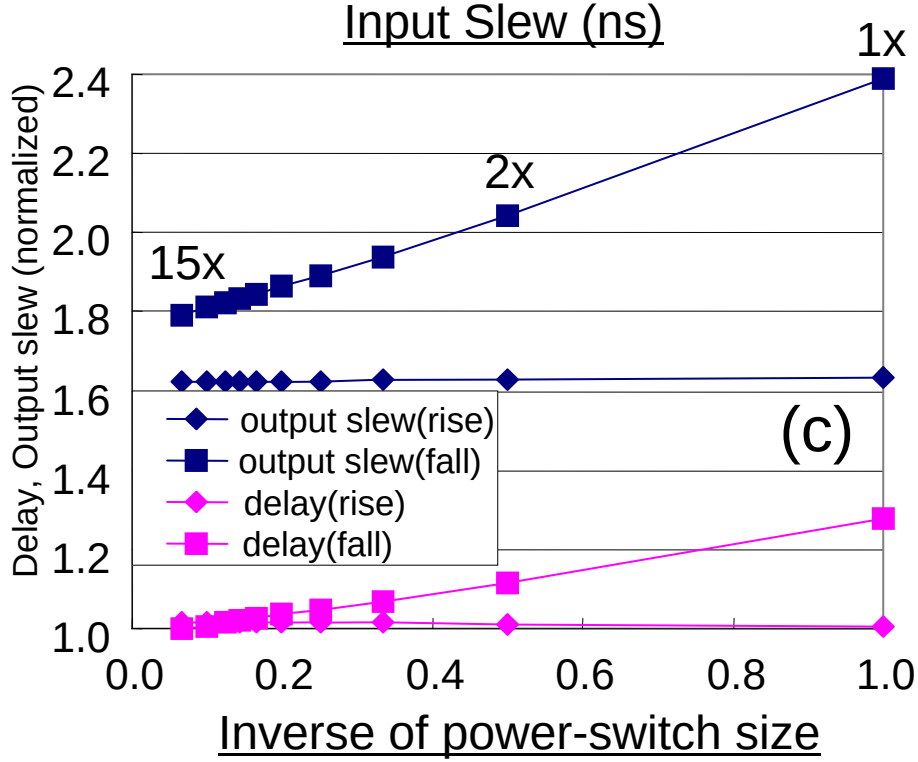


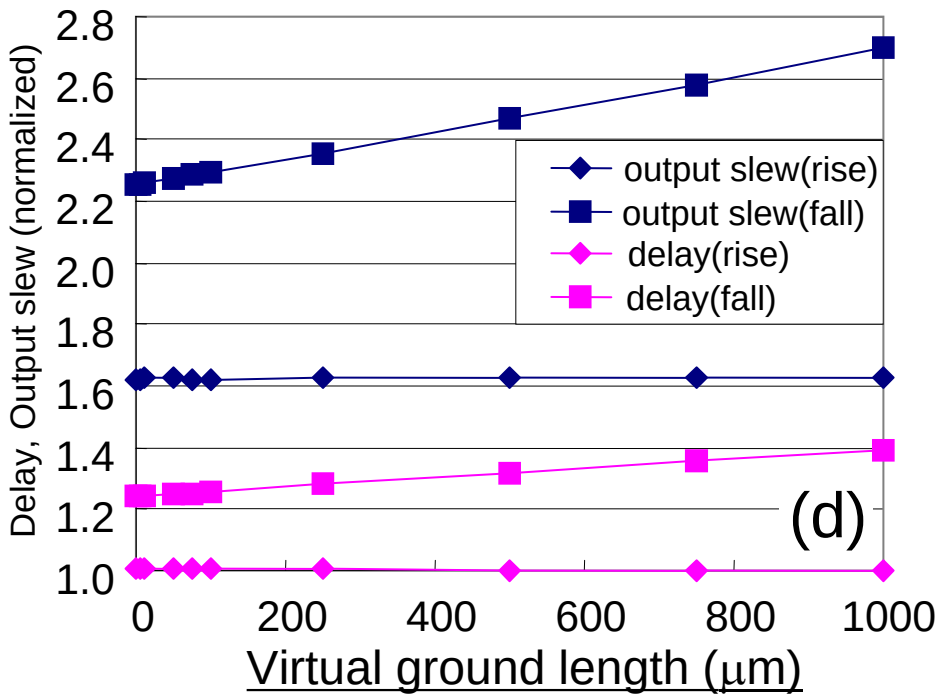
Circuit model for HSPICE Simulation (NAND)

- Modeled VGND line using π-type lumped RC circuit
- We assume the two routing layers (R and C are the same between the two layers)


output slew(rise)
output slew(fall)
delay(rise)
delay(fall)
Delay, Output slew (normalized)
6.0
5.5
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0
0.5
1
1.5
2
Input Slew (ns)
(a)


output slew(rise)
output slew(fall)
delay(rise)
delay(fall)
Delay, Output slew (normalized)
60
50
40
30
20
10
1
0
100
200
300
Output capacitance (fF)
(b)


1x
2x
15x
output slew(rise)
output slew(fall)
delay(rise)
delay(fall)
Delay, Output slew (normalized)
2.4
2.2
2.0
1.8
1.6
1.4
1.2
1.0
0.0
0.2
0.4
0.6
0.8
1.0
Inverse of power-switch size
(c)


output slew(rise)
output slew(fall)
delay(rise)
delay(fall)
Delay, Output slew (normalized)
2.8
2.6
2.4
2.2
2.0
1.8
1.6
1.4
1.2
1.0
0
200
400
600
800
1000
Virtual ground length (μm)
(d)

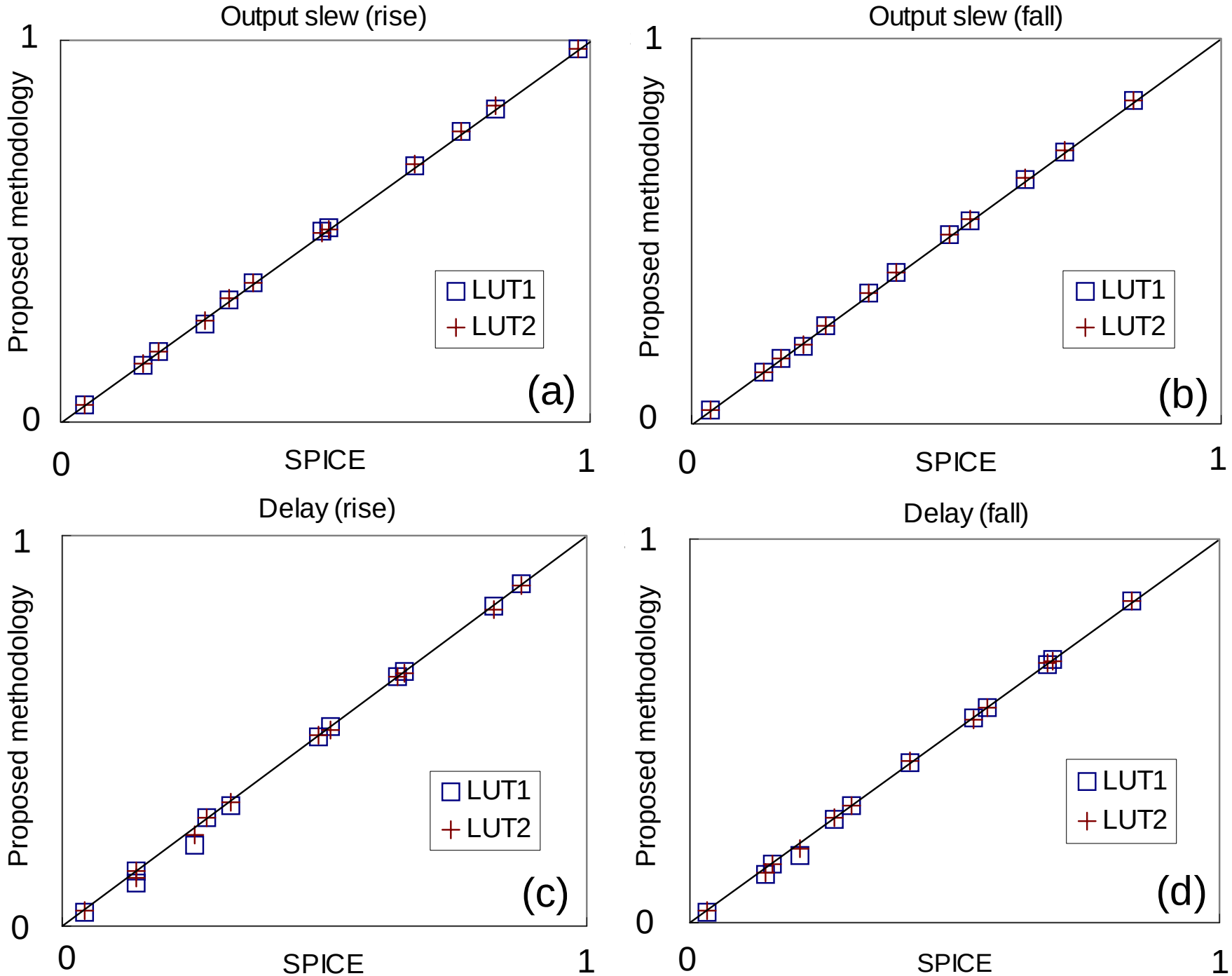
Application to a NAND Gate

- We prepared the two types of LUTs

	LUT 1				LUT 2			
Input Slew(ps)	10	600	1200	1800	10	400	900	1800
Output capacitance(fF)	5	100	200	300	5	50	120	300
Virtual ground length(μm)	1	150	300	450	1	150	300	450
1 / Power-switch size	1/1x	1/2x	1/4x	1/8x	1/1x	1/2x	1/4x	1/8x

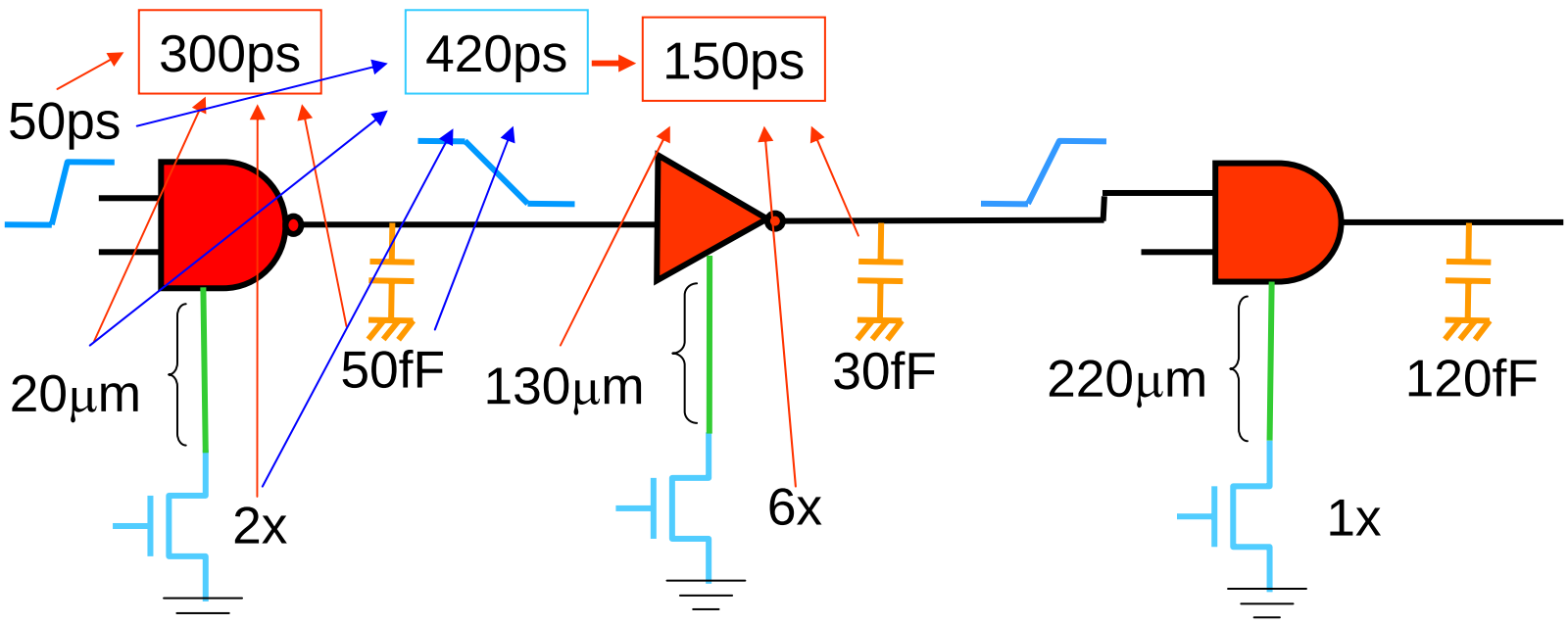
- Examine the accuracy using 12 examples

	Ex1	Ex2	Ex3	Ex4	Ex5	Ex6	Ex7	Ex8	Ex9	Ex10	Ex11	Ex12
Input slew (ps)	50	750	1600	230	610	1720	20	1010	1340	490	880	1130
Output capacitance (fF)	110	20	220	4	85	100	55	290	35	230	135	185
VGND length (μm)	380	22	75	320	120	440	95	160	310	200	140	190
Power switch size	x3	x1	x7	x9	x5	x1	x2	x3	x4	x2	x6	x8

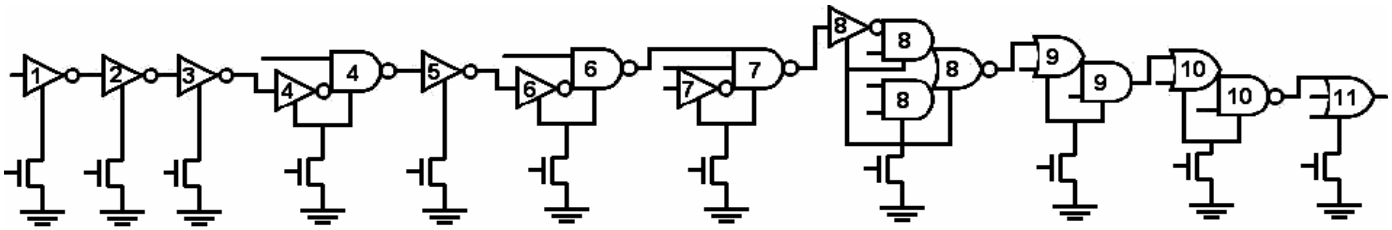

Output slew (rise)
Proposed methodology
SPICE
0
1
LUT1
LUT2
(a)
Output slew (fall)
(b)
Delay (rise)
(c)
Delay (fall)
(d)

Application to the STA

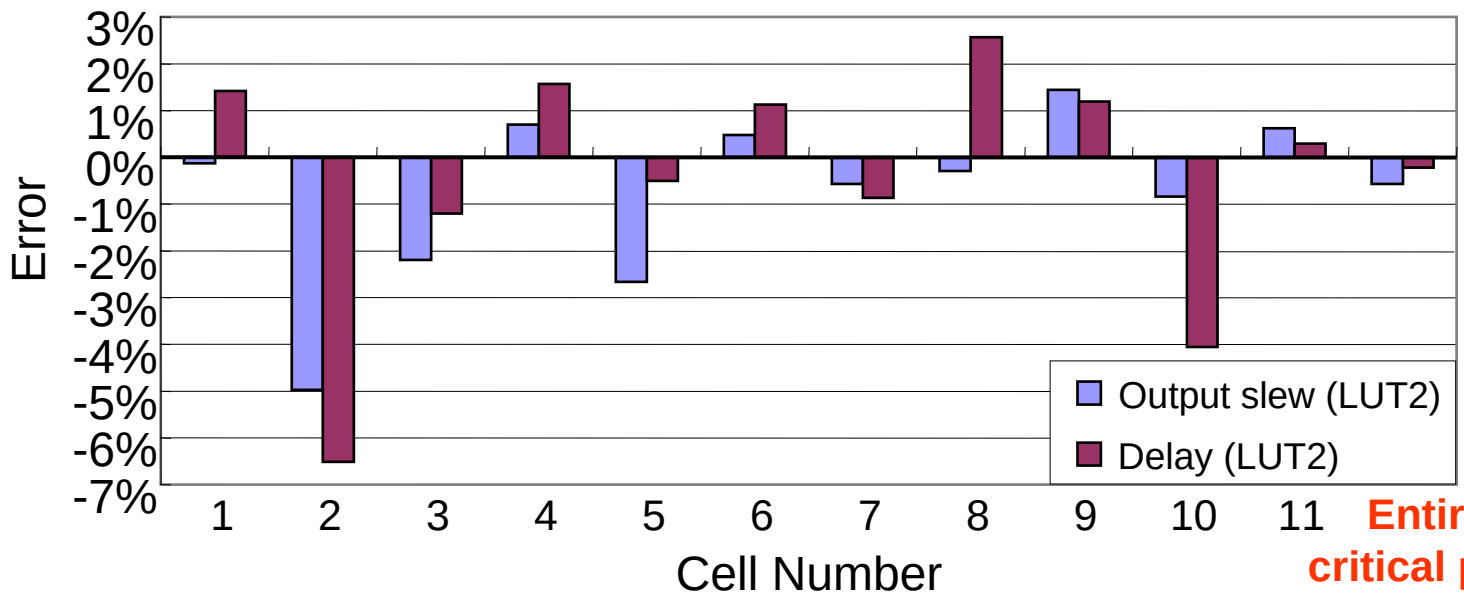
- Output capacitance, VGND length and power-switch size
  → randomly generated
- Input slew of the first gate → 50ps
- Input slew of gates at later stages
  → using the output slew of the previous gate



Results (MCNC SAND : 11stages)

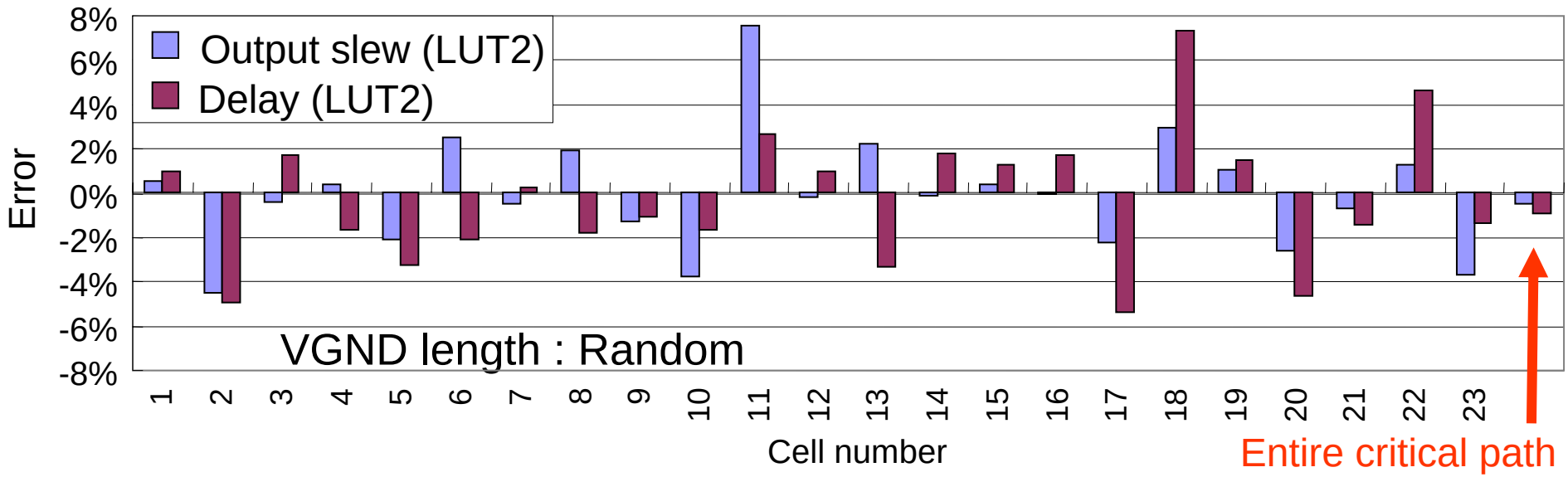


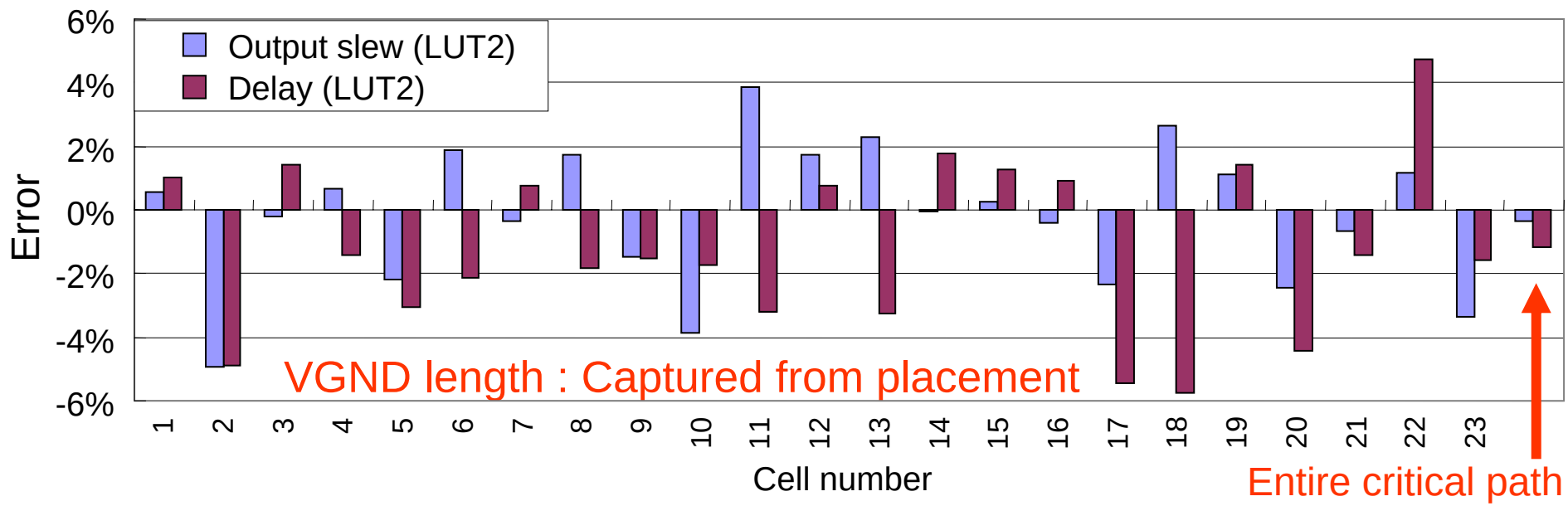
SAND	1	2	3	4	5	6	7	8	9	10	11
Cell size	x1	x1	x1	x1	x1	x1	x1	x1	x1	x1	x1
State	fall	rise	fall	fall	rise	rise	fall	fall	fall	rise	rise
Output capacitance(fF)	65	22	115	105	49	43	184	72	89	36	92
VGND length (μm)	28	121	33	62	73	49	350	185	90	5	212
Power switch size	x2	x2	x2	x4	x1	x1	x4	x3	x6	x1	x5



Entire critical path

Results (CPU Control Unit : 23stages)





Conclusions

- Delay modeling for MTCMOS circuits
  - Add the VGND length and the inverse of power-switch size as the parameters for interpolation
    - Circuit delay and slew almost linearly increase with parameters
  - Enable to compute both “rise” and “fall” delays in good accuracy
- Application to the critical path delay calculation
  - Allows to calculate the path delay within 2% error
- Future work : Extend to shared VGND circuits

END